MEMS & Microsystems
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Lecture No. # 09
Microelectronic Technology for MEMS – III

We will continue our discussion on microelectronic technology for MEMS. In the last lecture already we have discussed on the deposition techniques; namely the evaporation, chemical wafer deposition and various kinds of evaporation techniques also. Today's lecture we will continue on discussion on different topics like metallization, lithography, diffusion and ion implantation. All these steps are very much required for fabrication of micro sensors and MEMS. Let us first discuss on lithography.

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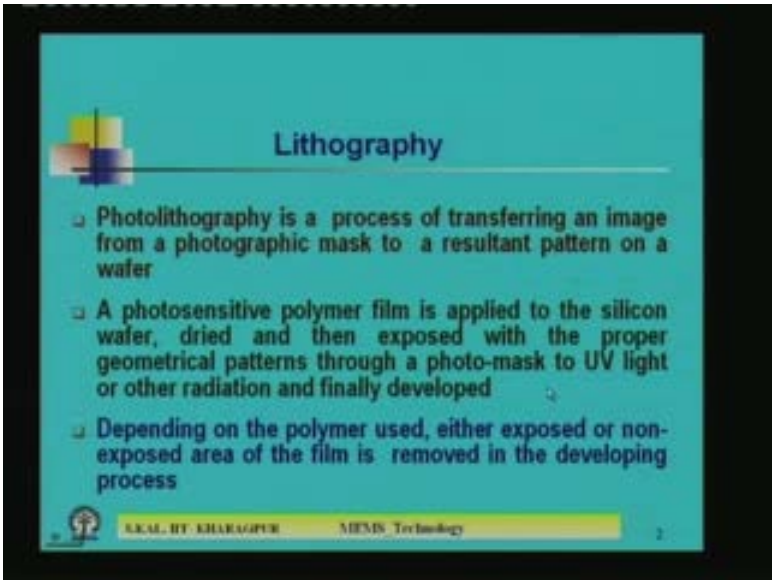

Lithography, sometimes it is called also photolithography, is a process by which we can transfer some pattern from photographic mask to a resultant pattern on a wafer. That means transfer of any kind of structure from mask level on to the wafer level is known as photolithography. What is the technique? In photolithography process a photosensitive polymer film is applied on silicon wafer. This photosensitive polymer film is known as photo resist. This film is dried and then it is exposed with the proper geometrical patterns through a photo mask to UV light or other radiation and finally developed. Instead of UV light in some cases we use x-ray, electronic beam or ion beam. Accordingly, those techniques are known as electron beam lithography or ion beam lithography or x-ray lithography. When you use UV radiation for exposing the film, then it is known as UV lithography. When you use deep ultraviolet rays then it is also sometimes known as deep ultraviolet lithography.

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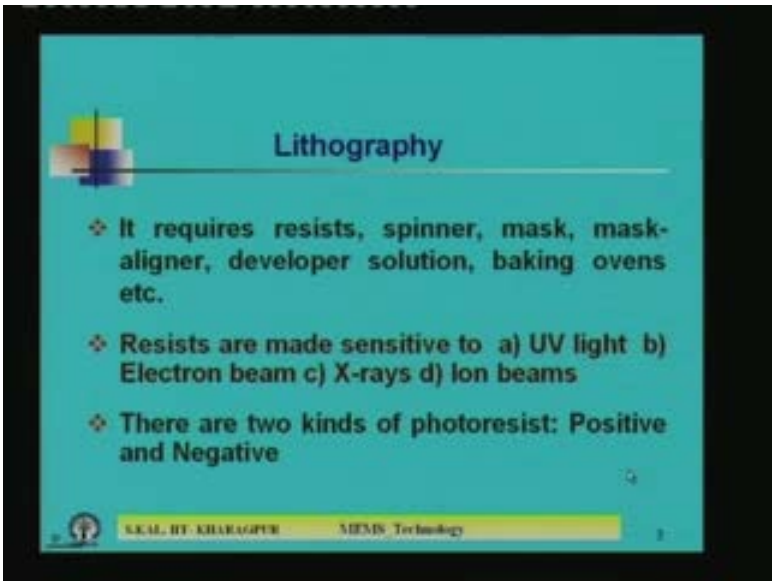

Now depending on the polymer used, either exposed or non-exposed area of the film is removed in the developing process. That means in some cases we will find that exposed portion of the film will sharpenand it will be dissolved in developer solution. In some cases after exposure we will see that this polymer film which is photosensitive has been hardened and is very difficult to dissolve in developer solution. So there are two kind of photo resist; one is known as positive, other is known as negative photo resist. Now the photolithotrophy process requires various chemicals,gadgets and equipments. Those are namely photo resists, spinner, mask aligner, developer solution, baking ovens, etcetera.

So photo resists are made sensitive either to UV light or electron beam or x-rays or ion beam. But out of all these lithography, ultraviolet exposure source is very much popular and UV lithography is very much used in most of theMEMS or VLSI process. Very few cases we require ion beam or x-ray lithography where we need high resolution and is very small picturesize,then sometimes you go for x-ray lithography or ion beam lithography. Now as I mentioned, there are two kinds of photo resist; positive and negative photo resist. They are complimentary to the each other as far as their properties are concerned.

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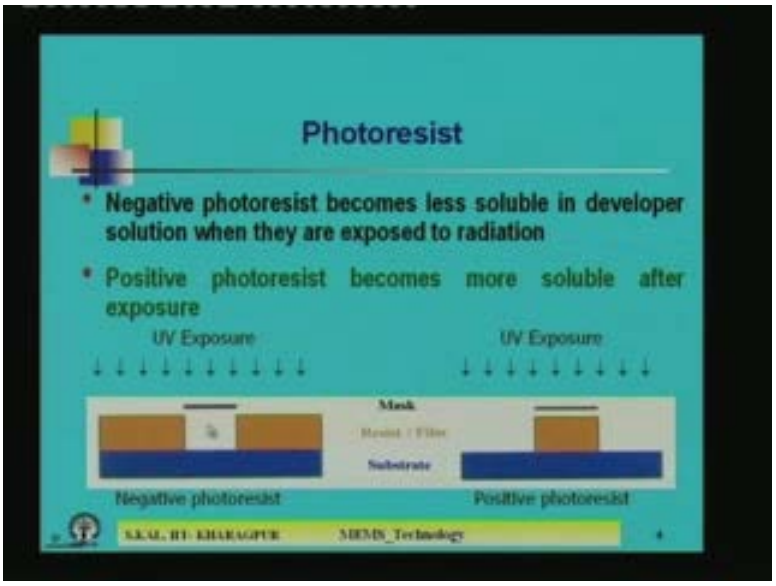

Now negative photo resist becomes less soluble in developer solution when they are exposed to radiation. On the other hand positive photo resist becomes more soluble after exposure. In the diagramthepositive photo resist and negative photo resist behavior is shown. Now you see the mask, it is a black portion here. This line is a mask, heresimilarly here the black line is the mask. So here through that black portion the ultraviolet light cannot pass. Now the blue color layer is substrate and the red is photo resist or any other film which is sensitive to radiation. Now if we expose the side by side negative and positive photo resist, thephoto resist coatedsubstrate using the ultraviolet light with the same mask, then the pattern will be different. Now here the left side of the picture you can see, when it is exposed, so this portion, red portion will be exposed with ultraviolet light and this will be hardened and unexposed portion will remain as soft.

As a result of which after developing, this portion photo resist will remove and we will get windows with the black region on the top of this particular window. Now here in the right side same mask is used where the exposed portion, for example here and here the photo resist becomes more soluble and then it will be deserved in developer solution. As a result of which you will get only this portion after development and exposure. So the last we find that if we use positive photo resist is state of negative, we will be getting this structure which is complimentary to the structure obtained in case of negative photo resist.

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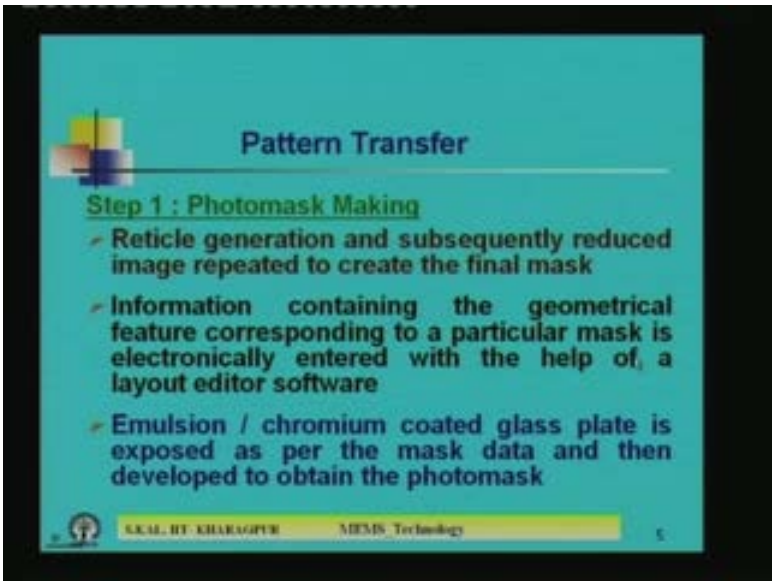

So what are the various steps in this kind of pattern transfer techniques? So the first step is preparation of the photo mask. So photo mask making that is first step, for that you have to have certain information which contains the geometrical feature corresponding to a particular mask and that geometrical feature is electronically entered with the help of layout editor software. There are various kinds of layout editor software are available. One such name is LASI layout editor. You can design your pattern and electronically transfer onto a mask making machine. Then according to the data the mask making machine will expose onto an emulsion or chromium coated substance or you can call it as a mask plate. So depending on the data enter into thepattern generator, the mask plate will be exposed and after that if you develop those masks plate, then you will be getting this structure on that particularchromium plated or emulsion coated glass plate and your mask will be made.

In some cases we initially prepare the reticle of the mask and then by step and repeat camera we can duplicate those patterns in multiple numbers, so that you can get at the same type, may be thousands and millions of chips will be exposed on the same wafer. So inVLSI process first you generate the reticle. Reticle means single chip mask. Then that is repeated in different camera which is known as step and repeat camera and then you can have the full mask which contains millions of chips. So first step of any kind of pattern transfer is to make the photo mask. After making the photo mask then you go for pattern transfer onto the wafer.

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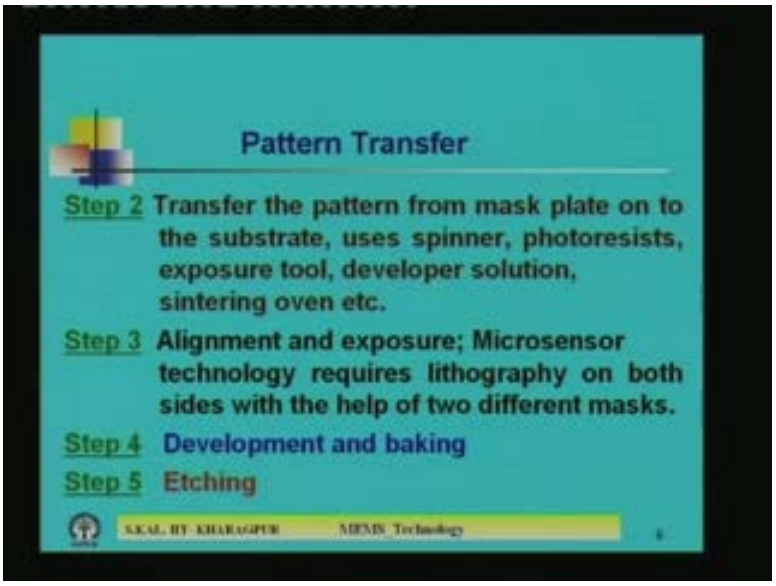

Now step two is that transfer the pattern from the mask plate onto the substrate. It uses spinner photo resist exposure tool developer solution and sintering oven and step three is the alignment and exposure. In case of micro sensor or MEMS devices, we sometimes require lithography on both side. With the top side and bottom side because sometimes you want to etch certain windows with respect to some structure at the back or on the other hand. We want to open some windows at the back side of the wafer with respect to certain structure in the front side. So this kind of alignment lithography is not required in case of VLSI fabrication. But in case of micro sensor fabrication we need this kind of double sided alignment technique.

So you have to use a different kind of mask aligner machine which is known as double sided mask aligner machine. So that you can align either front side or back side with respect to the other to create certain microstructure for your specific application. So that, here some difference is there, so far as VLSI lithography is concern. Now next step will be developing. After exposure of the film you have to develop just similar to the photographic plate developing, should develop then during developing either the soft portion or the hard portion depending on which kind of photo resistor going to use. So that we will be deserved and then you will get the pattern and after getting the pattern then you sinter whole thing then you go for etching to create certain windows or the structure finally. So that is the totalthe transfer process from mask level onto the wafer level.

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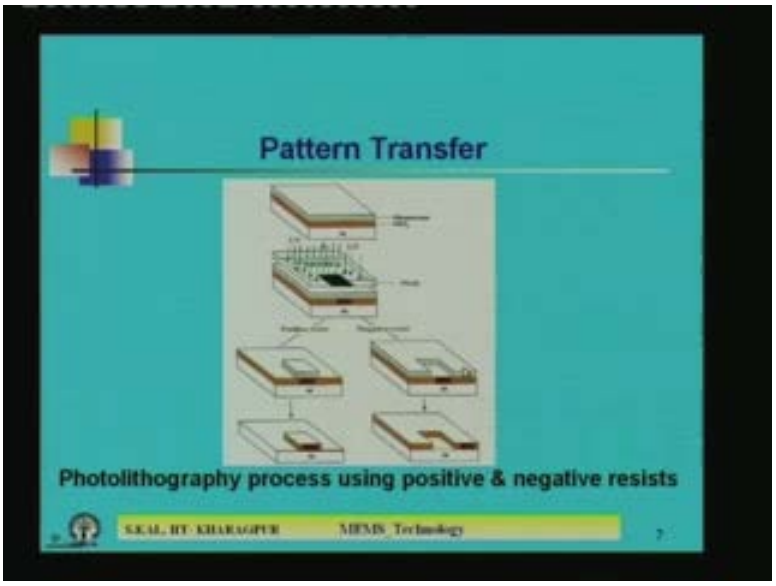

Now this is a pictorial diagram using both positive and negative photo resist to get the pattern from mask level to the wafer level. So here you can see herethe first is silicon wafer on top of that silicon dioxide and on top silicon dioxide we have coated with photo resist. Now this is a photoresist then silicon dioxide bottom is the silicon and now mask plate is aligned onto the photoresist film and on the mask plate you can see this portion is a black and rest of the portion is transparent and this is the opaque. Now through the black region which is opaque the ultraviolet light cannot pass and through the transparent region it will pass. So now if you use positive resist or negative resist then the structure will be different. Now you can see the positive photo resist case where the transparent region, particularly this portion when it is exposed. So this portion the photoresist will be softened and in the developer solution, this portion photoresist will be removed and only the black region this particular region photoresist will remain.

On the other hand if you use negative photoresist, so under exposure of ultraviolet light this portion to this portion to this portion it will be hardened. So here it is hardened and only the black region the photoresist will not be exposed by ultraviolet light. As a result here it will remain as soft and in developer solution this particular region photoresist will dissolve. Now so in positive resist in the same mask we will get this structure in negative resist when the same mask will this kind of structure. Now that is the next step? Next step is to etch the film. So nowduring etching the silicon dioxide, because this particular region it is covered with silicon dioxide and silicon can be etched here where is covered with photoresistthen silicon dioxide can be etched here. Similarly here this is the silicone dioxide,the red region is silicon dioxide so it is a photoresist. So now through the photoresist window you can etch silicon dioxide. Only this portion, as a result of which you can get windows, here on silicon. Similarly here the complete silicon dioxide film will be etched and the covered region the silicon dioxide will remain. So in the same structure if you go for positive or negative this similarsuch kind of pattern you will get after development and etching.

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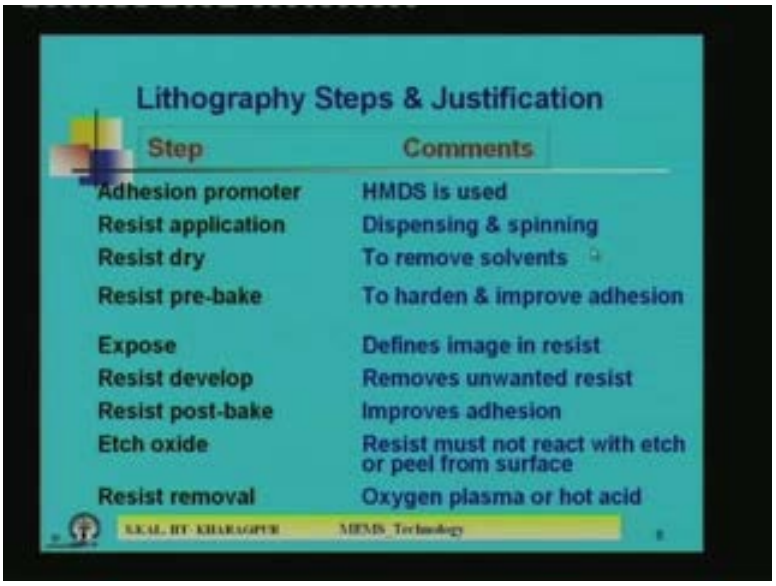

Now the steps of lithography are shown here along with the justification. In some cases we found that because ofthe inadequate surface, inadequate quality of the silicon dioxide or silicon surface. The photoresist will not properly adhere to the substrate. In that case you have to use some addition promoter. So addition promoter helps to properly adherence with the photoresist film and silicon or silicon dioxide film. So it is very important because untiland unless the photoresist adherence with the substrate is not proper. So in the subsequent process photoresist can peel off so then you cannot go for the full complete etching or developing steps. So you have to ensure that photoresist will adhere properly on the silicon dioxide or silicon surface and this is very important as I mentioned. Why it is important? This kind of problem sometime you can face if the oxide quality is not good and oxide is contaminated or the substrate is not properly clean.So in that case the adherence will be poor. Some remedies are there. This adherence problem is much more severe if you go forvery fine line lithography.

If you go for resolution of 1 micron or some micronkind of structure, then if addition is not 100 percent perfect then there is aproblem of CPH of the developer solution to the side of that photoresist film. As a result of the structure will not be according to your design and the resolution you will not get. So in case of thedesigning ofmicron or some micronkind of structure, the addition promoter is very much essential and one of the addition promoters is HMDS. So HMDS film initially coated on silicon dioxide surface and then you go for spinning photoresist. So, after that resist application and that is the technique is dispensing and spinning. That means, dispensing mean you justput the photoresistenough amount of photoresist on the surface of the silicon dioxide. Then you spin the silicon wafer, spinning is require to get uniform photoresist thickness. So, if you spin of photoresist material is a liquid material. If you put that enough amount of liquid on the surface of the wafer then you spin it suddenly with the certain speed and that speed is nearly 3000 to 4000 RPM. Then you will find the thickness of the photoresist film where the entire wafer will be uniform.

Why you need uniform? The reason or the requirement uniformity of the thickness lies uniform exposure. Because, if you see during exposure, the ultraviolet light will react with the photoresist film. Now, if the photoresistfilm thickness is different. The time required for complete reaction will be different at different region. Where thin photoresist film so reaction will be completed very fast. Where the photoresist film thickness is more, then the time requirement for complete reaction that polymerization that is known as polymerization will be more. So as a result of which is some portion will be developed very fast and some portion will not be developed where the reaction is not completed. So because of that we need the uniform thickness photoresist film so that uniformly and equally over the entire surface of the silicon, the reaction will be completed. So that the developer solution and at the same time the structure will be developed.

Non uniform thickness of the photoresist will lead to or non-uniformthe structure appearance on the surface after development. In some cases the structure will much more prominent; in some cases it is not prominent. So after that you are drawing the photoresist and why you are drawing? To remove the solvents. Because there is a liquid. Why liquid? Because we have to spin and if it is not liquid, you cannot spin on the surface. So afterspinning here the solvents are removed by drawing the photoresist. Next step is a resist pre-baked that drawing means when you are spinning automatically the solvents will be evaporated. After that pre-baking at certain temperature you have to pre-bake the film to harden and improve the adhesion. Next step is expose and where you defines the image in the resist after that is resist develop which removes unwanted resist. So in developer solution what will happen? As I mentioned, that soft region will remove wash awayin the developer solution and hard region will remain. So that removes unwanted resist in developer solution.

After that resist post-bake when you are developing then again you are putting the whole thing in the liquid. So those developer solutions will be there on the surface of the photoresist as well as substrate and some of the developer solution will be absorbed by the film. So as a result of which the film photoresist, film will be soft and again you have to dry before going for actual silicon dioxide etching. During that drawing which is known as post baking, again the photoresist film will be completely adhere on the substrate. So that will improve the adhesion. After that you etch the oxide and here you have to see, resist must not react with etch or peel from the surface. When you are etching silicon dioxide, then the protected silicon dioxide should be ideally protected. That means on that silicon dioxide there is a film of photoresist and the etching solution of the silicon dioxide should not react with the photoresist or in that solution. Which is in case of silicon dioxide is buffer hydrofluoric acid you know.

The buffer hydrofluoric acid will not react with the photoresist or it will not help the photoresist to peel off. So that we have to be ensure. Now after developing is completed, then post baking is done. Next step is resist removal. So thendeveloping completed photoresist post bake and then oxide is etched and after oxide is etched then the job of the photoresist passivation is over. So this protection layer is not required, then you have to remove the resist and that removal is done with the help of either oxygen plasma or hot acid and that hot acid sometimes in case of negative photoresist we use $H_2O_2$and H_2SO_4 , 1:1ratio which is known as a Caro's acid. In case ofthe positive photoresist we used acetone, hot acetone or sometimes it is usedis a special photoresist remover solution. From the photoresist supplier they can give some can,they also specify

somechemical for photoresist removal. Or if you go for dry removal then you can go for oxygen plasma and that also etch photoresist. So this is the complete steps along with justification.

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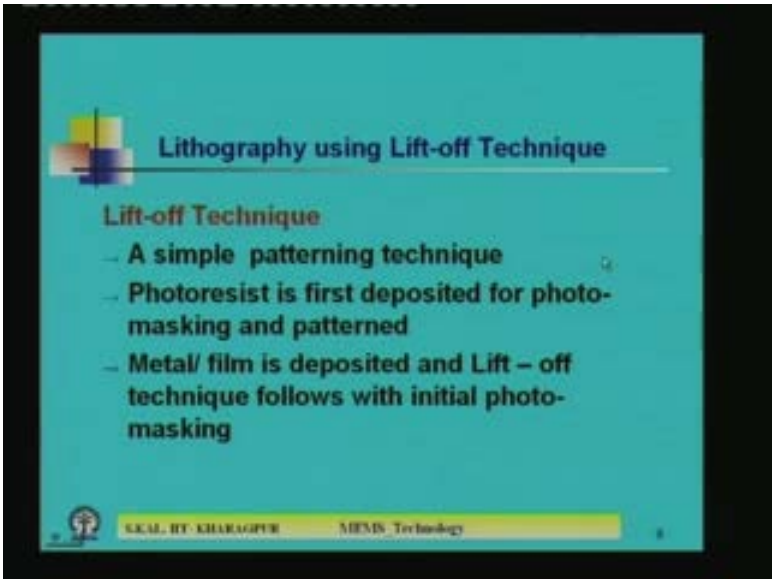

Now there is another kind of photolithotrophy technique which is known as lift-off technique. So lift-off technique is a special technique where you donot require the etching solution of the film. So in some cases we may not know the etching solution. For example if you are going to design or pattern, a tungsten film or molybdenum film or some other, say ceramic film whose etching solution is not known. But you want to pattern it, so in that case the ideal technique is to use lift off technique and lift off technique is totally different. Here what wedo? We pattern the photoresist instead ofnormal photolithotrophy. First we deposit the film or in case of silicon dioxide, silicon dioxide you grow it or in case some metal we first deposit metal and then we coat photoresist, then you go for patterning. But in case of lift off technique we donot deposit film or grow silicon dioxide. First we coat with photoresist and we get the pattern. Then we will deposit film, then the photoresist is first deposited for photo masking and pattern and then metal film is deposited and lifts off technique follow with the initial photo masking.

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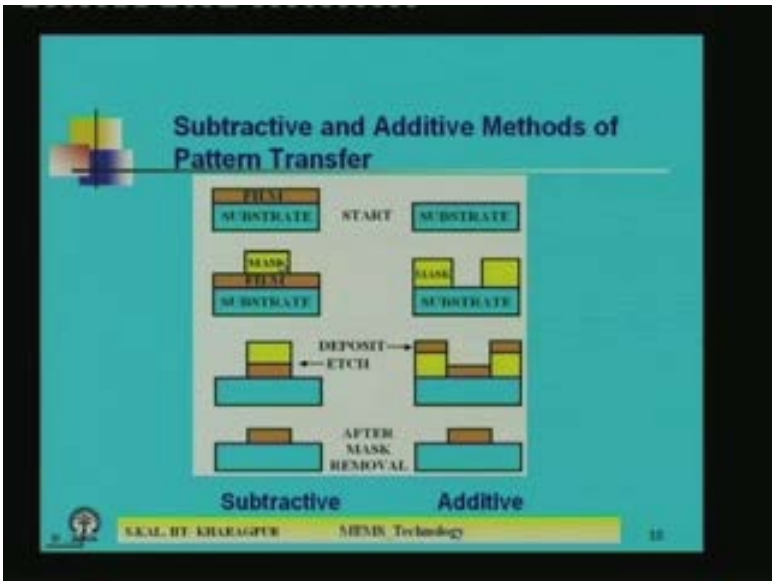

So let us see in the picture. What is the difference in this picture? What is the different between normal photolithotrophy and the lift-off technique photolithotrophy? So normal photolithotrophy is known asthe subtractive method and lift off technique is known as additive method of pattern transfer. So subtractive method means here what I discussed in earlierview graph, that film substrate. Then this is the mask thenthis film is, for example the mask is the photoresist and the film is say silicon dioxide for example. So now the mask, then here you can etch the silicon dioxide. Then what do? You can remove the photoresist, you can get the pattern. This is the silicon dioxide pattern. Now this is a normal, but in case of additive thewhat wedo? On the substrate instead of depositing film we first deposit mask. What is the mask means photoresist. You can see the difference. Here first film that film may be either aluminum in case of metal or it may be silicon dioxide. So we have coated first. But here what we did? First it is coated with photoresist and then on photoresist you pattern it and after that we deposit the dissolved metal silicon dioxide.

Not initial silicon dioxide, in photoresist, first photoresist is deposited, then pattern, then we depositeither metal or silicon dioxide here, that is the film. Now what we do, after this we just dip the structure into a photoresist removal solution. So if you dip the whole thing in photoresist removal solution, what will happen? You can see here the developer solution or the photoresist remover solution I could say. The photoresist remover solution will remove photoresist from this portion and from this region it will react the first photoresist remover solution will react with the photoresist here and here. As a result of which photoresist in this region and this region will deserve and these two portions will be floating and that will go away and you will get this structure here. So if both cases we got the same structure here. But in this particular case you need the etching solution of the film. But in this particular case we do not need the etching solution of the film. So this lift off technique is used in some cases where the etching solution is not known or you know the etching solution. But that etching solution will react with the photoresist film.

If that etching solution react with the photoresist film, in that case also photoresist will not protect the surface. When you are going to etch the film here so then here you will say photoresist will be reacted and film also will be reacted. Then whole thing was there. So but here if you need something, some solution which can react, which can dissolve the photoresist, but not the film. So that is innormally we use the positive photoresist and in that case positivephotoresist remover solution acetone. So here after this step you just dip the whole thing into the hot acetone. So acetone will remove the photoresist and you will get the structure here. But here one limitation is there. What is the limitation? Now you can see from the diagram, the photoresist will react only through this portion or this portion. Now if I use the thickness of the mask means photoresist film, is very small. So that thisportion isbecause this is very low. So this portion will be nearly here. So there is no chance of attaining photoresist from this side or this side.

So in that case the photoresist will not be removed. So one condition you have to satisfy. What is that condition? The film thickness should be smaller than the photoresist. This is the film thickness, the red region, it should be smaller than the mask means photoresist thickness. That means thickness of the photoresist should be large. Otherwinse this sort of large compares to what, large compare to the film thickness. So otherwise you cannot go for the lift-off technique. So if you can get thicker photoresist film, for that you have to use this special kind of photoresist, positive photoresist whose viscosity is more and by which you can pattern larger thickness resist. So this is one condition, if you satisfy then easily you can pattern without knowing the etching solution of that particular film. So this is very much used in many cases of pattern transfer.

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Now next step is the metallization. So metallization requires after completion fabrication of the individual devices. That means if you fabricate, say some resistance or you can fabricate some transistors or diodes, then at the end you need interconnection of these components or devices. For that you need a metal film and metal film is etched and as a result of which you can get the interconnect lines. So now when you go for metallization there are certain thumb rules to select

the metal film which will be suited for your application or your device. What are those points? Number one is low resistivity or high conductance, easy to fall. What does it mean? Obviously the metal lines are used for interconnection or contact. So its resistivity should be low. If it is not low, then what will happen? So total interconnect line will give you certain resistance and that resistance will be parasitic I can say and that will reduce the speed of your circuit. Because adhesion resistance is coming into the picture which is not desired.

So in high speed circuit or any of the VLSI circuit which the metal lines are required only for interconnects. So their resistance should not be incorporated. So low resistivity should be there. That means high conductor and easy to form. Easy form means that metal film can easily pattern. That means there are certain metal film by lithography you cannot get the pattern. One such is say copper. But you have to go for certain metal film so which can be easily patterned by conventional lithography and etching technique. For example gold, aluminum are most choiceable material for metallization or any integrated circuits or VLSI. Low contact resistance and non-rectifying contacts. So metal films are used for contacts also. So the contact, that means the silicon and metal contact, so that must be omit, non-rectify. If it is a rectifying contact, then at the contact position unintentionally fabricating some diodes, which is metal semiconductor junction diode. So metal semiconductor junction should be omit for ideal contact. So that all the metals with silicon will not give you omit contact.

Some of the metal combinations with silicon give rectifying contact. So when you will select the material you have to care of that aspect. So the contact must be omitted, so that you can choose the proper material. Others is the low contact resistance, because in VLSI or even in MEMS devices the contact windows are very small and in some cases you go for say even 5 micron by 5 micron contact in some cases 10 micrometer by 10 micrometer contact. If you go for VLSI devices the contact windows are getting more and more, smaller much more, smaller. So in that case if it is a small it will introduce some contact resistance and that contact resistance should be as small as possible. Otherwise additional parasitic resistances are coming into the circuit. So that you have to shaped and controlled as required. That means what does it mean?Your metal film which is being used for metallization must be safe means it will be lithographically compatible. So later that metal film can go for lithography process and it will be patterned using conventional lithography. That is shaped and controlled as required, has mutual solubility with silicon, that is another aspect.

So if that metal film does not mutualthedoes not dissolve into the thin layer of metal, you will not get proper contact. Mutual solubility with silicon. That means at the interface the metal and silicon will form certain alloythat is mutual solubility. Otherwise contact will not be proper. It is very important aspect when you are selecting a material. Next is it penetrates thin native oxide. When you deposit metal film on silicon then always bear silicon you will not get it and a native oxide will be there even you clean the wafer and then go for buffer hydrofluoric acid dip. So when you are transferring the wafer into a vacuum chamber for deposition of metal film, during that period a thin layer of native oxide may be in the range of 2 to 3 angstrom unit so that will be formed and that native oxide is very difficult to remove from the silicon. So ason top of that, you are depositing aluminum. So that means aluminum must penetrate to that native thin film of oxide. Otherwise if it cannot puncture, you will not get good proper omitted contact.

So the metal film which you are selecting for metallization must penetrate to that thin layer of oxide. Next is a mechanical stability, good adhesion and low stress. Good adhesion is obviously you require, low stress that means you are depositing metal film on silicon. So silicon the metal and this metal film will run on silicon dioxide. So that means silicon dioxide, silicon and the metal that must produce low stress. Because subsequently if you go for high temperature step for annealing. So then after annealing when you are cooling down, so if there is no compatibility on the thermal expansion coefficient, so a stress will be developed and if a stress develops, so in metal film in some bump may create and you will not get proper contact there. So because of the stress, sothe metal film can bend and it can peel off from the surface, so that you have to take care.

So that mean low stress is desirable, mechanical stability should be high. Because when you are patterning so if100 or 1000 microns or millimeter length and with these of the order ofsay 5 micrometer to 10 micrometer, then these narrow lines in subsequent process must be mechanically stable.So during subsequent process said those lines should not come out from the silicon surface. So that is mechanical stable means it will not only adhesion, it should not, there should not be any crack on the lines. So there should not be any discontinuity in the line so that mean mechanical stability is highly desirable. Metallurgically compatible with silicon other metals and passivation. Metallurgically compatible means the equal form with that proper align with that silicon or other metal. For example in multilevel metallization or multi-layer metallization sometime you deposit gold on chromium sometime in between chromium, gold, aluminum you can use the titanium as a differential layer.

So that means with titanium and gold it must be metallurgically compatible that mean it may formthe layer by layer it willshow its own identity in the multi-layer environment. So those are known as metallurgically compatible. So next point you should not contaminate wafers or working apparatus. The metal which you are selecting should not contaminate the wafers or working apparatus. Next point is minimal junction penetration and low electromigration. So the metal film should have low electromigration. What is electromigration? If you apply field electric field, then the metal molecules or item should not migrate. Because electric field will be high because in VLSI metallization. If we even if we use say1.2 volt supply or 5 volt supply, so if the lines are very narrow, so field developed in one end to other end of the metal line will be very high. If it is exceeds 10 to the bar 6 volt per centimeter, then there is a possibility of migration of the molecules. In case of aluminum metallization, aluminum molecules will separate from each other.

So as a result of which there a chance of open circuit into the line and those aluminum particles after migration if it falls on nearby metal line, so there is a possibility of short circuiting of the first metal line in the neighbor metal line. So in due to the migration of the of the aluminum molecule both open circuit and short circuit is possible. So that you have to take care of. Another is minimal junction penetration. That is very important if you go for shallow junction devices. If the aluminum penetrates through the silicon because aluminum dissolves in silicon and it goes into deeper layer into the silicon it may shocked the shallow junction. If the junction depth is not very high, there is apossibility of shocking the junction. So that also you have to take care. That mean there are lots of points which you have to take care of when you are selecting a certain metal for metallization.

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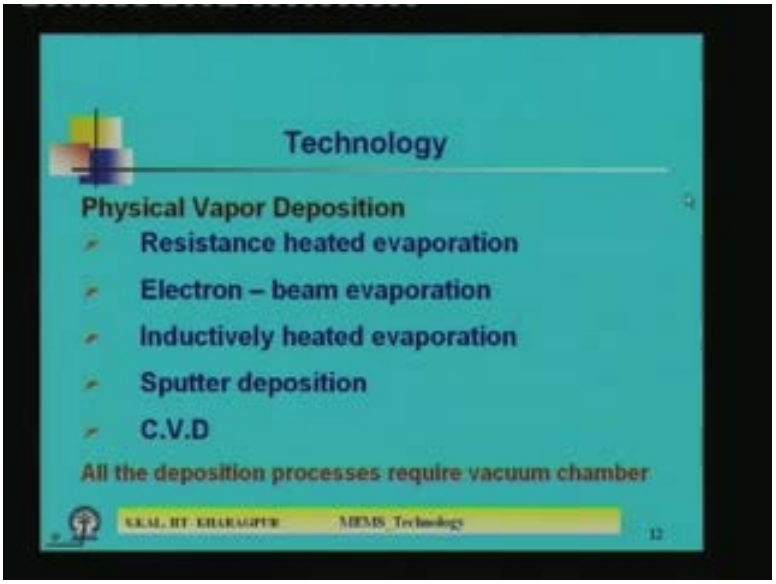

Now what is the technology of metalizaton? There are various kinds of methods used; one is resistance heated evaporation that I have already discussed in the first lecture of themicroelectrical technology for MEMS. Various kinds resistance heated evaporation is being used, that is you seethedifferent of kind elements are used that already I have electron beam evaporation I have discussed. Inductively heated evaporation I have discussed, sputter deposition and CVD. All these techniques which are used forfilm deposition means say silicon or polysilicon or oxide film. The same techniques are being used for deposition of metal films also. All the deposition process require vacuum chamber.

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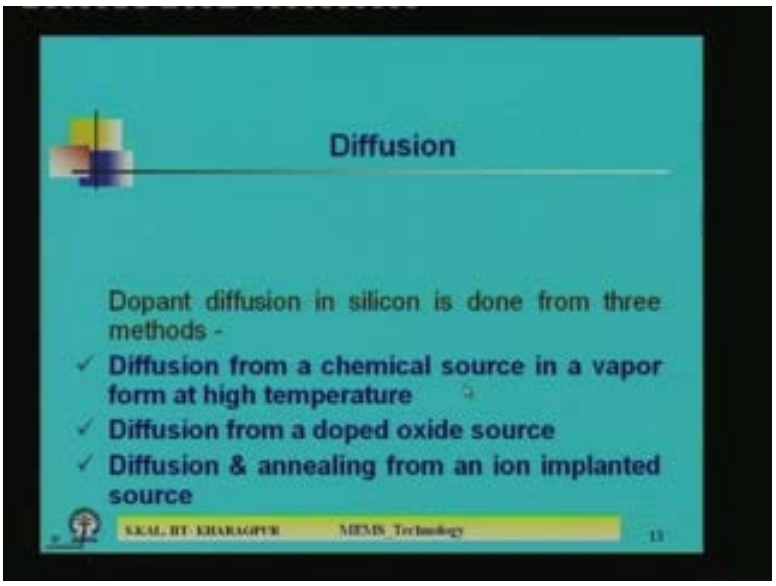

Now I will discuss on diffusion. So diffusion in silicon is donefrom three methods. What are the three methods? Diffusion from a chemical source is a vapor form at high temperature, diffusion from a doped oxide source, diffusion and annealing from an ion implanted source. These are these are the 3 techniques which are used for diffusion of impurity into the silicon.

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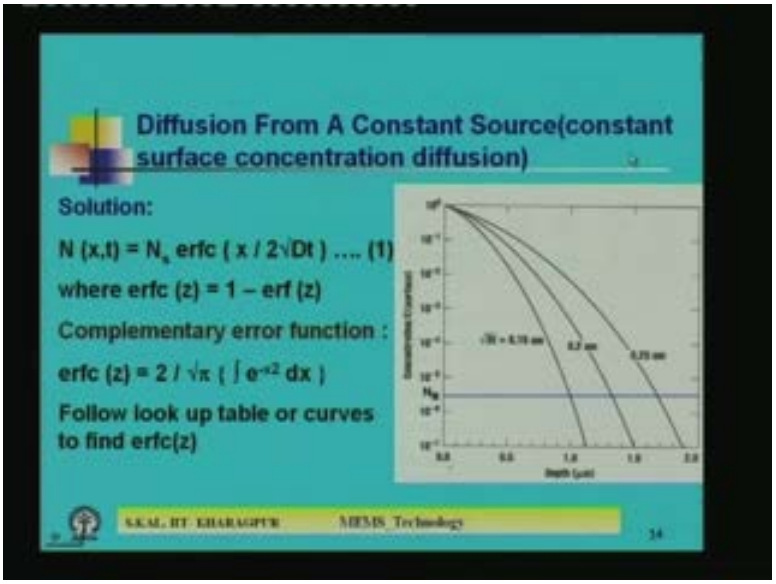

There are two of kind diffusion.One is known as diffusion from a constant source which is known as constant surface concentration diffusion and diffusion equation you know you fix law that if you shock in this particular situation. That means constant diffusion from a constant source then you will get the solution N x t is equal to N_s complimentary error function X by 2 root Dt. So constant surface concentration diffusion means that at the surface, the supply of the dopant atoms will be infinite. So continuous supply is there, so the surface concentration will be constant at the surface. Then if you increase temperature and time is small t and temperature lies in D. D is the diffusion constant, is a function of temperature and small t is the time. So total deciding factor is D and t product. So DT product if you increase so the impurity atoms we will diffuse more and more and if NB is the background concentration. If you diffuse for longer time then the junction depth will be more and more. So this is Dt, under root Dt is 0.15 micron you can get junction depth nearly 1 micron. If it is a 0.2 micron junction depth you are getting nearly 1.4 micron, if it is a 0.25 micron a junction depth you will get nearly 1.6, 1.7 micron.

That is more means two way you increase product of DT. One is you can increase the time and another you can increase the temperature. If you increase the temperature then capital D will also increase. So this is a function of temperature and this complimentary error function diffusion. We use the error function and error function is defined by this equation and the value of the error function is curve is a not a close loopformerly. You have to search some tables of curve to find theerror function value. If you know the error function value, you put it here and you can get the doping concentration at different X value and the complimentary error function profiles are like this.

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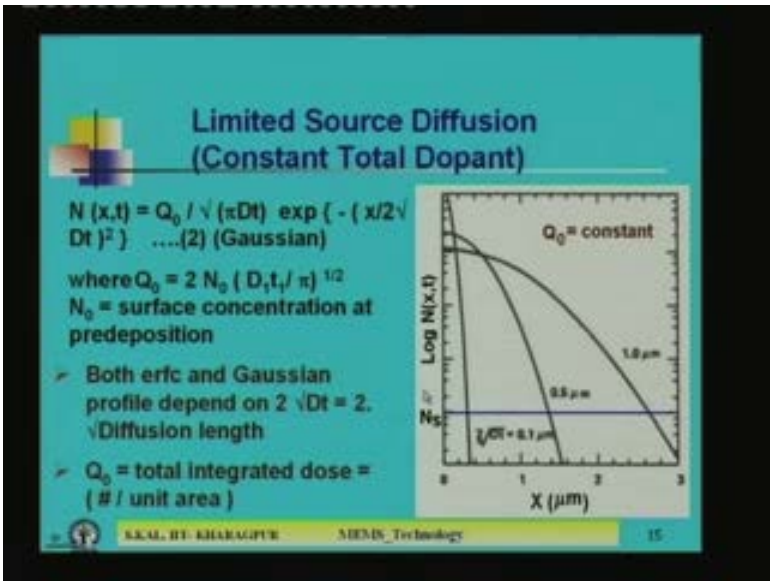

There is another kind of diffusion which is known as constant total dopant.So constant total dopant means at the surface of the silicon the supply of the dopant atoms are not infinite. A fixed amount dopant is supplied then you cut the supply of impurity atom. So as a result of which, what are the constant dopant lying on the surface, those dopants will go gradually into deeper into deeper into the silicon layer and as a result of which surface concentration goes down. That you see initially the surface concentration is here and the supply of dopant atoms is fixed. So if you go for longer diffusion either you can increase the temperature a longer time, as a result of which the dopant atoms will go much deeper into silicon. As a result of which surface concentration goes down again. If you go for further diffusion, that mean you see the root over Dt, that is 0.1 micron to 0.5 to 1 micrometer. That mean if you increase the t much more then surface concentration further goes down. But as a result of which the junction depth will get larger and larger. This kind of profile is known as Gaussian profile and basically it is a half Gaussian.

So this is sometimes known as limited source diffusion or Gaussian diffusion and here if you shock the fixed law, the doping concentration is given by N X T is equal to Q_0 by under root 5 Dt where $Q_0$is a total dopant of the surface and which is constant as far as limited source diffusion is concern and $Q_0$is given by twice N_0under root $D_1t_1$by pi and $N_0$is the surface concentration and at the deposition. Now both error function and Gaussian profile depend on two under root Dt means 2 multiplied by under root diffusion length.Dt product is sometime known as a diffusion length and $Q_0$is the total integrated dose. That is number of impurity atoms per unit area. So this is these are two kinds of diffusion. In normaldiffusion technique we use 2-step diffusion. One is known as pre-deposition; diffusion other is known as the drive-in diffusion. So pre-deposition diffusion is controlled by error function diffusion and drive in diffusion is controlled by the Gaussian profile.

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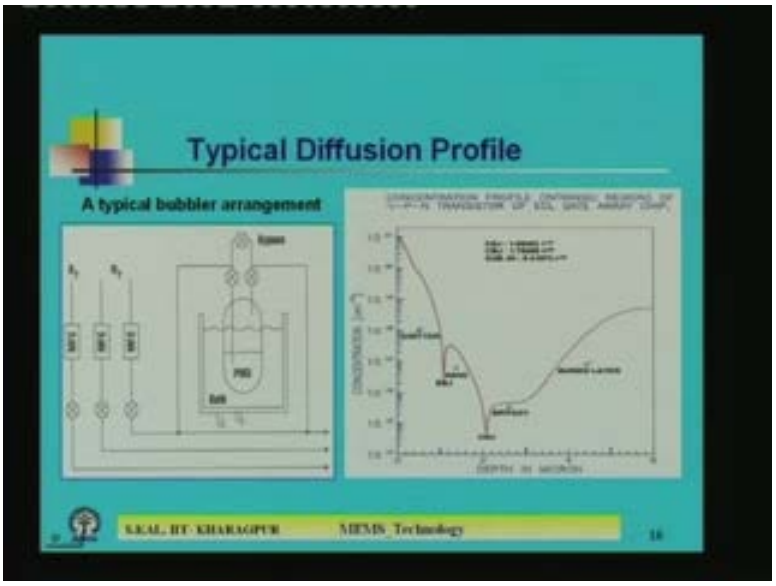

Now typical diffusion profile in a particular transistor is like that. This is the emitter region, so N plus diffusion, this is the base region P diffusion,and then it is a epitaxy, N epitaxy then N plus. So these are the typical doping profile in a NPN transistor. In this side a bubbler arrangement is shown through which you can justpush dopant atoms into a bubbler and then the dopant atoms in the form of gas and it is flown into the tube. So that for example if you for thephosphorus diffusion one of the liquid source is POCLC, this POCLC phosphorus oxychloride. So then raw phosphorus oxychloride is not enter intoit is not passed through the tube which we do normally some carrier gas is used which is nitrogen. The nitrogen is bubbled through this POCLC. So POCLC wafer along with THE nitrogen that it flows into the chamber and there silicon substrates are keep and the POCLC will react on silicon ultimately phosphorous atom will come out and that phosphorous atom will go into the silicon. So this kind of the bubbler arrangement is used for incorporation of dopant wafer into the diffusion tube.

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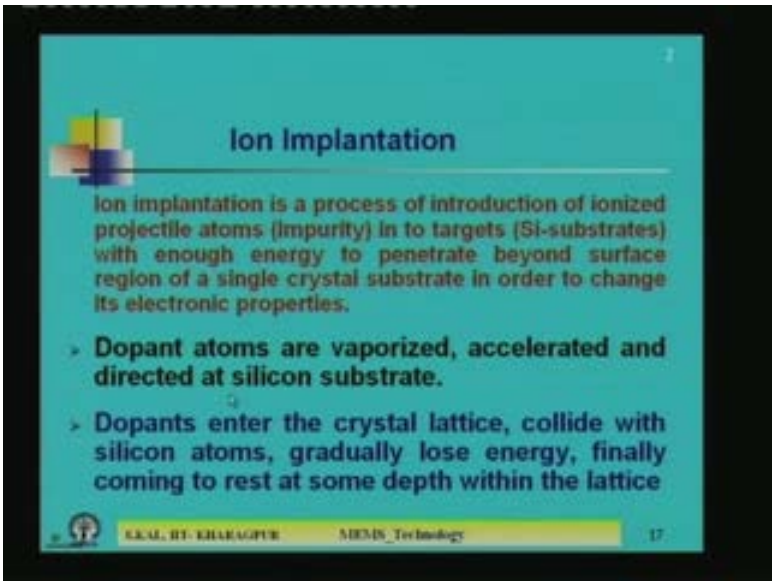

So now, next step is the ion implantation. That is another kind of technique by which you incorporate dopant in a controlled manner. So ion implantation is a process of introduction of ionized projectile atoms which we call impurity into targets and the targets here is silicon substrate with enough energy to penetrate beyond surface region of a single crystal substrate in order to change its electronic property. That is the definition ion implantation and how it is done? First the dopant atoms are vaporized, then they are accelerated and then directed at the silicon substrate. That mean there are three steps the dopant atoms are fast vaporized it has to be in wafer form then it has to be accelerated. So the energy of the impurity atom will increase, so after acceleration then they are focused and directed towards the silicon substrate where it will collide into the substrate and it will go deeper into the silicon. That is the physical bombardment process ion implantation. Dopants enter the crystal lattice, collide with silicon atoms,and gradually lose energy finally coming to rest at some depth within the lattice that is the process. First collusion it will lose energy and during after losing energy, it will settle down at a particular depth on the silicon that is the steps.

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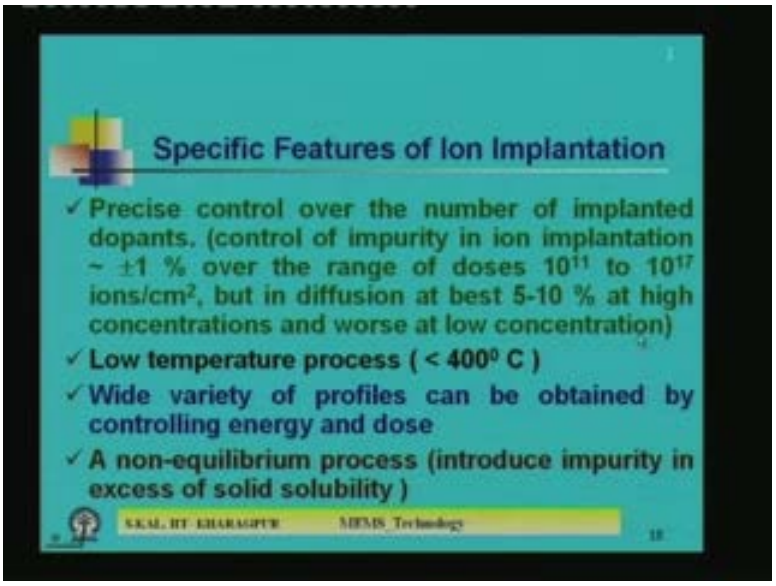

Now what are the specific features of ion implantation? You can get precised control over the number of implanted dopants. The control of impurity in ion implantation is of the order of plus minus 1 percent over the range of doses 10 to the bar 10 to 10 to the bar 17 ions per centimeter square. But in diffusion at best 5 to 10 percent at high concentration and worse at low concentration. That means what is that? You can get the control of impurity atom plus minus 1 percent in case of ion implantation. In parallel you can see in case of diffusion the control is 5 to 10 percent. So much more precised doping profile, much more control on the dopant atom is possible in case of ion implantation. What isanother aspect, is a low temperature process. Ion implantation is a low temperature process. It is done below 400 degree centigrade where diffusion is a very high temperature process and normal temperature range is 900 to 1100 or 1150 degree centigrade and now days all VLSI process people prefer low temperature because of the out diffusion of impurity.

Because the problem of rearrangement of dopant atoms and further diffusion which will clean the doping profile, that people try to get read up and as a result of which low temperature process is highly desirable and then ion implantation is one of the choices method of incorporation of impurity atom into the silicon. Why a variety of profiles can be obtained by controlling energy and dose which is not possible in case of diffusion? Different kinds of profile you can get by controlling energy and dose I will show you some dopingsome profile diffusion profile curves in ion implantation which will show you how the various kinds of doping profile you can achieve. Ion implantation is a non-equilibrium process. What does it mean? That means it can introduce impurity atom in excess of solid solubility, which is not possible in case of diffusion. Diffusion maximum dopant incorporation is up to it solid solubility limit beyond that you cannot do it. But in ion implantation you can do it. The impurity atom makes it solid solubility limit. That is why it is known as non-equilibrium process. Diffusion is not a non-equilibrium process.

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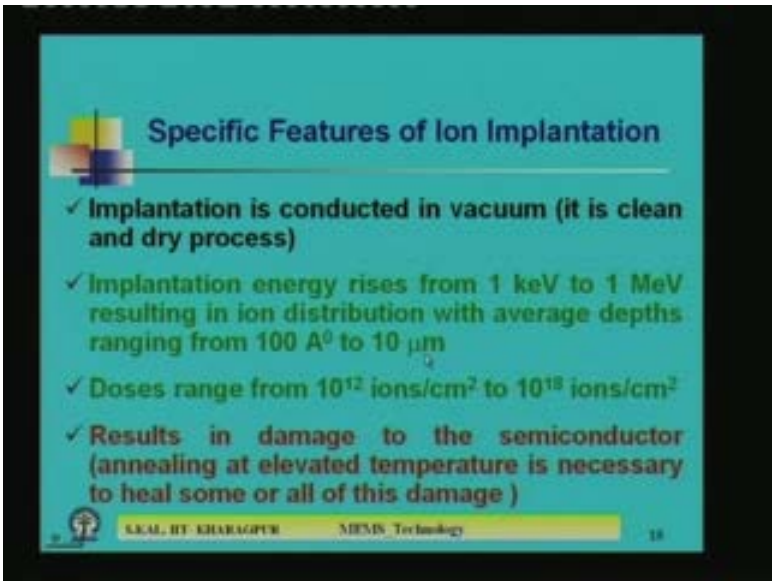

Other points are also there. Implantation is conducted in vacuum, so you can expect clear and dry process diffusion is not in vacuum in normal atmosphere. So there is chance of incorporation of dopantimpurity atoms, other than the dopant atom. So it is a clean environment clean process is ion implantation. Next point is implantation energy rises from 1keV to 1MeVresulting in ion distribution with average depths ranging from 100 angstrom to 10 micron. You can get 100 angstrom depth, diffusion depth which is not possible in case of diffusion by controlling energy. So low energy ion implantation of the order of1keV,2keV,5keV you can have very shallow depth junction. Sonowadays shallow diffusion are all made by ion implantation, not possible in diffusion. On the other hand if you use high energy ion implantation in the range of one MeV you can get higher depth. So in SY device, they are silicon and insulated devices. So normally high energy implantation is required they those kind of things you cannot get in case of the diffusion.

So doses range from 10 to bar 12 angstrom per centimeter square to 10 to the bar 18 ion per centimeter square. So those basically gives you the resistivity value energy gives you the junction depth.How much deeper you canimplant the dopant atom and concentration which gives you the resistivity or conductivity of the layer will be decided by the dose. So it can range from 10 to the bar 12 toper centimeter square to 10 to 18 ions per centimeter square, but only one drawbackin ion implantation. What is that? It results in damage to the semiconductor, but its solution is also there. What is the solution?Annealing at elevated temperature is necessary to heal some or all of these damages. So that is why ion implantation is followed by annealing. Because during implantation some minor damages will be created and those damages will be removed by annealing technique which is solid phase epitaxy.

So during the implantation process because of the damage, the material may be amorphous in nature and how do we know it just after implantation? If you go for the measurement of the sheet resistor, you cannot measure because it is amorphous in nature. But after annealing it will be recrystallized, so easily you can get the single crystal layer and then you can measure the sheet

resistor by 4 point resistivity method. So that isone of the reason just implantation. If you go for measurement of sheet resistor by 4 point resistivity method you cannot measure it.

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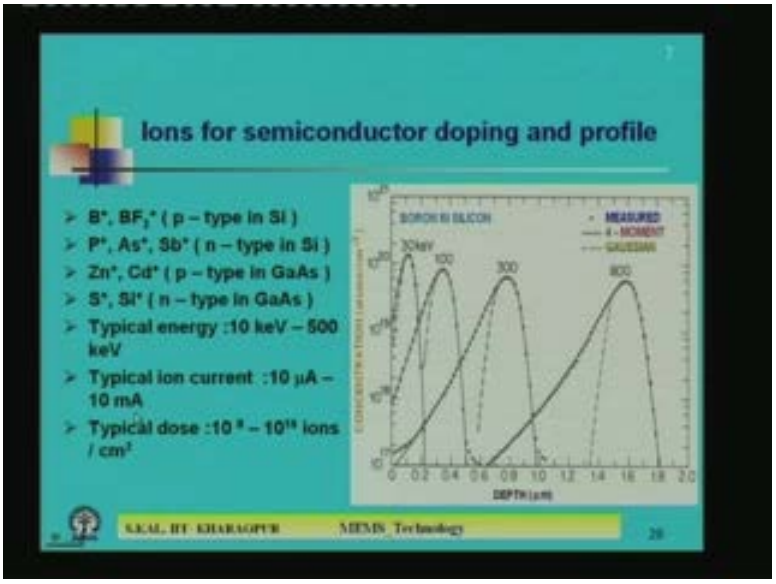

Sowhat are the differentof the ions used in case of ion implantation these are shown here? In case of P type dopant in silicon we use the boron or BF 2 ion. For N type in silicon we use phosphorous or silicon antimony ions. In case of gallium arsenide for P type dopant we use zinc and cadmium, gallium arsenide N type we use silicon and sulphur. Typical energy in ion implantation is 10 keV to 500 keV, typical ion current we use 10 microampere to 10 milliampere. This is the ion current typical dose we use 10 to the bar 11 to 10 to the bar 16 ions per centimeter square and this particular picture shows that how the profile changes for different implantation energy. You can see here30 keV,100 keV,300 keVand 800 keV boron is implanted into silicon.

So if you use 30 keV your profile is looks like this,100 keV profile looks like this,300 keV profile looks like this. So that means if you want 300 keV, so from the surface also you will not get the impurity atom. Here also you know you are not getting. So in the middle of the wafer you will get profile like that. If you want the Gaussian profile at a particular depth of the silicon, then go for 100 keV, there you will get the profile like this. So that meanssubsequent implantation if you go so then you can get a profile like this. It will comeif you combine all these things something like that. So that means by controlling energy and dose you can have any arbitrary profile in case of ion implantation which is not at all possible in normal diffusion techniques.

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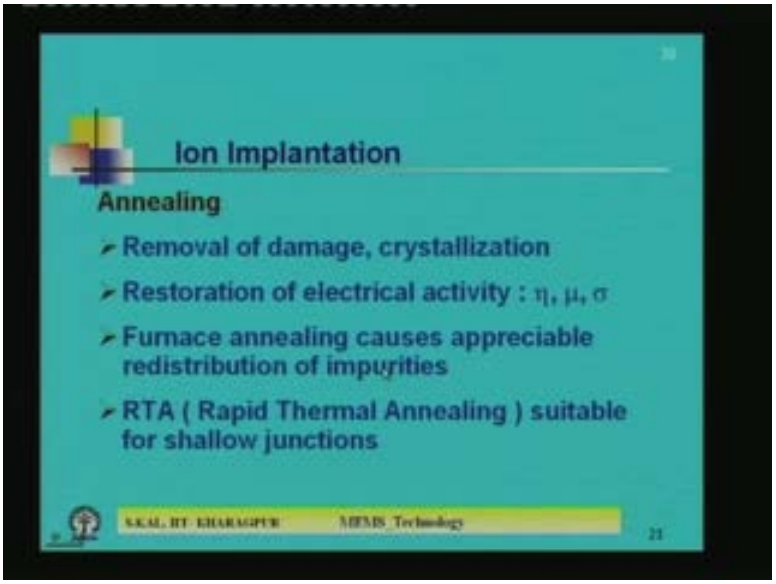

Sothe annealing is must, in case of ion implantation for removal damage and for re-crystallization as I mentioned. Restoration of electrical activity because you mu, sigma, eta all will be restore after annealing. Then furnace annealing causes appreciable redistribution of impurity, so people prefer for RTA which is a rapid thermal annealing and it is suitable for shallow junction. Two kinds of annealings are there; one is furnace annealing another is rapid thermal annealing. So furnace annealing cause again redistribution of impurities. But it you use RTA, it means high temperature very small time, may be 1 minute, may be 45 seconds. You can use for annealing at high temperature say 800 or 900 or 1000 degree. So that will the heal of all damage and again it will re crystallize and that is the prefer ion implantation followed by rapid thermal annealing.

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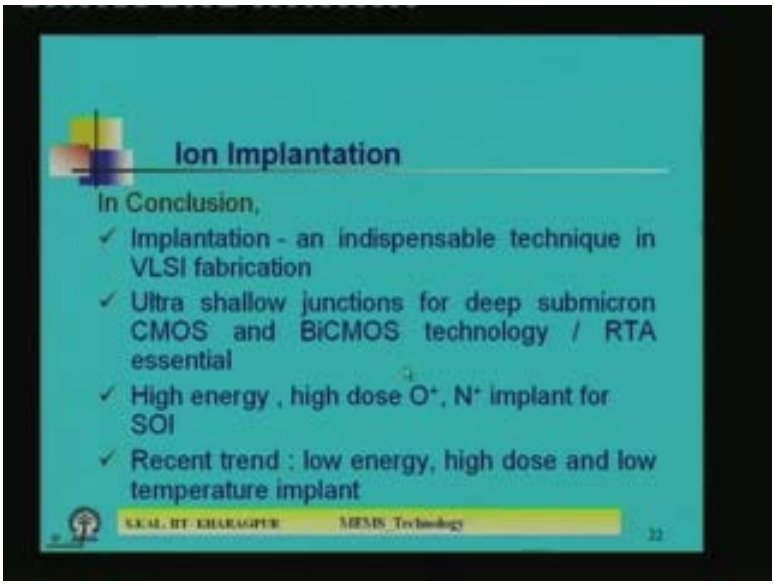

Now in conclusion of ion implantation we can say, implantation is an indispensable technique in VLSI fabrication. Ultra shallow junctions for deep submicron CMOS and BICMOS technology RTA is essential. High energy high dose oxygen nitrogen implants are required for SOI fabrication. Recent trend is low energy high dose and low temperature implant for the submicron VLSI ICC. Let us stop here today. So next class we WILL start micromachining of silicon and first step is the etching of silicon. We will discuss in the next lecture. Thank you.