Probability & Random Variables
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Lecture No. # 26
MEMS Capacitive Accelerometer Process

Last lecture I was discussing on a case study on the MEMS sensor. That is MEMS capacitive accelerometer. Some specification we define and from there how the specifications are achieved, we discussed on that. Two methods followed; one is analytical treatment and the other is the simulation using standard simulation tools and we compared the results. I remember I also discussed various structures of the capacitive accelerometers which are bridge type. Some are the cantilever flexure types. So out of that we found a particular structure which is double cantilever beam structure is quite sensitive and without much difficultly of technology and with that we achieved our goal by certain simulation, certain parameter variation and after satisfying those parameters, our next step will be how to go ahead for fabrication of those devices and basically the structures contain three pieces and how the three individual three pieces are fabricated and then how their assemble, that I will discuss today.

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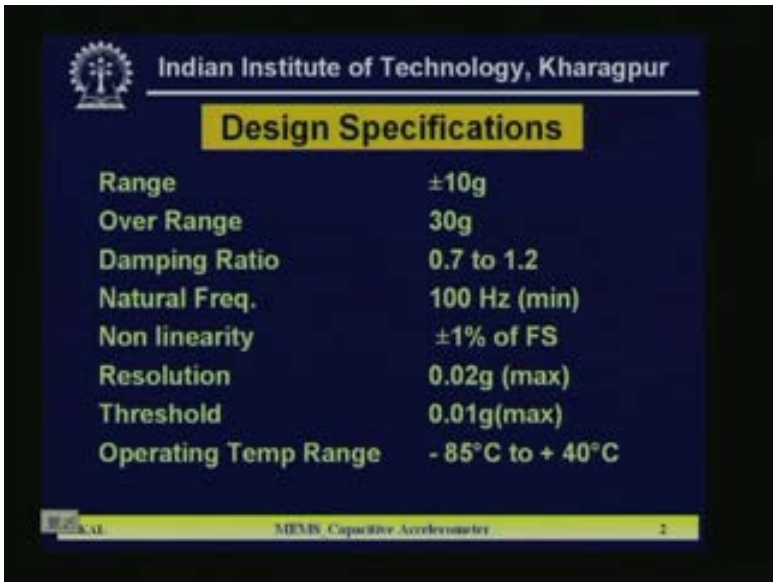

The design specifications which I mentioned in my last lecture are range 10 by minus plus minus 10g, over range 30g, damping ratio 0.7 to 1.2, natural frequency 100 hertz, non-linearity plus minus 1 plus 1 percent full scale. A resolution 0.02g, threshold is 0.01g, operating temperature range minus 85 plus 40 degree centigrade.

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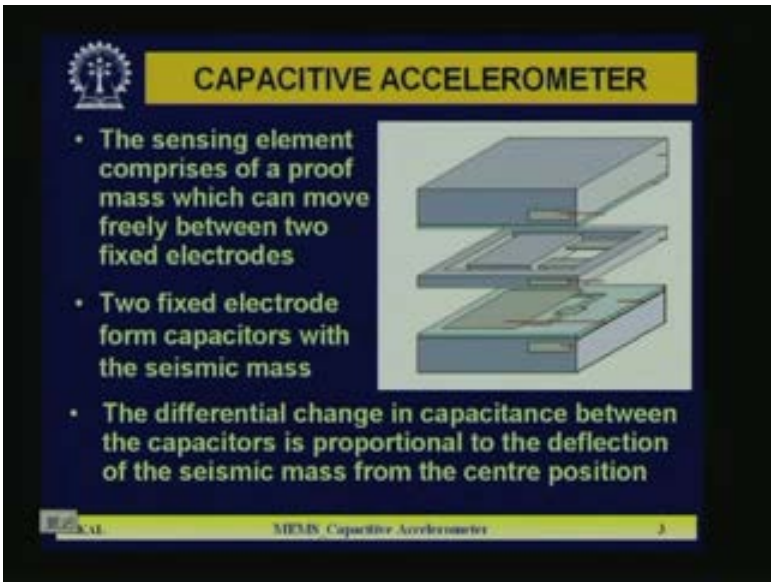

So with that we confine to the structure which is shown here 3 pieces. Middle piece is basically a the sensor and the top and bottoms are two fixed electrodes which formed parallel plate capacitance with the central piece and the central is comprising of proof mass which can move freely between the electrodes and accordingly the capacitance between top fix place in middle, the sensing electrode and that with the bottom fixed electrodes will vary and we are going to measure the differential changes of capacitance of this particular structure and as we used a proof mass and the proof mass will displace according to the acceleration and as a result of which the gap between two plates will change and capacitance variation will be detected and which is measure of the acceleration. That was the basic principle which I discussed in my last lecture.

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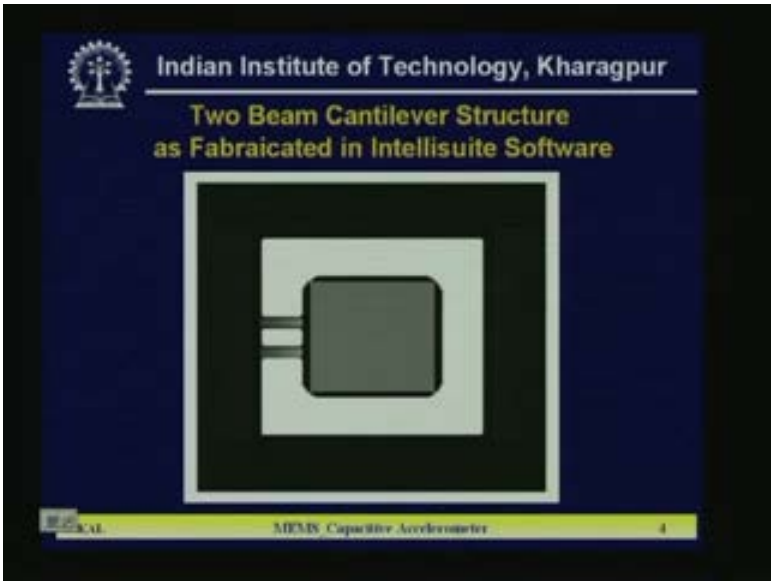

Now here the whole thing whole sensing element is the middle piece of silicon. That is two cantilever beam structure which we will confine in to that, one here, another is here and this middle one is proof mass and this structure is to be fabricated using micromachining technology and before that within using some standard, the process simulator which is intellisuite software which is micromachining, if you do it and it will show you after micromachining how the shaped looks like. So there how much will be the under card, how much will be the corner compensation, that we can get some ideas which are not 100 percent practical figure. After getting etched, but some idea we can have from this simulated tools, how it looks like after certain process. So we are going to have similar structure which is shown in the figure. Now here one thing is a different from earlier flexural cantilevers which I stressed in my last lecture also.

That is we found that this thing, this kind of structure is much more sensitive. If you make the flexure at the middle of the thickness of the proof mass, remember the flexure is not at the top surface. Is just of the middle of middle around the thickness of the vertical direction of the proof mass. There we found the sensitivity will improve drastically and there the performance will be also improved. So now the question is how to get the flexure or cantilever at the middle of the vertical dimensional of that means middle of thickness of the proof mass. So that is one difference which is a difference from the piezoresistive, the accelerometer which I discussed in 2, 3 lectures back. So there our problem was that we fabricated the piezoresistance at a surface of silicon. Because the sensing element where in that case is a resistances which has to be at the surface because this stress was maximum at the surface.

But in this particular case we are not going to fabricate the piezoresistances. Rather here sensing mechanism is capacitance variation. So the flexure you have design such that the displacement of the plate will be maximum. Plate means here the proof mass. Proof mass has got certain area and that proof mass displacement with acceleration from the top of and bottom fixed electrode should be as maximum as possible. Since there is no passive element we are not going to fabricate on the structure. That is either resistance or some other may be active device we are not going to fabricate. So there the problem does not arise if we make the flexure. Just at the center of the thickness of proof mass. So here our main objective is the displacement. Maximum displacement how can you get it? That we have found if you make it at the center, simulation results also tells us that then it will displace which is more, as results of which obviously the capacitance change will be more.

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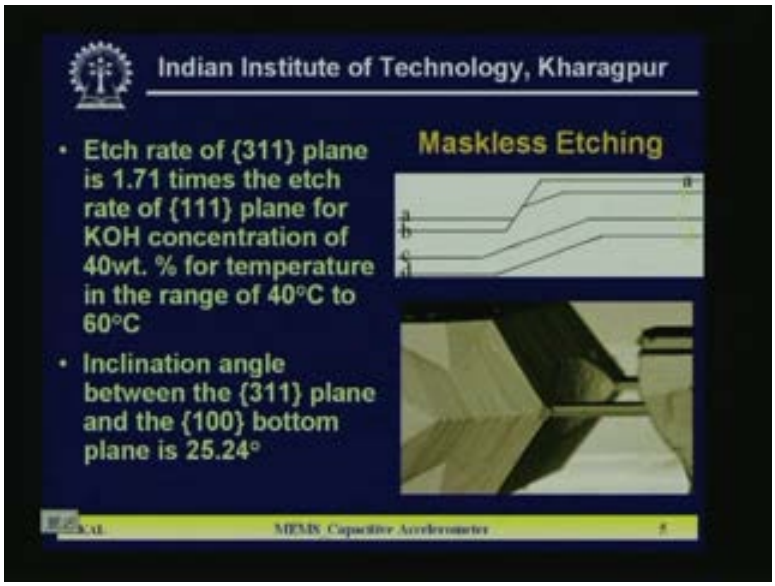

So that how can you get it? So that little bit I discussed again I am telling you. So we will go for the preferential etching technique which is the anisotropic crystallographic plane dependent anisotropic etching and we are going to use here KOH which is the standard silicon etching. So there we know the etch rate of silicon in different crystallographic directions are different 1 0 0, 1 1 1 and 3 1 1, the 3 planes are involved in this particular structure. So here we have seen the etch rate of 3 1 1 plane is 1.71 times the etch rate of 1 1 1 plane for KOH concentration 40 weight percent at temperature in of 40 degree C to 60 degree C. So that is the normal temperature we are going to use. Now since there is preferential etching between 3 1 1 to 1 1 1, so which are involved in making the structure in the central plane, because you can see here, there are different surfaces. One is the slant surface, one is a vertical surface, which is 1 0 0 and another you are getting some surface like this here.

So these 3 surfaces we need the etch rate should be in certain direction should be maximum. In other directions some variation will be there so that we want etching in a 3 1 1 plane after sometime, not in 1 1 1 plane. So that is achieved in KOH silicon, some differential is there and the inclination angle in 3 1 1 with 1 0 0 is 25.24 degree, so that is the thing. So initially what you can do here? So you can have some oxide masking at the flexure, than go for etching. So after certain amount of etching is done, then you can remove the oxide and just simply you dip the whole thing in to the KOH etching solution. So it will follow the preferential crystallographic dependent etching and you can get the structure. That means you can say in that direction it is a mask less etching. Some kind of the mask less etching is also relevant in this particular fabrication safe.

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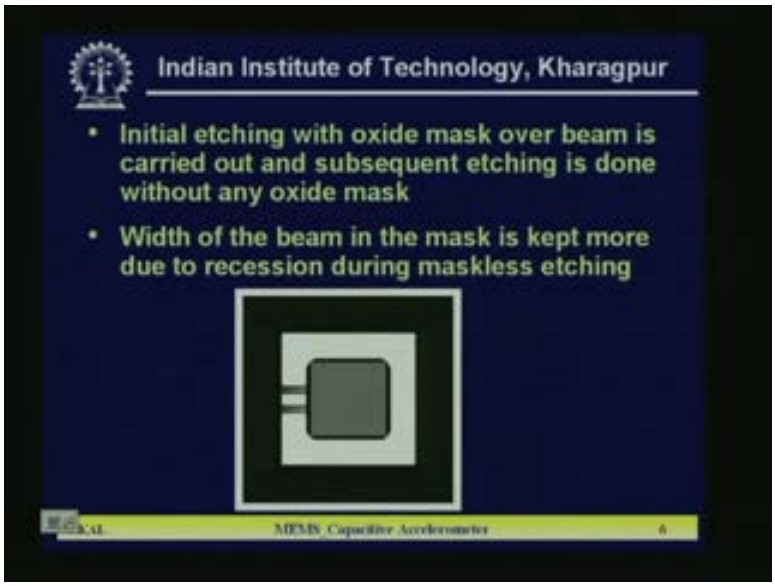

So that is normally followed. Initial etching with oxide mask over beam is carried out and subsequent etching is done without any oxide mask. Width of beam in the mask is kept more due to recession during mask less etching recession means it side all also little bit it will attack. So that is why the mask level, the size or width of the basically flexure beam is kept little bit more compared to the actual weight. So now let us see how the process will follow. What will be the actual process to get the structure which I have shown in the beginning, in the second slide I believe?

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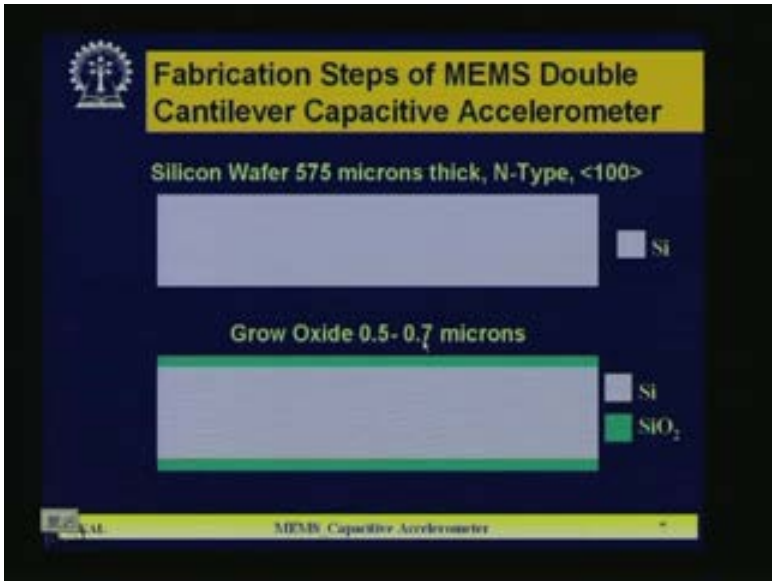

Now this thing is the fabrication step. Initially let us concentrate on the middle piece which is the sensing piece. How you can get it? So we have to start with the silicon wafer that is 575 microns, 520, a 500 plus minus. Some variation is there. So which wafer we have simulated, that is 525 to 75 micron thick n type 1 0 0. That is say wafer. Now if I see the color of the silicon is this, so then this is the silicon wafer, there silicon is cross section diagram I am showing. Now next what will you do? We are going for oxide growth. Masking oxide growth, that is 0.5 to 0.7 micron oxide, we have to grow on the both side of the silicon and it looks like this. So is top the greenish color and bottom greenish color are the oxide. So 0.5 to 0.7 micron thick oxide is grown at the beginning.

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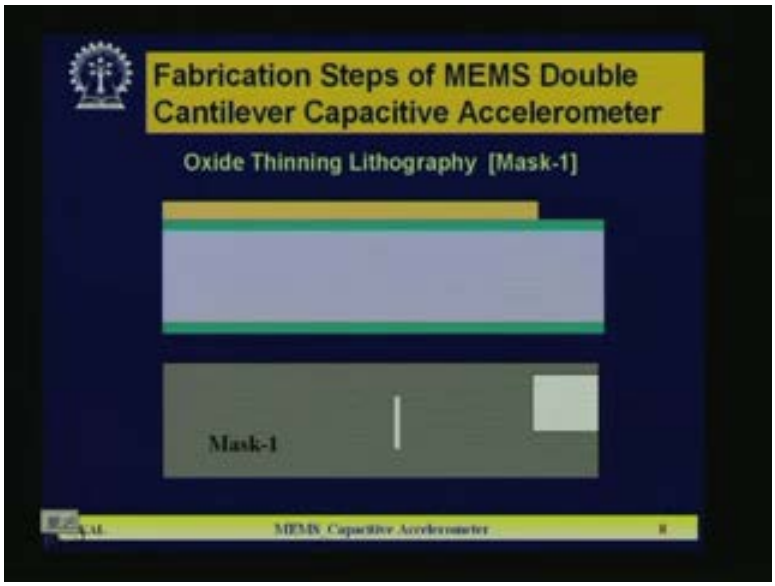

Now in the next, what is the next step? The oxide thinning lithography. That is the mask one. Oxide thinning lithography means we are not going to remove the oxide or not we are going to opening window in the oxide. So that is oxide thinning lithography. Using the mask one so this is the mask is shown at the bottom. So this portion, some window like structure is there. So lithography, this color is photoresist. So here this portion is here is a white portion in the mask. So automatically here there is no photoresist. No photoresist here and at the same time you can see here one slit type of thing is there. So this particular portion we have intentionally done here because you see we want when the middle piece will go up or go down, in that case so sticking problem is to be avoided. That is I mentioned sometimes back if you remember in surface micromachining, there is a problem is surface stiction. That is any kind of the membrane or the cantilever during the moment, maximum moment it can stick either in the top or bottom surface and there you get it fixed.

Now in order to here also if you see over ranger protection kind of thing, if the complete proof mass, the whole proof mass with jerk it goes down drastically. So it should not touch the bottom electrode. Because you see is a parallel plate capacitance, top is electrode and bottom electrode that makes short circuit. So it should not be there, so for that in the proof mass we can make certain narrow over small narrow hill type of thing, some protrude structure which will struck

there and then it may prevent breaking of the flexure also. As well as that if that protrude is not metalized, so then automatically that short circuits between the middle plane and the bottom plane or either top plane will not be there. So for that we are, in all the mask we have made some slip kind of thing here and accordingly there we will deposit something or we will made certain structure which will not disturb the proof mass are struck with the either top or bottom.

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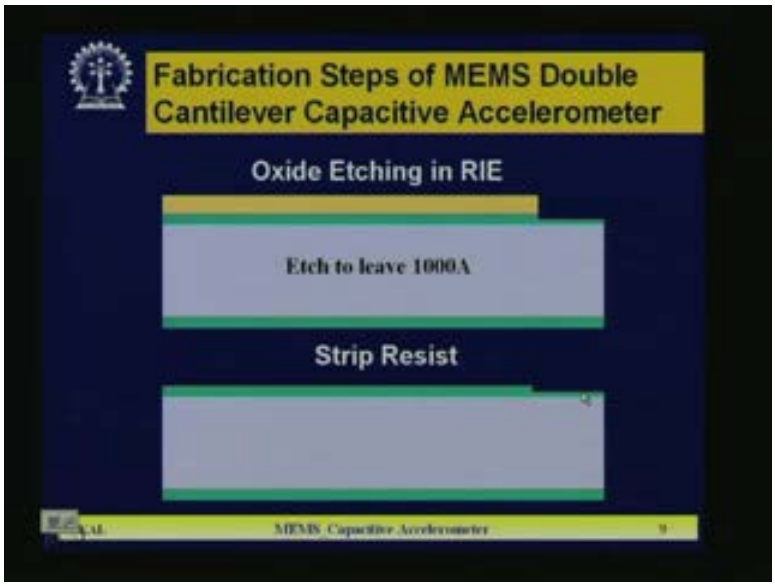

Now next is the oxide etching RIE and this is the thinning. I told you the thinning layer, thinning kind of thing oxide masking. So etch to leave 1000 angstrom only. So here only 1000 angstrom will be there and initially I think it was nearly 0.5 to 0.7 micron we took it, so out of that rest of the portion is etched. Only this portion is left in this region. Now this strips the photoresist, so this color is removed. That means photoresist has been removed. If it is a positive easily you can remove it by acetone, warm acetone or if it is a negative resist, then you can go for the 1 is to 1 is to H_2SO_4 boiling or you can use the photo resist remover and which is used at the little bit higher temperature, more than room temperature may be 70 degree or 80 degree C. So you remove the strip and then mean photoresists you the strip resist, then you will get will structure like that. So here oxide thickness is less here oxide thickness is more.

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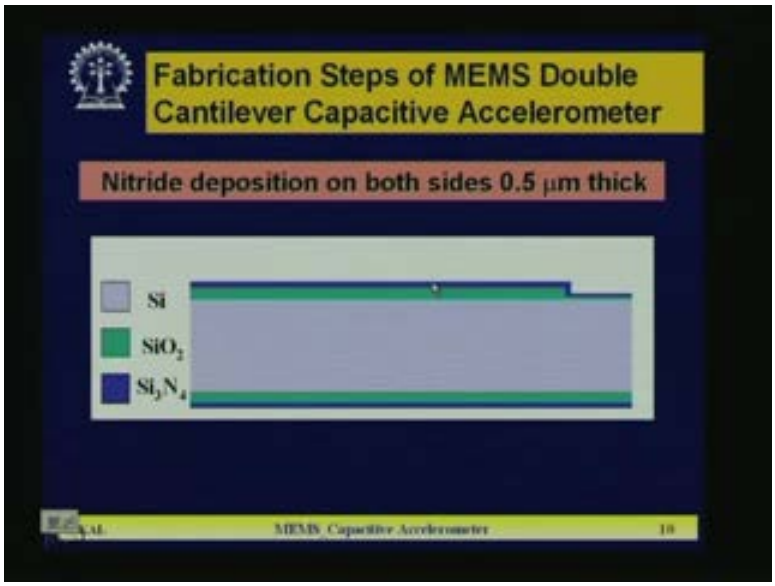

Next step is so here now we go for deposition of silicon nitride on both side of thickness 0.5 micrometer. So this is silicon, the green color silicon dioxide, here we have thin down. Now silicon nitride which is bluish color on top and the bottom in a both a places we have to get silicon nitride and that you can only get by deposition technique and that deposition technique may be either your CVD or you can go for spotter deposition. So you deposit nitride top and bottom both sides.

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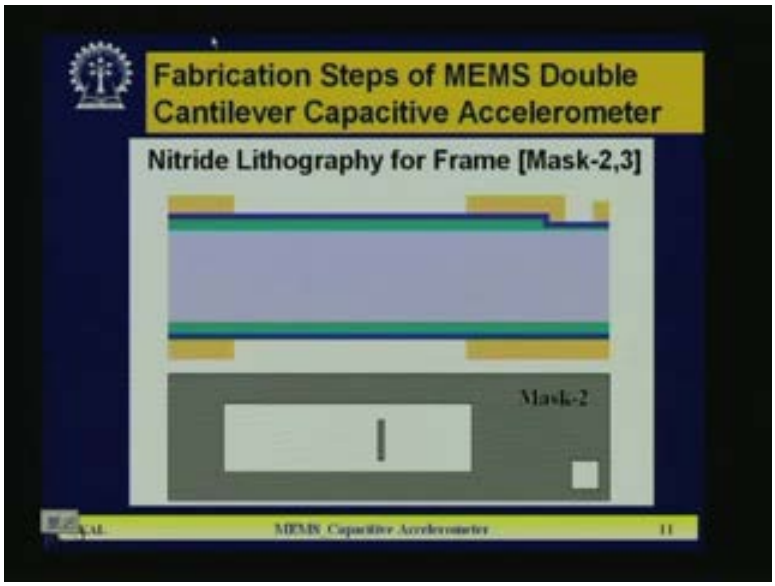

Next is nitride lithography for frame. Because the middle structure if you remember 2 flexures are there proof mass is there at the middle and surrounding there is a frame. So now we have to

define the frame and for that we need lithography and that lithography is shown here and mask 2 is also shown at the bottom. So that means here we normally we coat photoresist, then using this mask then we get removed photoresist from top and bottom certain portion. So there after that we are going to etch nitride and will further process and the frame will be defined. This portion and this portion, this region and this region away from frame and here you can see in the left side some structure we are going to create. That is basically at the end you will find that is done only for taking contact. Now in this kind of structure where 3 pieces are used one bottom top electrode fix, bottom electrode fix, top electrode fix and the middle. So you have to take contact parallel plate capacitance means the top electrode the bottom side will be one plate and middle electrode you have take contact and the bottom electrode top surface of that plane you have a take a contact. So taking contact from those pieces in case of capacitive accelerometer is not so simple. So that we will see how those contacts are taken. So at the end of this process technology step, I will just explain how it is being done. So now this nitride lithography in this particular step.

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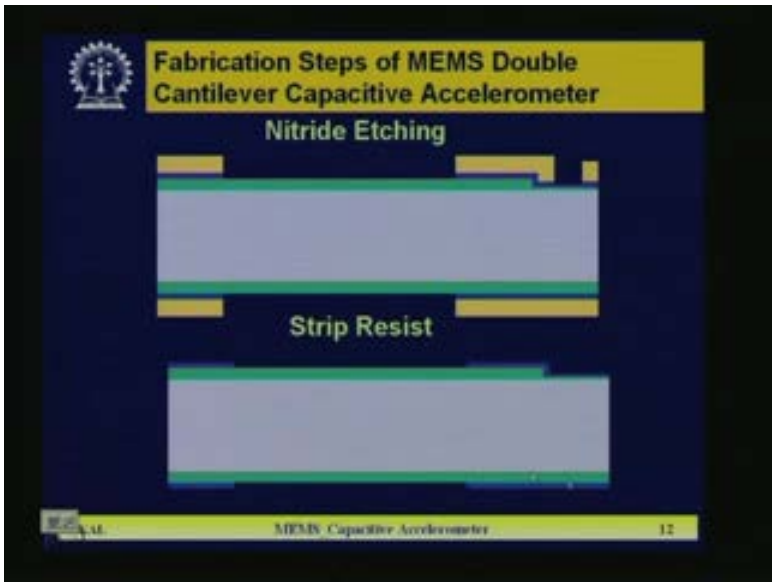

We can go for the nitride etching. So in the last slide it was just lithography pattern. Then nitride the blue color has been etched. You see from top and from bottom also blue color thing has been etched. Now after photoresist removal stripping photoresist, so this photoresist is removed, this color is not there. So only here the blue color nitride is also gone. So the wafer looks like that only oxide is there. Now keeping nitride as masking material we can remove the oxide and then subsequently go for etching of silicon. So since nitride, now you will act as a masking layer for removing the oxide.

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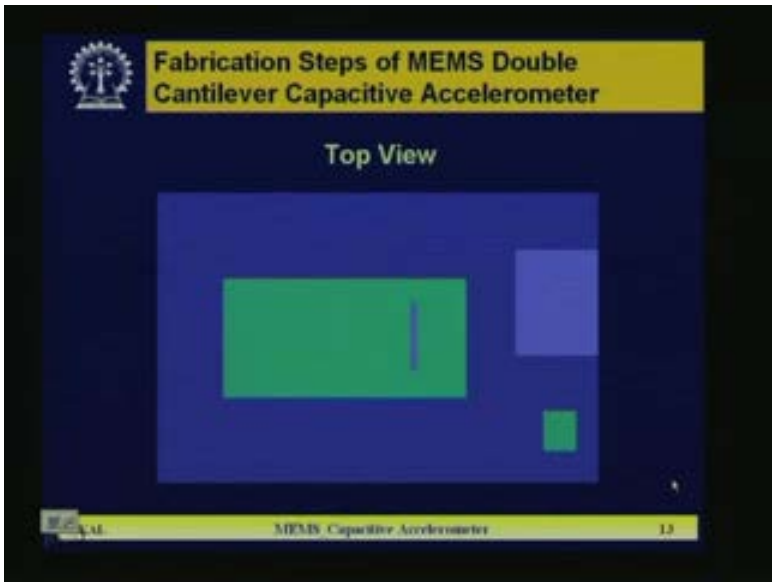

Now that next is the top view of the mask looks like that. It is also shown because you can see here in the slit always maintaining. This are other pictures are cross section view. This is a top view how mask looks like this. Now the oxide patterning for flexure.

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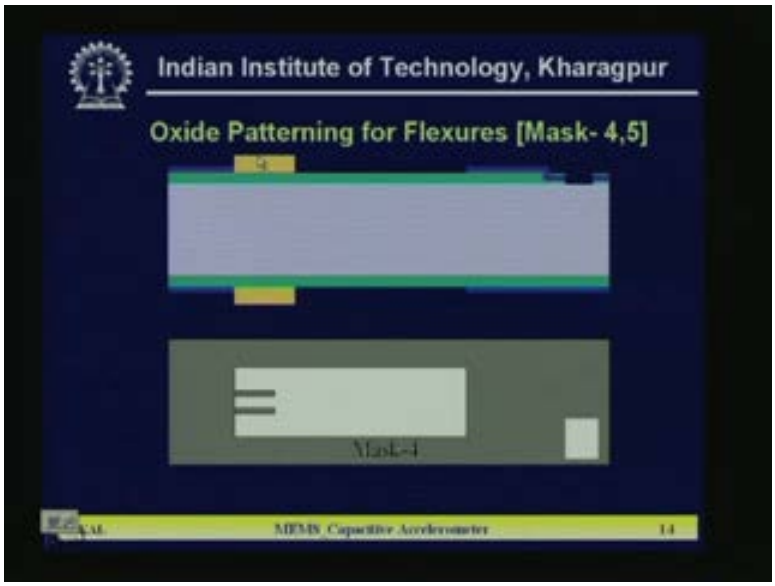

So this is the mask 4 here and I have to pattern oxide for the flexure, flexure is here. So since it is a cross section you can see only this color into these two region top and bottom and top view with photoresist is not seen. That picture will clear how it looks like at the top surface. We are taking in one of the flexure side the cross section. Now you see here we have not started removing this oxide and etching may be in the next step we will go for that oxide etching.

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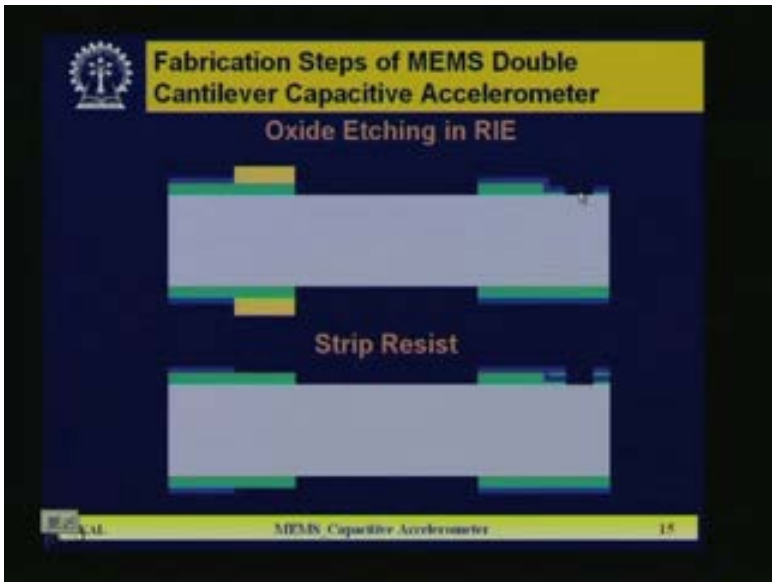

Now in next step is oxide etching in RIE. Now after flexure definition then will go for oxide etching a flexure has been covered here. Then oxide is removed here by RIE technique and than will strip the photoresist. So here photoresist has been removed and oxide is covering here and here is bear silicon. Here in particular step RIE oxide removing. Because oxide etching, you can see the photoresist is covered that normal etch oxide etching is buffered hydrofluoric acid. But here buffered hydrofluoric acid basically it takes in a lateral side also it is isotropic etch. So if I need the anisotropic then we have to go for the plasma etching or reactive ion etching. That is an isotropic is removed. An isotropic structure you can get it and there even oxide will not be oxide will be protected. It can act as a masking layer also there so the oxide in the so portion is removed as well as this hole also here it is also you see can oxide has been removed. So nitride cover, there is nitride cover here in photoresist. Now after removing the oxide if photoresist is stripped. If you strip the photoresist, then it looks like this. Here is direct silicon, this portion direct silicon and from bottom also this place direct silicon 3 places direct silicon is available.

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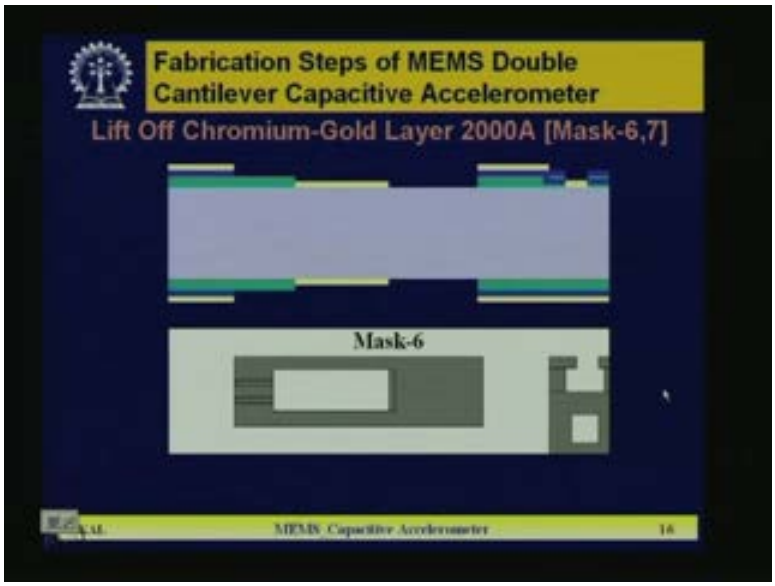

Now the lift of chromium gold layer 200 angstrom. So now still we are not started etching silicon. So we are going to protect some portion of the silicon by Chromium Gold also. Now you see here the Golden color is chromium Gold. So here the mask is here shown like then using the lift off technique, we deposited Gold in selective places. You can see which is also shown in yellowish color. This portion and this portion here and in the left side also above of the nitride, above the silicon and here also in bottom side also, just above nitride it is also deposited. So that is the chromium Gold, the chromium purpose you now it is for good addition of the Gold film with either nitride or oxide or silicon chromium is used and very thin layer may be say 300 to 500 angstrom unit and then you can have Gold layer of 2000 angstrom. Then using the mask number 6 you can go for the lift off pattern.

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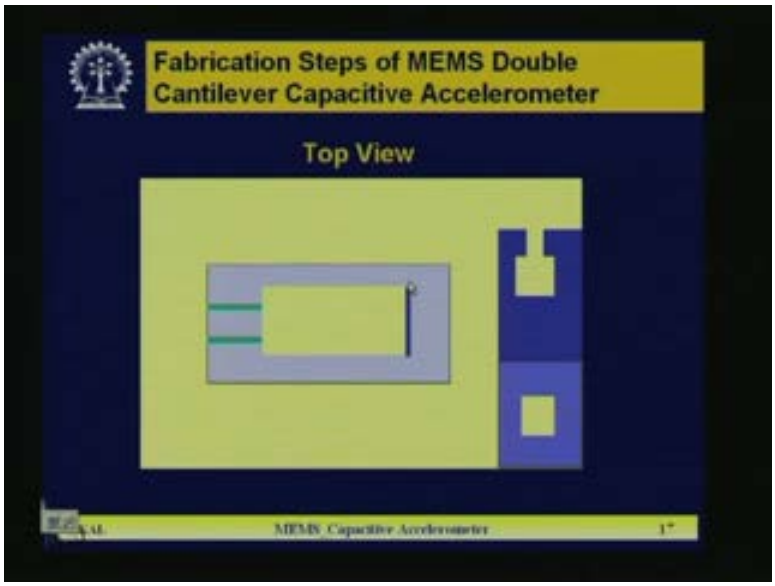

Now the top view of the structure looks like this. We have taken some cross section view in earlier diagram. So if you see on the top, with oxide, nitride and chromium Gold, this structure looks like that. So is a golden color is a yellowish color is Gold and the bluish is color is nitride, a bluish color is what, the bluish color is a nitride and greenish color is oxide, here is oxide and bear thing is silicon. So which you saw here in the cross section structure if you see from the top then it looks like that. So now if you go for etching, then only this portion it will be etched and in the central place you can see is basically proof mass and I have shown you in some of the mask. This strip, this a strip, bluish color strip is here which will protect the proof mass against the damage and this is the top view after that step.

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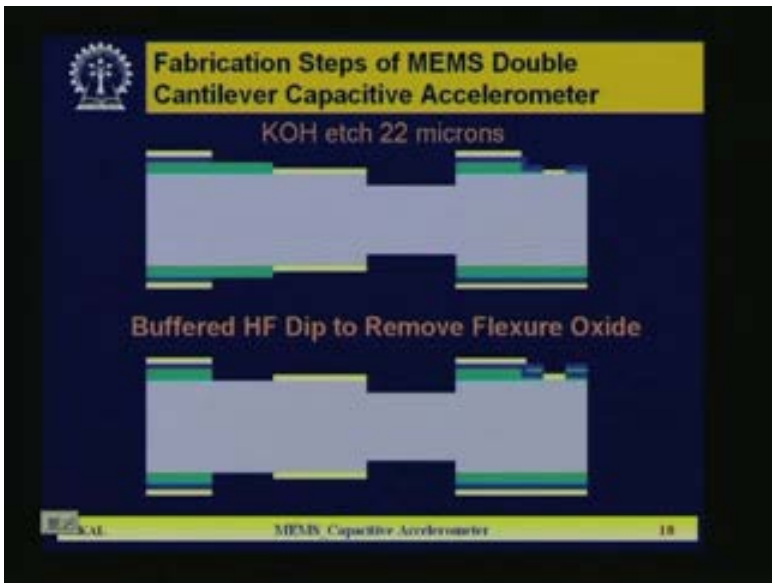

Now we go for KOH etching. So for KOH etching again I am coming to cross sectional diagram. So 22 micron KOH has been etched from this portion and this portion its not top view cross section that is why I am showing this portion. Now you can see here the passivation has been made in some of the region by chromium Gold, some of the region by the oxide here and accordingly you are getting at the surface different steps. So that means from here height is different, from there again this place is chromium Gold, from here again 22 micron delineation is there, from top and bottom and then here also it is just covered with chromium Gold because you stops etching in the portion also. Now in the next step is a buffered hydrofluoric dip to remove flexure oxide. Because you can see here as this stop here this, a flexure oxide in this portion. Now initially keeping that you went for diagnosis etching than at the end you are going for a removal of the flexure oxide. Then it will be mask less etching in that part that I mentioned at the beginning. So that means now buffered hydrofluoric acid dip to remove flexure oxide. So flexure oxide here and here it is removed. But here it is protected by gold, bottom also protected by Gold, and here automatically silicon is there. So now you can see, now you are getting the surface of the silicon sub portion silicon thickness is less in this portion here and in some portion the silicone thickness is more. So you can somewhere if you etch from top and bottom it will make through hole in somewhere you will get the flexure.

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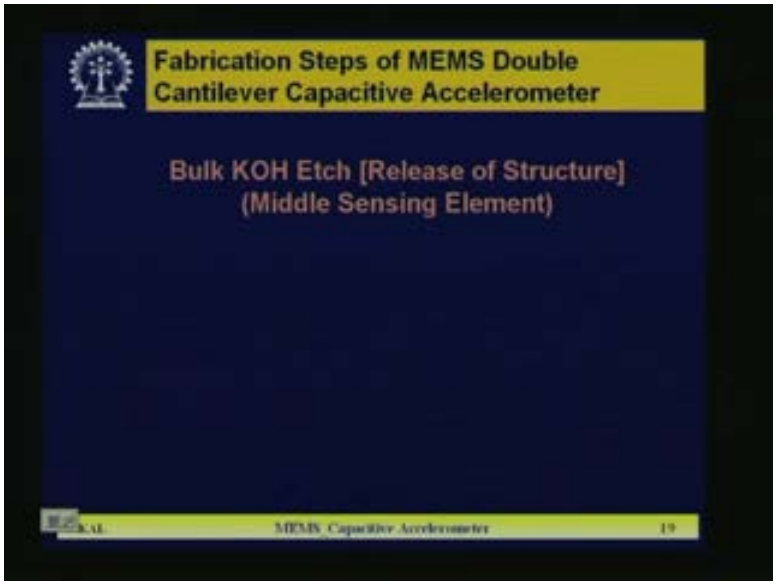

Now next is bulk KOH etch and release of the structure.

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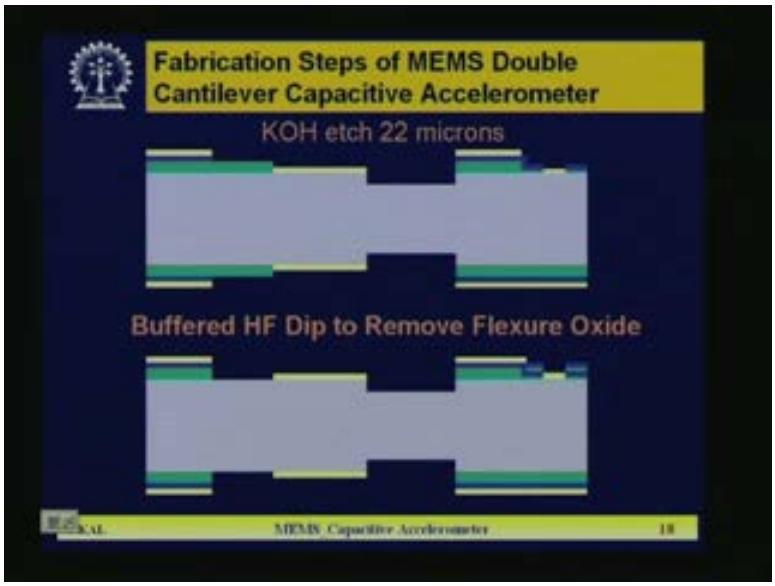

So because here you bulk etching now starting initially I just removed some portion because you have seen that some portion it has to be through hole. So that total proof mass will be hanging, supporting with the flexures and in flexure also from top and bottom it will etch and at the middle it will stop somewhere.

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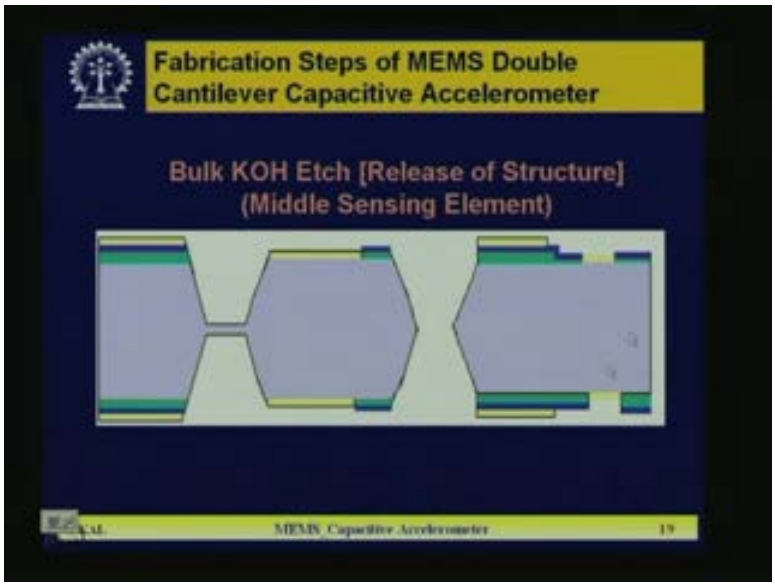

So that is why the bulk etching has been done now. And with that bulk etching the cross section diagram looks like that. Here you can see the, because in this portion initially we have removed 22 microns. That means this 22 micron thickness will be left here. So now it is KOH, it is etching from top and bottom here top and bottom thorough etching will be there. But since here earlier

we have made 22 micron more. So automatically in this portion you will get 22 micron thickness of the flexure. So this is the proof mass is also protected and there you can see is a here little bit the strip kind of thing which we made in mask. Here some deposition of nitride will be there which is basically insulated and if it touches in the top and bottom, so will not short circuit the thing. So it will struck in that particular deposited you can say the crest height is more here compare to this place. So now this is the structure, after that you can go for next step is a top electrode.

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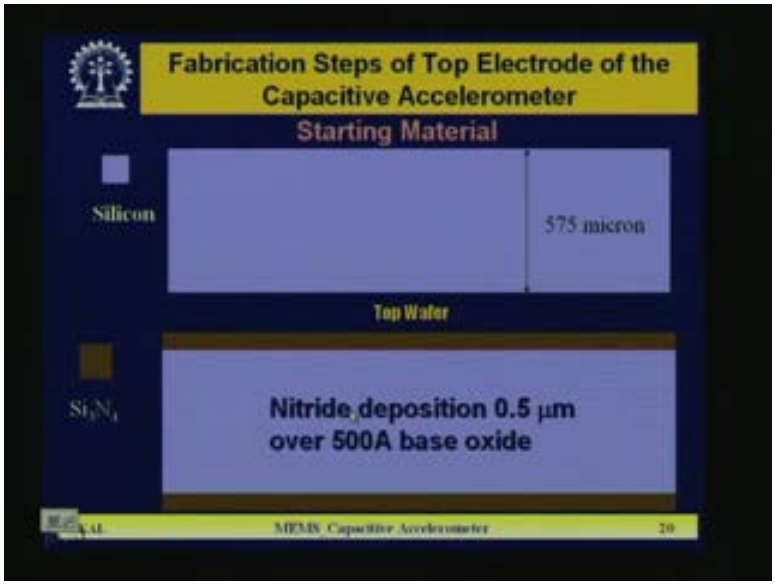

So middle is already been fabricated. Now you go for the top electrode. How the top electrode again we start from silicon wafer which is 575 micron thick and bear wafer, then we go for nitride deposition. You can see here the contrast over the blue is not clearly seen. It seems so it is some brownish color is deposition on the top and bottom. So that is silicon nitride. We did not go for silicon dioxide. But here the both top and bottom silicon nitride is deposited. Now that is of 0.5 micrometer over 500 angstrom base oxide. So always when on bear silicon if we deposit some nitrite we have to be cautious. First some base of pad oxide is formed then we deposit silicon there is certain reason because if you directly deposit silicon nitride bear silicon then the white ribbon effect will take place. So that means nitride stain on this surface. Later on if you want to remove those nitride to get the bear silicon you will not get it. So that is the problem and not only that interfaces of the silicon and nitride will be damaged, in order to prevent silicon underneath the dielectric intact. So initially some pad oxide of thickness of say 200 angstrom or maybe up to 500 angstrom it is grown from silicon then you deposit nitride. Whenever if you want to make the complete removal of the passivating layer of nitride, you first etch nitride then this 500 angstrom or 200 angstrom oxide also can be removed easily. So that is a preventive layer between silicon nitride and silicon is made to protect silicon intact below the dielectric film. So now that is why a base oxide or pad oxides are 500 angstrom on TOP 0.5 micron silicon nitride is deposited.

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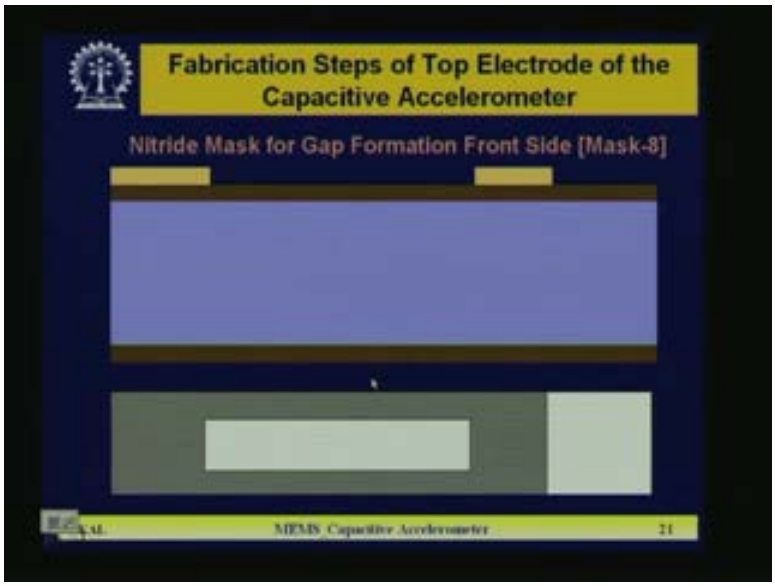

So next step is nitride mask for gap formation front side. From the front side nitride is masked. Backside we have protected and for masking just we went for some lithography and then the windows are open from this portion and this portion and in the next step the mask looks like here is shown. Here is a big rectangle at the middle and in this side a complete square structure. This the whole area of a particular capacitive accelerometer. So after nitride masking the wafer looks like is a mask number 8 wafer looks like this.

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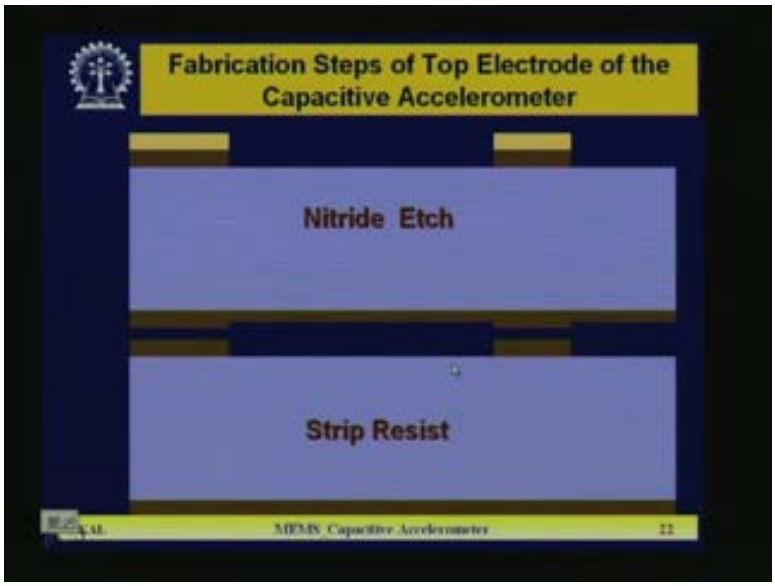

Then is nitride etches that is from this portion and in the extreme rights portion, nitride has been etched and so the structure looks like this. Next is after can you see there the nitride contrast

color it is very difficult. It is a blue on top of the brown. So it is almost mix colors I should have changed. Anyway so the nitride from the top a because this portion is photoresist you can see from there nitride has been removed and then you can go for the stripping of photoresist. So the photoresist has been removed from this point and this point and you are getting windows in the nitride, in this region and then you have to go for the next is nitride mask backside for slit formation.

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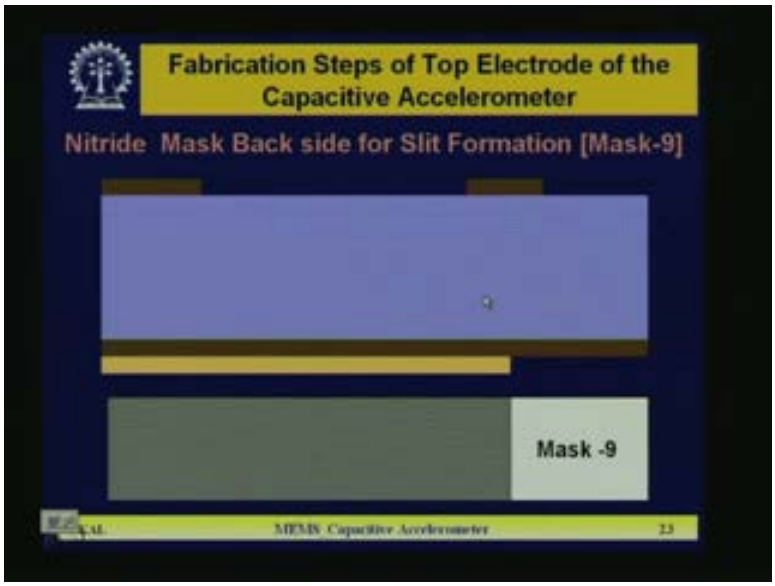

Mask number 9. Here also after you after patterning the front side of the top electrode now backside lithography are being made. So that here some portion is to be removed and then mask of this particular mask number 9 looks like that. This is a mask number 9. So in this portion photoresist is not there. So nitride easily you can etch, so now then because in the next step if you remove the nitride so you can go for the silicon etching from top and bottom. So here if top and bottom means is through you can complete remove it and here some delineation will be there. So for top electrode which will be another fixed electrode and then you can see how it looks like in the next slide.

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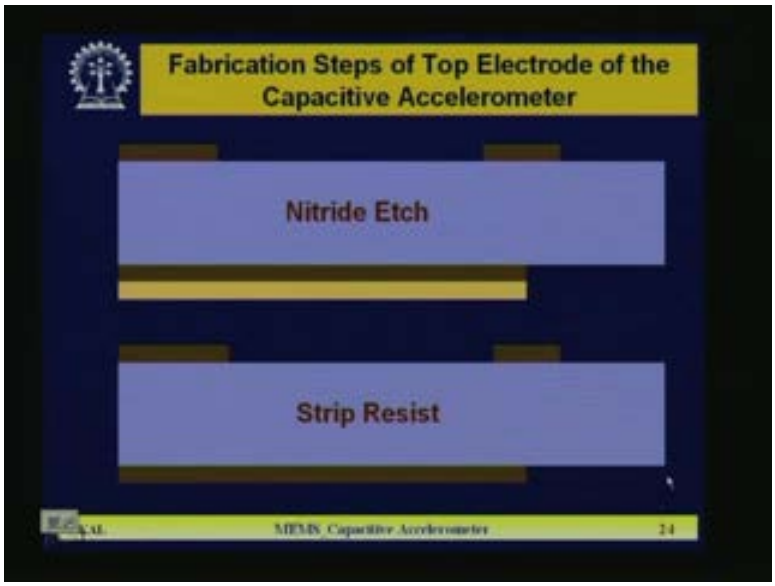

So now here also the nitride is removed and nitride etches then strip resist. So resist is removed from their bottom, so then you are getting the structure which looks like this. So that means 3 places if you see the bottom wafer, from the top only certain portion the oxide can be removed. Silicon can be etched and in the extreme right portion either from the top and the from the bottom both side it will etch. So it will be completely removed. So that you can get opening for your contact formation.

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Now next is KOH etching front side with backside protection it looks like that. So you protect backside and front side you go for KOH etching. So its opening is from this side and this portion

and this portion. So you etch here and here then go for the KOH etch backside with front side protection. So initially KOH front side with backside protection and then next is KOH etch backside with front side protection. So ultimately the structure looks like this.

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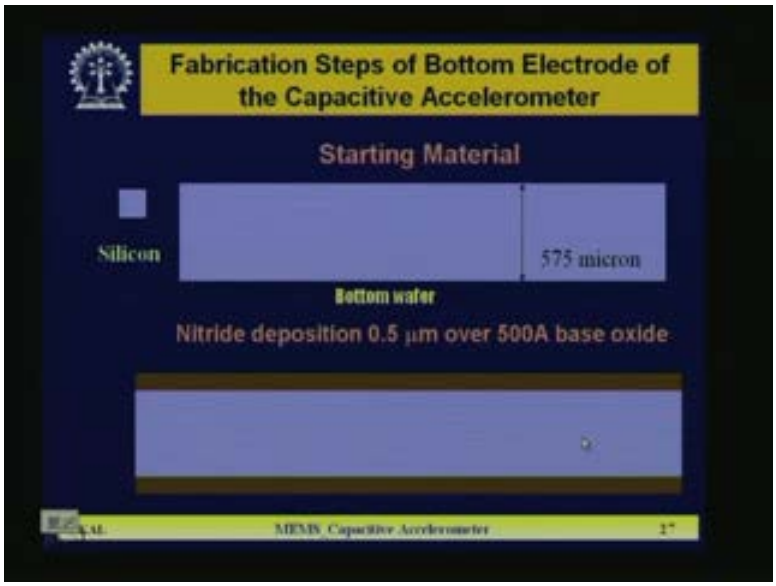

So with that next step is your deposition of the nitride. After the KOH has been etched completely you remove nitride. So because purpose of nitride is over if you remove KOH. Now then you deposit the chromium Gold by evaporation. That we called is a global. Global means the full surface we are not going to pattern. So that means this is the top electrode. Now when you are going to assemble we invert it. By inverting we will place it and then we will bond it. So top the electrode formation is over, now we will go for bottom electrode.

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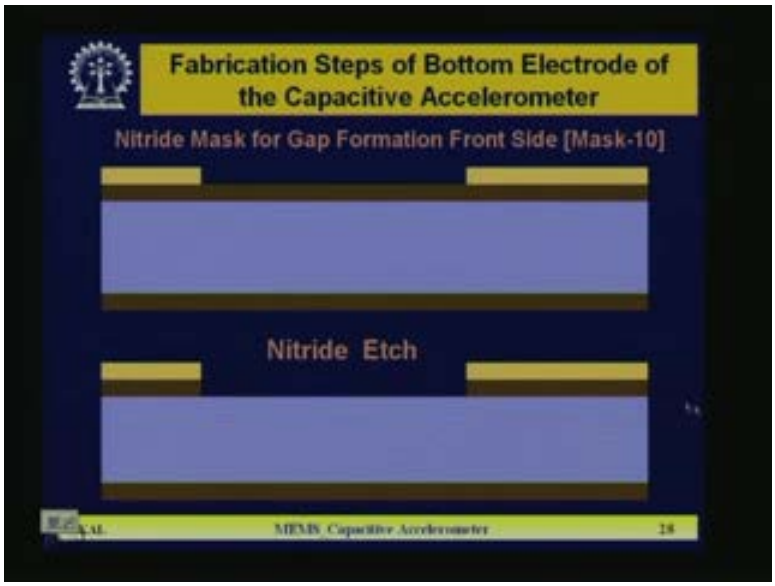

This is a fabrication steps of bottom electrode of the capacitive accelerometer. Initially we fabricate middle one which is the important sensing, then we make top one, now you we go for the bottom one. So bottom one is relatively easy compare to the top. Because in the top electrode you have seen in the some age has been completely removed and that removal is necessary in order to have contact from the middle piece, middle sensing piece. But in bottom electrode contact can be taken from the wafer itself if it is conducting wafer. So there you do not have to etch completely one side at the bottom electrode. You will understand if I show you the structure.

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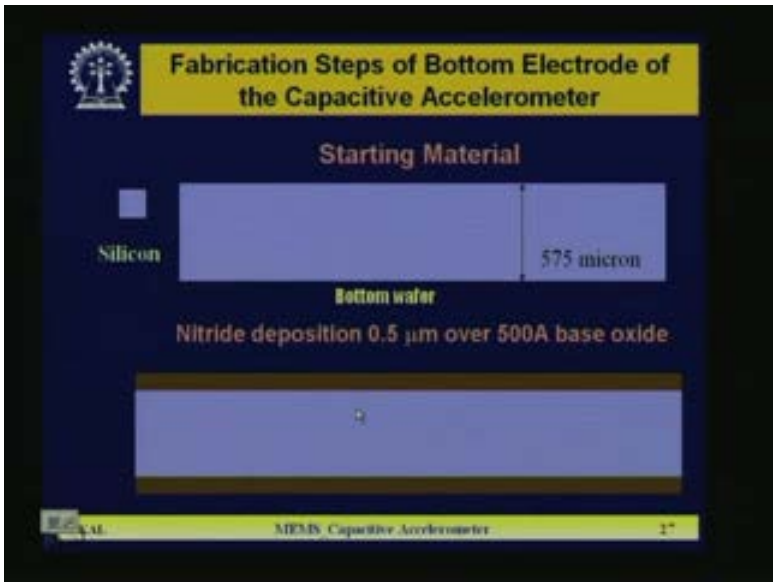

Here again the bottom wafer silicon 575 micron, silicon wafer is taken, then nitride deposition of 0.5 micron over 500 angstrom oxide in the same a step like the previous one.

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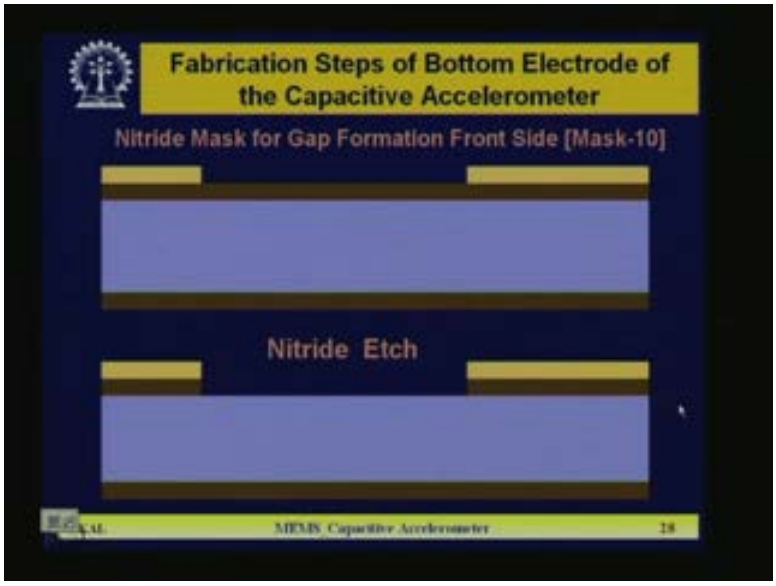

Then we will go for nitride mask. For gap formation from the front side like here. Then we go for nitrides etch. So if you etch nitride from this portion and this portion it has been etched, so this is protected.

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Now in the next step you will get photoresist removed and the nitride looks like that. KOH etch front side with backside protection. So it is in earlier case you in the top electrode from bottom

also pattern and you etched little bit. But now in the bottom wafer bottom electrode we etch only the front KOH etch and backside is completely protect will be protected by silicon nitride. So now with that next is nitride etched front and back.

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When the silicon is etched, I mean group is a form. Then purpose of nitride is over. So if you remove nitride from front and bottom also and then again chromium gold evaporation global. So you deposit chromium Gold on the top of this bottom electrode, this is basically the metal plate because is parallel capacitance electrode plates has to be formed. That is the bottom electrode plate is here. So in the next phase we are going to assemble the structures. How can you do it?

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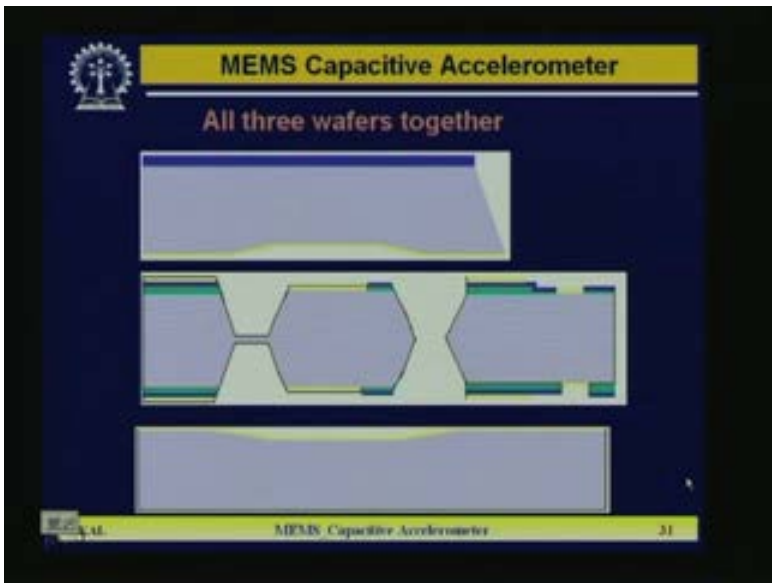

So now you can see what the three pieces are one by one. All the three wafers were brought together. These are the three pieces. So you have seen the bottom wafers. This potion was not removed in the top wafers it is removed and this is a cross sectional diagram basically. Now this is a middle one. So now here is that gold plated in the proof mass, here also Gold plated in the proof mass. So in the top also is a Gold plating is there. In the bottom also Gold plating is there. Now if we combine the 3 pieces, now this Gold and this Gold will be attached together and this gold and this gold will be attached. So that means if you make a, if this piece is a bottom one is basically the conducting wafer, so here you a make contact, if it is a contacting means is highly doping n type silicon wafer. If a you take it, so that middle piece contact is taken from here. Middle piece contact is taken here.

Now if you press this with that because you see in the top wafer the Gold line and the middle wafer Gold line is molded. So then this connection is coming up to this, you can take contact from this point. This point is a top electrode contact while connect. This portion you can see, this portion here one contact. So this is if you press here and here join together. So you join together here, so this will one contact and that will be top electrode contact. Bottom is this wafer itself. This is a highly conducting wafer. This wafer is silicon if it is a conducting wafer, so is a Gold plated here, so this you can take amount contact. So automatically you are getting contact of this and that means it is not disconnected. In frame somewhere it is connected so. But this portion and this portion over nitride and oxide is there insulated, similarly in the bottom also over insulation the Gold is there. This Gold is helps you proper bonding on bottom and middle wafer.

So then here is an electrode, so this electrode contact is again this wafer contact can be taken from the bottom piece. Because in the bottom of this bottom electrode, it does not have any insulating layer at the bottom side of the wafer you have delineated this portion but this side is intact. So that mean one you can take here one you can take here and the third you can take ether side or from the bottom. That means say middle is fixed from middle and this will give you the one C1 and similarly this and this you will group another C2. This and this will give because this is a common contact you are making. So in this way you can get after the 3 wafer bonding.

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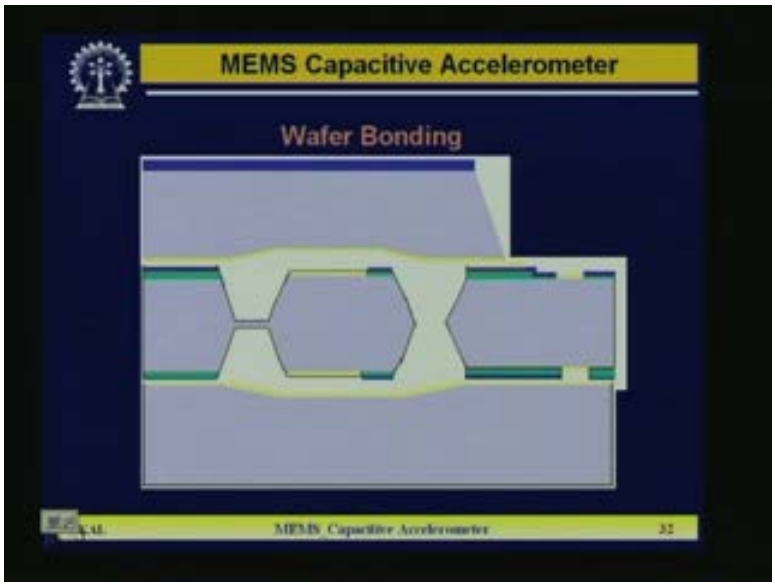

You can get the complete thing, the wafer bonding has been taken place. Both top and bottom now we are joined together got the 3 structure. So in this way one by one you fabricate separately. Now the assembly is another very important point in this particular the capacitive accelerometer fabrication where you have to have the both C1 and C2 top and bottom capacitance contact should be proper and then you will, because you now these C1 C2, both capacitance structure top and bottom will help you. Elimination of any parasitic or some noise pickup, because you are giving stress on your differential capacitance. Difference delta C1 minus C2 that is proportional 2g, that variation will be g will be there that we are interested. So in that way because you see here lot of the conducting planes are there and if you use the conducting silicon wafer, there is also going to create a problem because conducting wafer with another ground plane it will have some parasitic also.

And that are major concern case of many capacitive accelerometers. So there we have to see certain design modification certain techniques. So that those parasitics can be a removed completely. So this is the complete process sequence of this capacitive accelerometer structure and I am not going to discuss further on this and now we will discuss another inertial sensor, so that is a gyro sensor. So we covered two case studies; one is a piezoresistive accelerometer, the second one capacitive accelerometer with certain goal and how we design it and after design how we fabricate also. That also we discussed in both the cases. Now I will give some stress on the another kind of inertial sensor. That is a the gyro or rotation sensor and there I would like to give some stress on the quartz gyro sensor with little introduction of silicon gyro. So next class we will discuss on gyro sensors; MEMS gyro sensors. Thank you very much.