Digital Systems Design
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Lecture - 26
Programmable Logic Devices

Today, we will start a new topic that programmable logic devices. So, what do we mean by programmable logic devices and what are the different categories of this device. How the digital designs can be made using this programmable logic devices. We will read all these things in this class.

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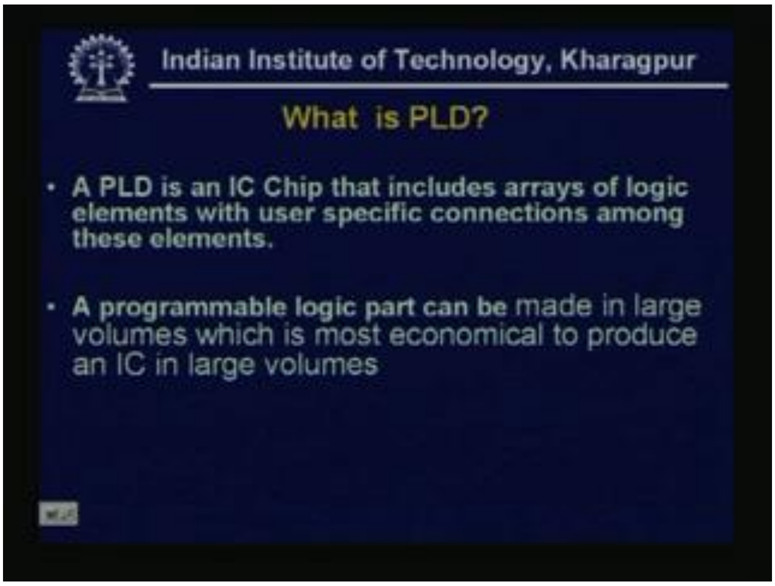

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What is PLD?

- A PLD is an IC Chip that includes arrays of logic elements with user specific connections among these elements.
- A programmable logic part can be made in large volumes which is most economical to produce an IC in large volumes

So, first we see, what do you mean by a programmable logic device or in short we call PLD. So a PLD is an IC chip, we think that includes arrays of logic elements, with user specific connections among these elements. Normally, it has two different arrays and they are, they can be programmed from outside. Now, we will see, how these arrays are programmed, what is the structure of this array, later and why it is so popular or what is the advantage.

So, mainly the, this is the programmable logic part or PLD, consists of the programmable logic part and the large volumes, which is most economical to produce an IC, we know that, the integrated circuit, that is advantage is mainly or the when we have discussed the VLSI. So, we want, nowadays we want that IC should be made, such that large volume of designs can be consist of a, or can be fabricated on a silicon. Now, this is the advantage of the programmable logic, that within small area, this devices can be fabricated. So, that is why, nowadays, this is the state of the art of the digital design, that the IC or most of the IC consists of a PLDs.

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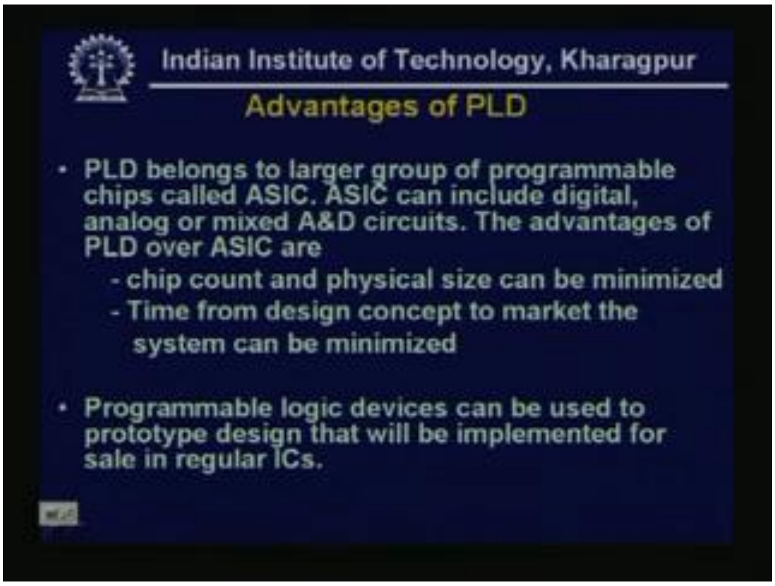

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Advantages of PLD

- PLD belongs to larger group of programmable chips called ASIC. ASIC can include digital, analog or mixed A&D circuits. The advantages of PLD over ASIC are
  - chip count and physical size can be minimized
  - Time from design concept to market the system can be minimized
- Programmable logic devices can be used to prototype design that will be implemented for sale in regular ICs.

Now, what is the advantages of programmable logics, so PLD belongs to a larger groups of programmable chips called ASIC. So, we know that, ASIC is the application specific integrated circuit, we have, we discussed earlier and that can include the digital design, that can include the analog or mixed analog and digital circuits. Now, the advantages of this programmable logic over ASIC, means, if this is a pure digital analog or mixed type, where the program, PLDs are not there.

We have designed, that the different type of design we have discussed, that semi custom, full custom, where the PLDs are not there. Now, if we consider the ASIC with PLDs, then the chip count and physical size can be minimized, why physical size is minimized. Because as already I mention, this is very compact and a large volume of PLDs can contain in a very small area in the IC, another thing is, as already the arrays are there, see just very simple way, we, what we can tell.

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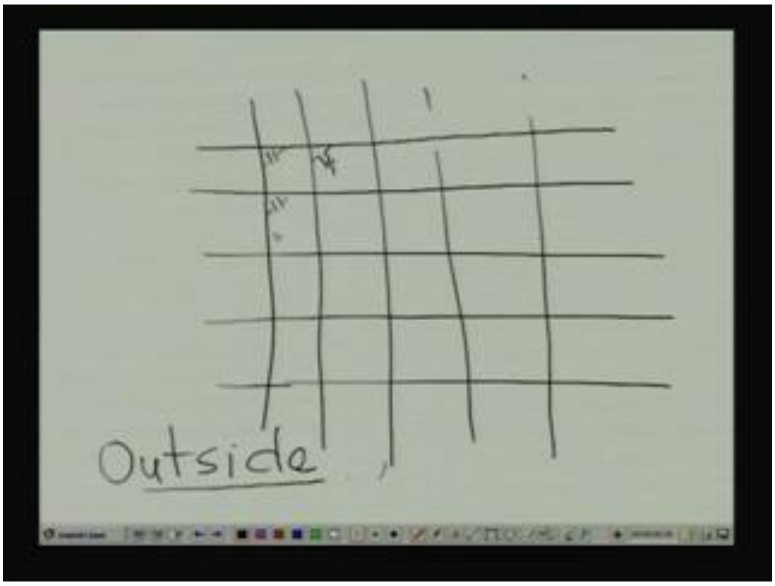

Say, as if, say this is some, some 2 D arrays, see this is some of the rows and say some of the columns are there, we will see later that how actually they are designed. Now, whether here there is a connection or not, that means, if I put a transistor here, say here or that can be in diode, that can be transistors, in this way if we put, then that can be programmed from outside. So, this is the user specification or depending on the requirement, what they want to design.

As if, these lines can be controlled from outside, so or this can be controlled mean, this can be programmed from the outside. So, the main advantage is that,((Refer Time: 06:03)) here everything is already there or it is fabricated, only it is programmed from the outside. So, time from design concept to market the system, that means, once the problem is identified or what design we want, starting from that we will, be marketing the system, this time can be minimized. Because, only program time is needed or the hardware is actually available or already predesigned in the ASIC.

The programmable logic devices can be used to prototype design, that will be implemented for sale in regular ICs. So if one is available, that means, the prototype designs that, it is available, then only again depending on the users or the depending on the variety of design requirement, that can be programmed. So, this is a very good advantage.

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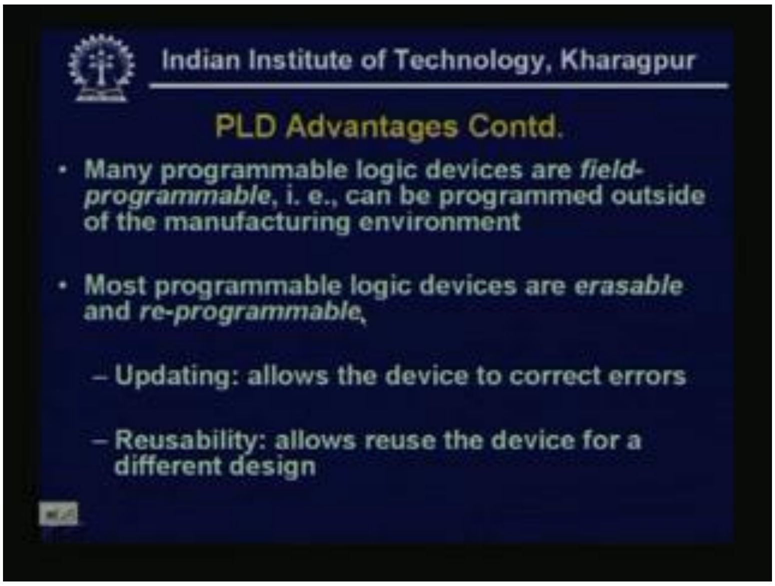

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PLD Advantages Contd.

- Many programmable logic devices are *field-programmable*, i. e., can be programmed outside of the manufacturing environment
- Most programmable logic devices are *erasable* and *re-programmable*.
  - Updating: allows the device to correct errors
  - Reusability: allows reuse the device for a different design

Now, some more advantages you see, that many programmable logic devices are field programmable, that is can be programmed outside of the manufacturing environment. Most programmable logic devices are erasable and re-programmable. This is one of the very important issue or the property, why the programmable logic devices are so popular or becomes the state of the art, of the digital design. See, they can be erasable and re-programmable.

So, one prototype is available or see that, one, what we have described, that as it one array, array of logics are there, this hardware is available, from outside depending on the design requirement, we are programming that thing, so we get one specific hardware. Now, as it is work or it demand finishes, it is requirement finishes, then the same hardware we can use for another design, that is why, it is, it can be, it can be made erasable and re-programmable.

Now, updating for this purposes, we need the two things, one is how to update and how to reuse, so updating means, allows the device to correct errors. See, even the program is available and some minor modifications are needed, then it can be done. And reusability, allows reuse of the device for a different design, that is that re-programmable or the hardware is there and the different programming, we can embed on this on different time.

So, we will get a different design on the same hardware and this is called the reusability of the PLDs. So, this is, one of the major property or the design property of PLD that, why it is so important or why it becomes the, state of the art of the digital design.

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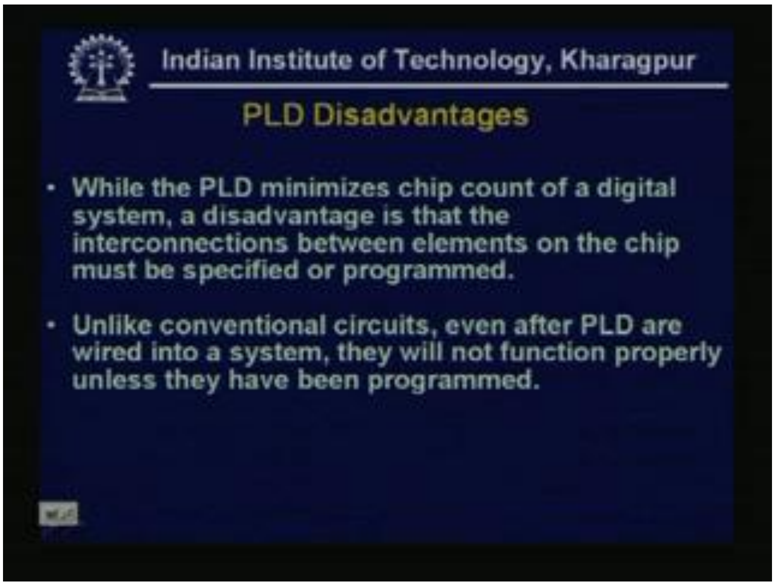

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PLD Disadvantages

- While the PLD minimizes chip count of a digital system, a disadvantage is that the interconnections between elements on the chip must be specified or programmed.
- Unlike conventional circuits, even after PLD are wired into a system, they will not function properly unless they have been programmed.

Now, what are the disadvantages, there are some minor disadvantages are there, because now the complex PLDs are used and while the min, PLD minimizes the chip count of a digital system, the disadvantage is that, the interconnections between elements on the chip must be specified or programmed. So, when that interconnections, this is once says it is a flexibility.

But as well as, this is very cumbersome to do that thing, because we have the cells to be programmed or the logic cells as well as the interconnections, that to be programmed and this becomes it makes the system or the design to be complex. Unlike conventional circuits, even after PLD are wired into a system, they will not function properly, unless they have been programmed. So, obviously, I have only one fixed hardware and unless, I program it correctly, it should not work.

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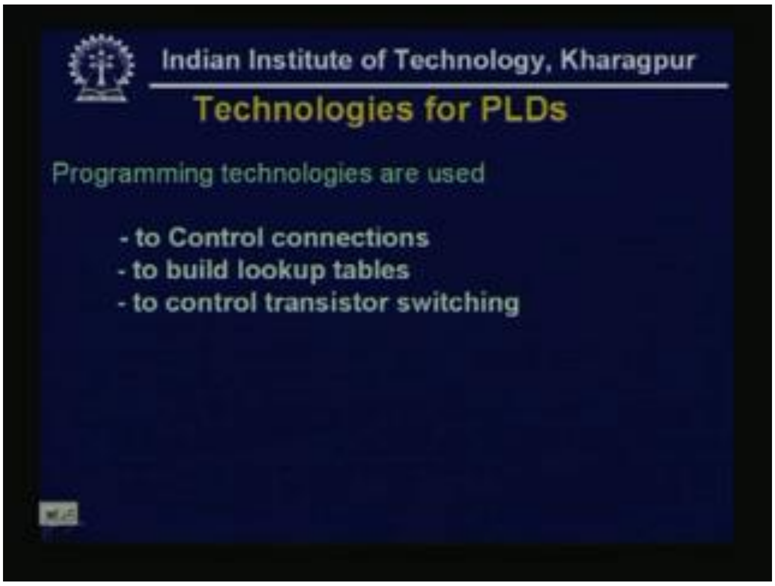

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Technologies for PLDs

Programming technologies are used

- to Control connections
- to build lookup tables
- to control transistor switching

Now, what are the technologies for PLDs, technologies means, that mainly the programming technologies. Now, programming technologies are used to control connections, to build lookup tables and to control transistor switching, now one by one we see that thing.

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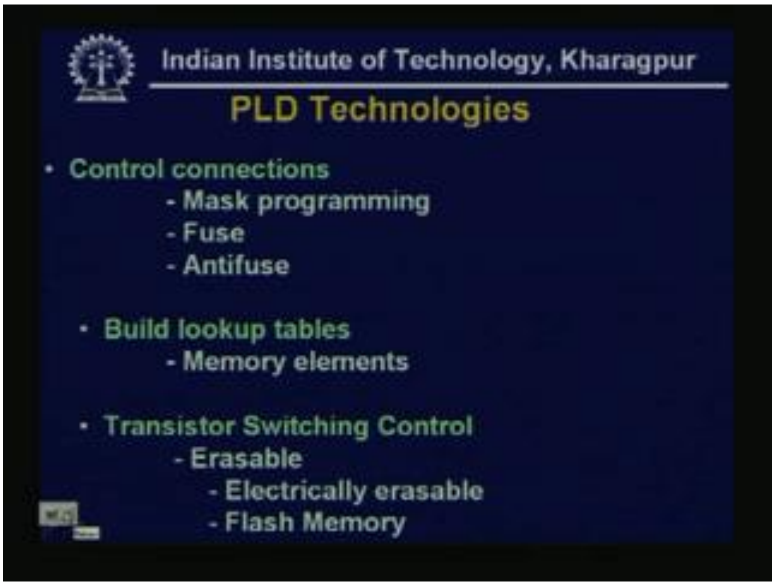

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PLD Technologies

- Control connections
  - Mask programming
  - Fuse
  - Antifuse
- Build lookup tables
  - Memory elements
- Transistor Switching Control
  - Erasable
    - Electrically erasable
    - Flash Memory

First, we see the control connections. So, these are, normally this mask programming or fuse and anti-fuse that are being used. We see that thing already, say if we, see like that…

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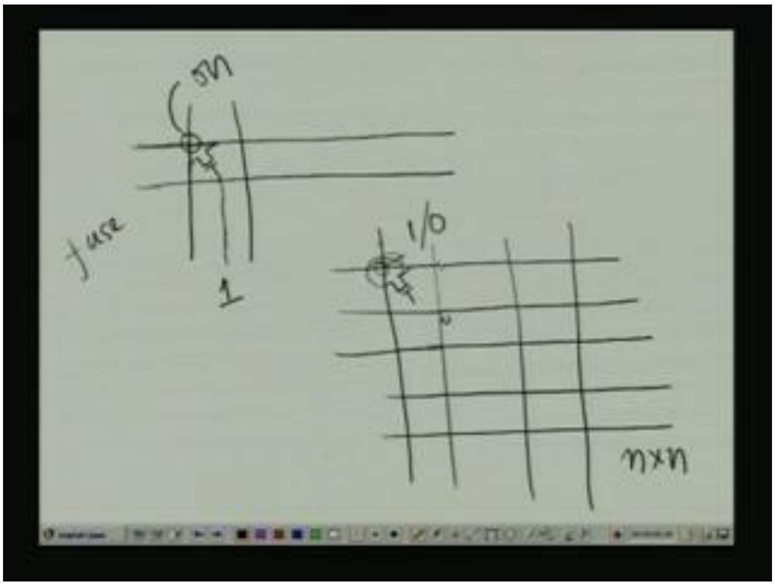

So, I have ((Refer Time: 12:05)) some, there I take only two things. So, these are some arrays, now I want, see some transistors are there. So, if I give this gate, see if it is a bus transistor, if I give, get a 1, then this and this should be connected. That means, which lines, these lines and these lines, that means, this point I will be getting on, then I am calling, this is a fuse. That means, this, the reverse thing should be, that reverse technology is the antifuse.

So, in that way, that means if I put… we can tell this is a switch. So, if I have a generic or a general array, array and whether I want a connection or not, that means, here if I get a 1 or 0, then what I will be doing that I will fuse this connection. That means, it can be a transistor, it can be a diode at every cross points. If this array is a, n by n then, there are n square cross points are there and these cross points, whether I get a connection or not.

Then accordingly, the element that has been used, element either this can be a transistor or this can be a diode. Then, these elements are on or off or the proper voltages, this can be programmed we can tell. So this is normally, just to control circuits, we call, this is fuse, antifuse or the mask programming is being used. So,, this is for the control connections.((Refer Time: 14:48)).

Now, another basic building block of the PLDs are the lookup tables. Normally, the PLDs are designed implemented using the concept of lookup tables and all lookup tables, say what is lookup tables, we will see again, we take an example.

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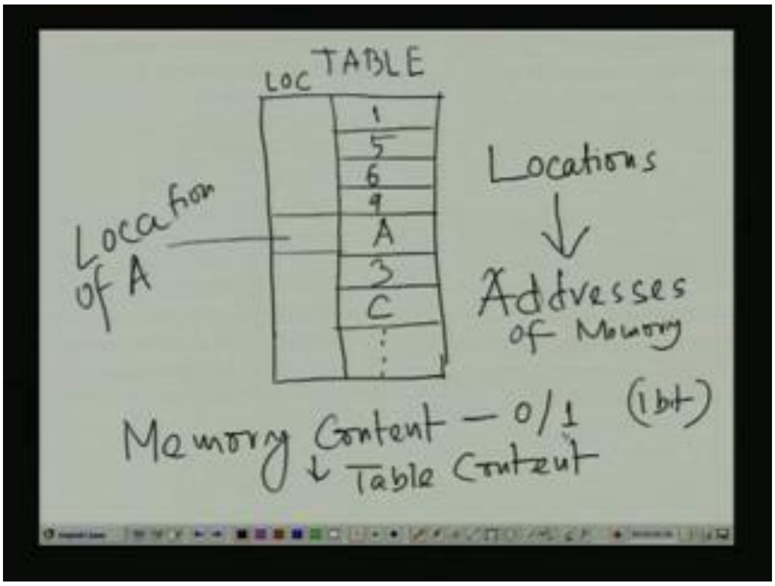

Say, I have, I have one table, I have one table and here, something is stored, some values are stored, say here it is stored 1, 5, 6, 9, A, 3, C like that, now see this is, in this table some values are stored. Now, if I want to get A value, then I have to give the, which location A is stored and say actually, normally this location we called the address of the table or the location. That means, whenever I want to get A from this table, I will give a location of A, and from there I will access A, similarly.

So, this is the concept of the lookup table, now see, if I treat this table as if this locations, this locations are nothing but the address, this locations we can take the address, addresses of the memory and the memory content are the table content. So, the memory content, normally these are 0 or 1, for 1 bit, that can be, these are actually the table content. So, in this case, this lookup table can be used as a memory, because this location of the table, where some value is stored, these locations are treated as the address of the memory.

And the content of the table, is the content of the memory or memory element, 1 bit or if it is the 8 bit, 32 bit memory. Whatever be the thing, that is the content of the table or this is the memory. That is why, the lookup table always can be implemented as a memory elements, ((Refer Time: 18:10)) so lookup tables is nothing but the memory elements. Then, transistor switching control, this can be erasable because already we have discussed, that the PLDs can be erasable and reprogrammable.

So, then, we will use that type of switching or transistor switching, which is say erasable, means the volatile electrically erasable or the flash memory. That means, this type of control we use for the transistor switching control.

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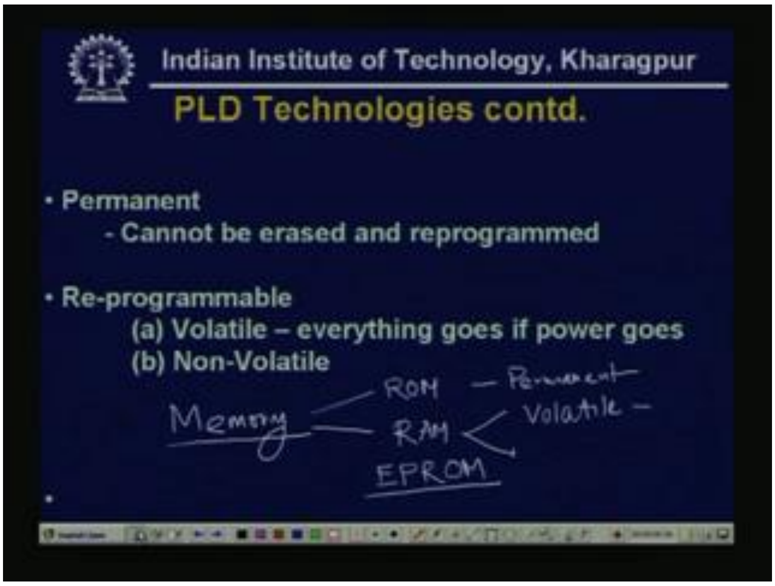

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PLD Technologies contd.

- Permanent
  - Cannot be erased and reprogrammed
- Re-programmable
  - (a) Volatile – everything goes if power goes
  - (b) Non-Volatile

Then, normally PLD technologies are either it can be permanent, permanent means cannot be erased and reprogrammed. That means, the memory we will use if it is a ROM, read only memory type. We have seen that, if it is a lookup table base and lookup table can be implemented by memory and if this memory is a read only memory type, that means, it cannot be changed. Then it is permanent, cannot be erased and reprogrammed.

That means, once we have programmed a design, that is a permanent or fixed one. So, though we are calling this is a programmable logic. But actually, the programmable means that only the hardware is available and only one time we can program the devices and we will get a one fixed design. Now, reprogrammable, these are of volatile or non-volatiles, means everything, volatile everything goes if power goes.

If we use a volatile memory, that means here, everything we are using. The lookup table is, how the lookup table is implemented, by what type of memory. So, if we use the memory, the memory element or the memory, type of memory. So, if this is a ROM type then, it is a permanent PLD, we will get only one fixed design for one PLD permanent type. Now, if it is a RAM type, that means, we can change here. Also there can be two type, volatile memory or non-volatile.

If it is a volatile, we know, that if power goes then everything go, if it is non-volatile, that means, once we have programmed, then it will be there. So, depending on the requirement or the board we use, say for academic purposes, or for our laboratory uses, if we use some programmable devices, obviously, we want that, some reprogrammable type of thing. That means, for one, say the logic devices are available programmable logic devices, say we will program for a one particular design.

And then, if it is a volatile, if the power goes everything will go or even if the power is there, it can be non-volatile. That if power goes, then also we will get a same design, but we it can be reprogrammed. That means, it can be erasable and, so here also, for it is that erasable type of EPROM, that erasable programmable ROM, that also we can use here see EPROM also we can use. So, mainly the type of, different type of memory we use, depending on that, that different type of PLDs we can get.

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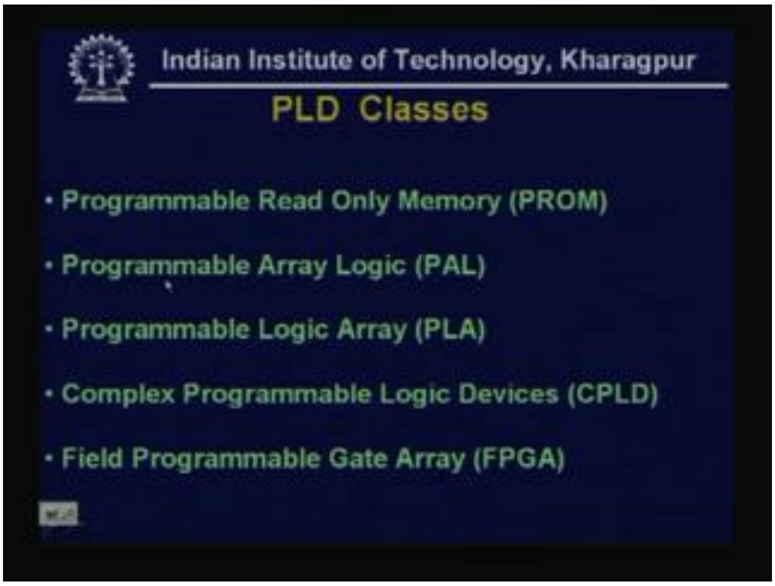

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PLD Classes

- Programmable Read Only Memory (PROM)
- Programmable Array Logic (PAL)
- Programmable Logic Array (PLA)
- Complex Programmable Logic Devices (CPLD)
- Field Programmable Gate Array (FPGA)

Now, we see what are the different configurations, normally we call the PLD classes. So these are programmable read only memory, PROM, programmable array logic, the PAL, programmable logic array, PLA, complex programmable logic devices, we call CPLD and field programmable gate array, FPGA. Now, one by one we will see that, what do we mean by all this classes, what are the differences etcetera.

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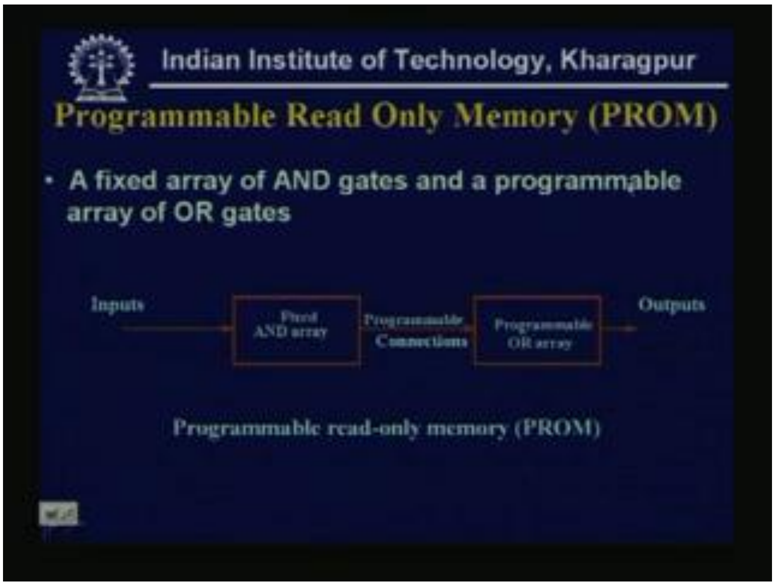

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Programmable Read Only Memory (PROM)

- A fixed array of AND gates and a programmable array of OR gates

Programmable read-only memory (PROM)

First we see the read only memory type. So, if these are fixed array of AND gates and a programmable array of OR gates first thing is, whatever be the type, normally the first three, ((Refer Time: 23:47)) the programmable read only memory, programmable array logic and programmable logic array, for this three, there are two arrays. The first array is called the AND array and the second array is called the OR array. Now, both arrays can be programmed.

Now, depending on the programmability or the order of programmability, degree of programmability, classifications have been done. So, if it is a fixed AND array and only the OR array can programmed, then we are calling that this is a read only memory. So, the structure is, if we apply the inputs to the fixed array, fixed AND array and the AND array outputs, this programmable connections… These can be programmed and it is going to a programmable OR array and giving the outputs.

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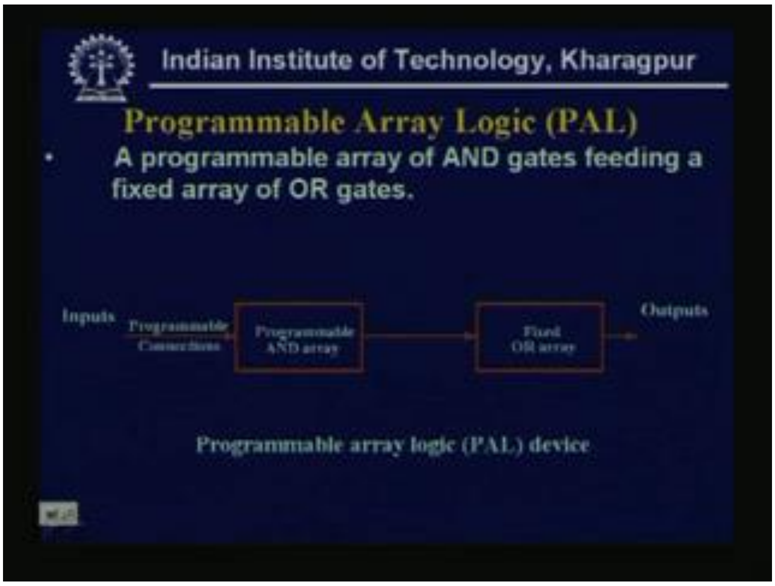

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Programmable Array Logic (PAL)

- A programmable array of AND gates feeding a fixed array of OR gates.

Inputs

Programmable Connections

Programmable AND array

Fixed OR array

Outputs

Programmable array logic (PAL) device

Now, programmable array logic, PAL, so here, a programmable array of AND gates feeding a fixed array of OR gates. That means, PAL is the, just the reverse of PROM, programmable read only memory, see here, the AND array is programmable. So, when the inputs are going, that can be programmable connections, array is programmed, array can be programmed. This AND array can be programmed and this is a fixed OR array, but OR array is fixed. So, this is called the PAL, programmable array logic.

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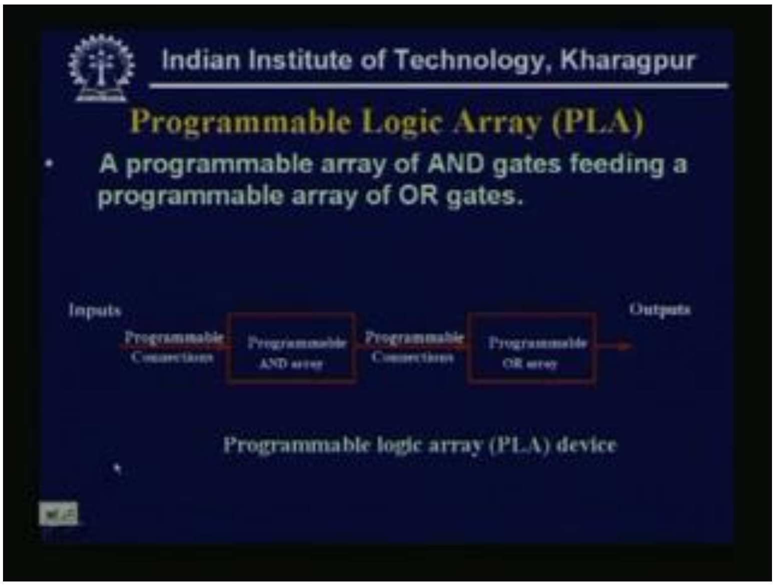

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Programmable Logic Array (PLA)

- A programmable array of AND gates feeding a programmable array of OR gates.

Inputs

Programmable Connections

Programmable AND array

Programmable Connections

Programmable OR array

Outputs

Programmable logic array (PLA) device

Then programmable logic array, PLA, here this is more flexible at both the arrays, AND array and the OR array, both the arrays can be programmed. See, this is programmable AND array, programmable OR array and the connections input as well as the intermediate inputs of the OR array, both can be programmed, so this is called PLA.

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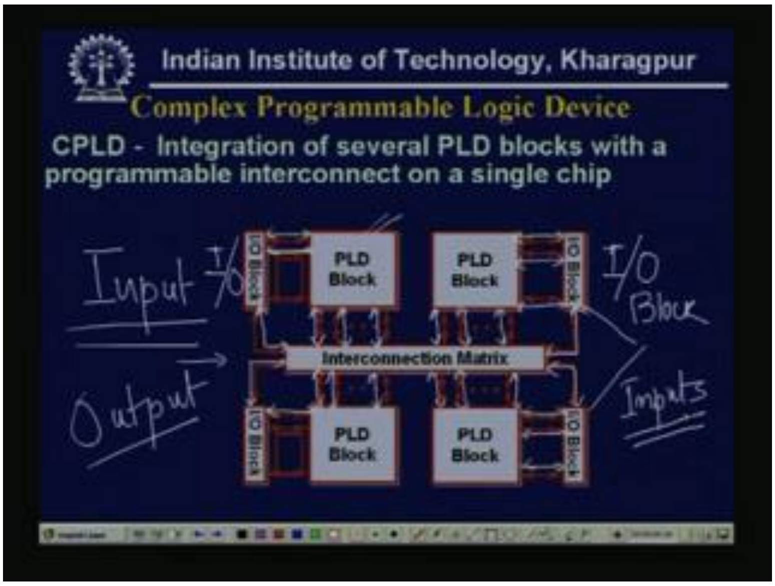

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Complex Programmable Logic Device

CPLD - Integration of several PLD blocks with a programmable interconnect on a single chip

Now, we see that complex programmable logic devices. So, now we have seen that PLD blocks, that can be say PROM type, PLA type, PAL type, three, we have already seen, programmable array logic, programmable logic array. Now, using anyone of this, we have seen that, this is the PLD blocks, programmable logic devices blocks and there are some IO blocks and these are the, these are interconnection matrixes.

Now, from this interconnection matrix, we can communicate or the switch can be done. Switching or the interconnections can be done using the, with the PLD blocks. So, this PLD blocks, similarly this PLD blocks, the interconnections can be made. So these are, now there are some IO blocks, so this is my IO, this is my IO blocks. Say, the left hand side, as if we are taking these are the inputs. So these are my input, so first, the inputs are feeding.

So, there must be some interconnection between the IO blocks and the PLDs. Similarly here and there are, the control lines are also coming from the interconnection blocks, IO blocks to interconnection. So, there must be some interconnection between IO block and interconnection matrix, because, actually it will control the, PLD blocks which will be selected or which will be connected. So, from IO blocks, these interconnections are there, now the PLD blocks are selected and say some outputs are generated.

So, again this side, that with this PLD blocks also the outputs, input output block, here also these two are IO, IO block that is also there and there must be the similar type of interconnection between the IO block and the PLD block. Here also, the similar interconnections are there and between the IO block and the interconnection matrix. There can be the connection, another thing is that, see this IO not only, as an example I have told that, this can be input.

Say, from this PLD block, some of the things can be the output, some outputs can be taken from this side or here also, some inputs can be applied from this side. So, it is totally programmable and totally flexible, only this is the compact architecture, that some PLD blocks, some IO blocks and interconnection matrix.

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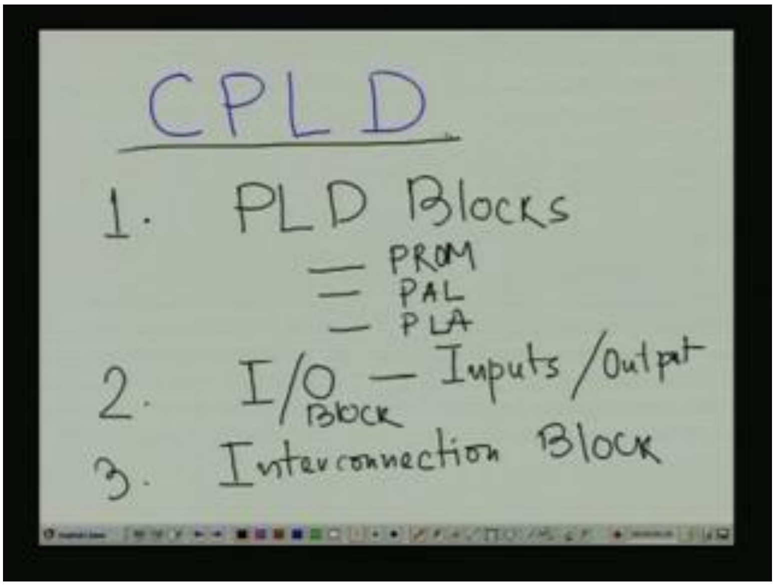

CPLD

1. PLD Blocks
   - PROM
   - PAL
   - PLA
2. I/O Block — Inputs/Output
3. Interconnection Block

So, what we can tell, that CPLD, so if we take the CPLD blocks, so it has three components, one is that some PLD blocks that can be made by PROM by PAL by PLA. Second is the IO block, where the, from the inputs and outputs are fed or taken out, so this is IO block and then, the interconnection block, so interconnection block, that is between IO and interconnections or interconnection to PLD blocks. So, mainly these three are the, that the three basic blocks, that is there in the CPLD structure.

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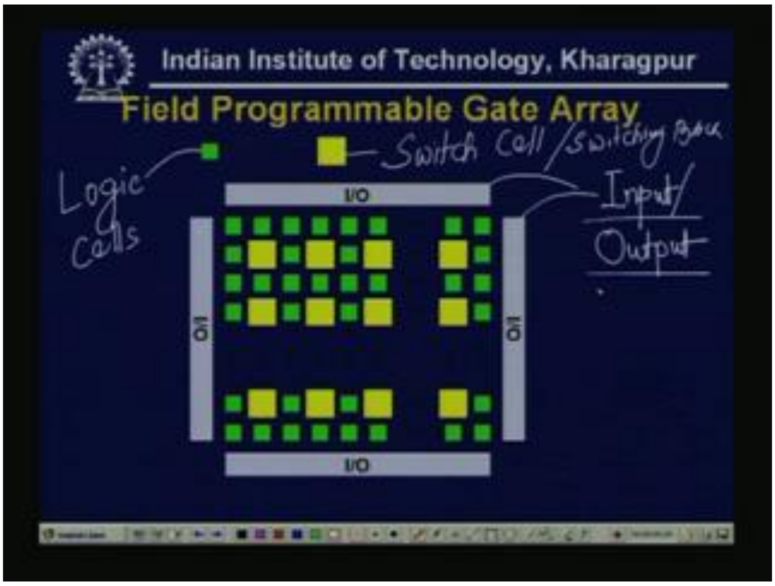

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Field Programmable Gate Array

Now, another is field programmable gate array and nowadays, this is the, state of the art of the VLSI design. So, as I mentioned, that this PLD devices are one of the basic building blocks of the ICs now and as there large volume of design can be built or can be fabricated, on a piece of silicon. So, this field programmable gate array is nowadays an alternate to the normal CMOS ASIC. Now, we see the structure, this is similar to the CPLD.

We will see that, see here also that, it is a 2 D grid structure and the boundary, the IO blocks are there. So these are my IO block, input, output blocks, these are the…and the, if we treat, this 2 D grid and or the, as a matrix, this matrix elements are of two type. See, in a picture, we have shown one small green block, this is our, say our actually, these are my logic cells, all logic blocks. And this larger yellow one, we take these are my switching block or switch cells, switch cell or switching block.

Now, these can be, this is field programmable, so actually from outside, that electrically this can be programmed, this cells can be programmed, as well as, this input outputs also can be programmed here. So, this is a totally flexible architecture, so mainly this, this is the fixed hardware or this is just like a form. That is if one hardware form, where the three different type of hardware, one of the logic cells, switching blocks and the IO blocks, that are available or we can take IO cell, logic cell, switching cell.

All are arranged in a 2 D fashion and they are programmed, from the outside, so this is the overall concept of the FPGA, later again, we will discuss in details. Now, we start that, so again if I summarize that, so far we have read, the different configurations of the PLD, one is the programmable ROM, PROM, programmable array logic, PAL, programmable logic array, PLA, complex programmable logic device, CPLD and the field programmable gate array, FPGA. Now, we will start discussion in details of the architecture or the actual architecture of the all this PLDs.

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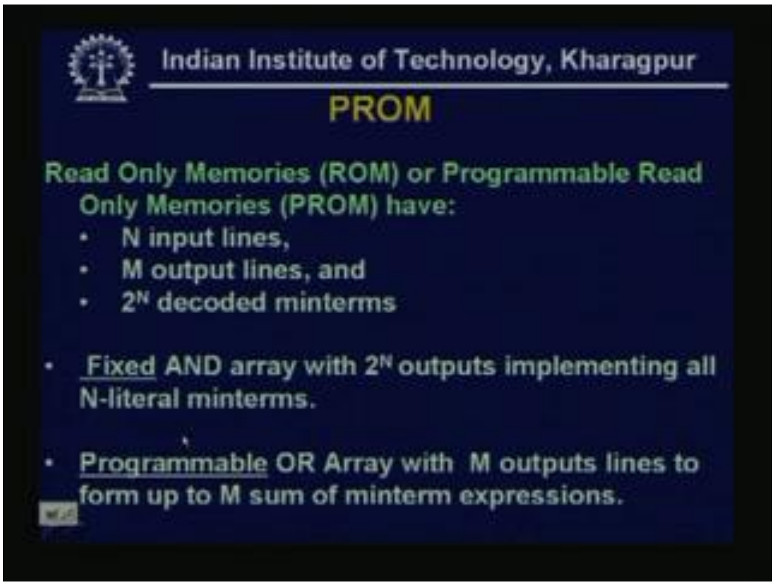

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PROM

Read Only Memories (ROM) or Programmable Read Only Memories (PROM) have:

- N input lines,
- M output lines, and
- 2^N decoded minterms

- Fixed AND array with 2^N outputs implementing all N-literal minterms.
- Programmable OR Array with M outputs lines to form up to M sum of minterm expressions.

So, first we see the programmable ROM, the first one, as already I defined or I have told that, this is a read only memories or programmable read only memories. So if it is read only memories, it has some, the in the memory, we know that, this has some addresses and some output address. Means that we give from memory element I want to get and as if output is the nothing but my memory content. So, here the specification is, that there are N inputs lines, M output lines and 2 to the power N decoded min terms.

If it is N input line, so we can by N input line, we can represent 2 to the power N values and this 2 to the power N, can be the min term. As if, the N input lines are nothing but the, N input variables. So all these, 2 to the power N values will give my, that minterms using N input variables and M output lines. So, M output lines, that means, I can get 2 to the power M values again, so M output lines. So, as if my content is a M bit, so my, as if this is a M bit memory.

So, as already we define the configurations of, configuration of PROM is a fixed AND array and a programmable OR array. So, if we remember the PROM, ((Refer Time: 40:05)) see this is fixed AND array, so inputs are coming, these inputs are N bit this and this is a fixed OR array. So, fixed AND array with 2 to the power N inputs, implementing all N literal minterms and programmable OR array with M output lines, to form up to M sum of minterm expressions. So, if block diagram level if we see, it can be like that.

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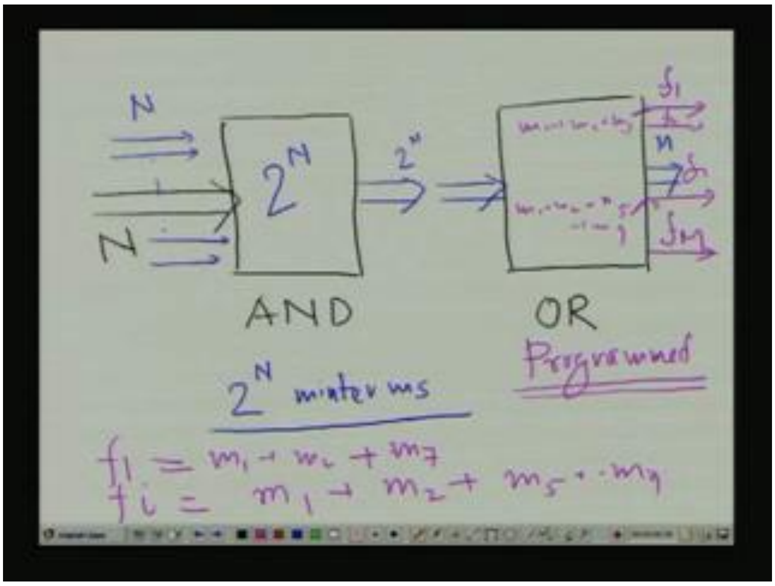

Say, I have 2 array, see this is my AND array, this is my OR array, say N input lines I am feeding N inputs, so as if, I am giving this in as, N variables, these I can represent as if, N, these are my N variables. So, here actually, 2 to the power N minterms, can be, this AND can represent 2 to the power N minterms, because N input variable, 2 to the power minterms. So if, these 2 to the power N minterms, output is actually 2 to the power N and that is fed to my OR array.

And this OR array is M output, so M outputs, I can get from the OR array, that means, I can, from these 2 to the power N minterms or using this 2 to the power N minterms, I can form M number of equations. That means, these outputs, if I tell these are my f 1, f 2 say f m, then this f 1 equal to, from these minterms, some minterms say M 1, M 2 like that. So, similarly f i is sum m 1, m 2, m 5 like that. So, in this way, I can form sum f m, so this is the configuration or the architecture of PROM.

So, it has N outputs, it has 2 to the power N inputs of the fixed, this is fixed AND array, so all 2 to the power N minterms can be treated as the, output of the fixed AND array. These are fed to the OR array and from there, accordingly this can be programmed, this OR is programmed. So, actually, depending on the design requirement, design specification, which minterms will be selected, see here f 1 is m 1 plus m 2 plus say m 7. So, here I will be taking this three and accordingly this, m 1 plus m 2 plus m 7 that is going to f 1.

Say f i, say this is my f i and that is nothing but m 1 plus m 2 plus m 5, so m 5 plus m 9 as m 9 and that is taken as… So, these m number of outputs or m outputs can be constructed from 2 to the power N minterms. So, this is the concept of the PROM.

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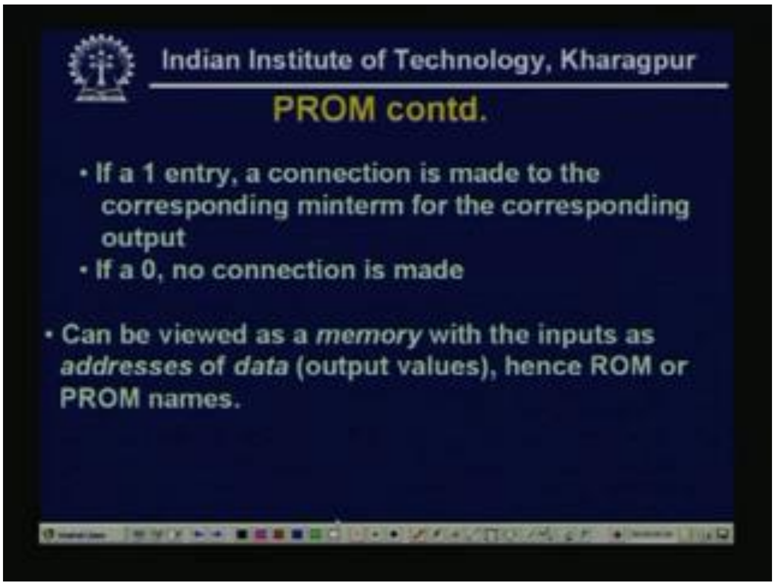

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PROM contd.

- If a 1 entry, a connection is made to the corresponding minterm for the corresponding output
- If a 0, no connection is made

- Can be viewed as a *memory* with the inputs as *addresses of data* (output values), hence ROM or PROM names.

Now, if 1, if a 1 entry, a connection is made to the corresponding minterm for the corresponding output, if a 0, no connection is made, so this is the conventional thing. That means the, when I get the AND array, which minterm I will be taken, which minterm, just now I have shown, that m 1 plus m 2 plus m 5, then the m 1 crosses. I will give a one entry, just like that ((Refer Time: 45:43)) our Karnaugh map of conventional for a Karnaugh map does can be viewed as a memory, with the inputs as addresses of data, hence ROM or PROM names. That is why it is called as the semi programmable logic, why it is called a ROM, read only memory. See, it has some fixed, 2 to the power N, just now, I have shown.

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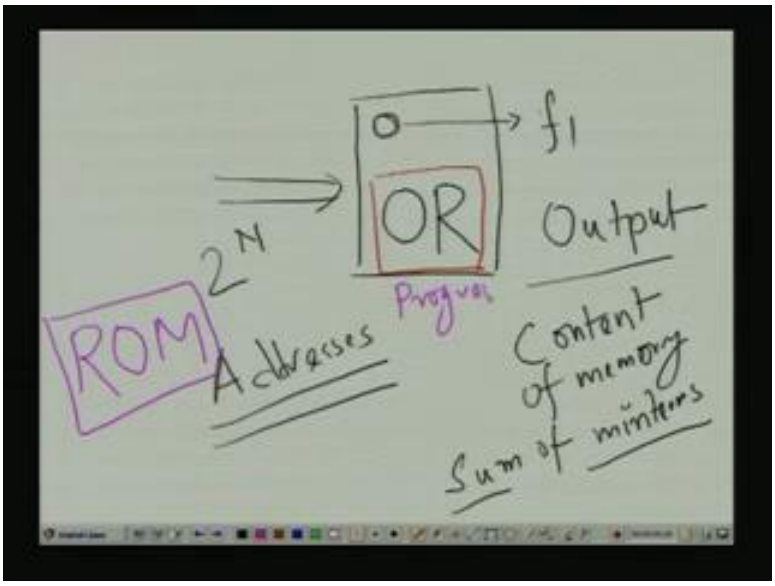

So, if I consider only the OR, as if, it has 2 to the power N inputs, the minterms, this can be treated as a addresses. So, this is n bit, as if this is n bit address and from there, which value, as if these addresses, that you will give that, that the values will be taken. So, this is in the m 1 or that, what just now I called f 1 are taken. So, this can be address and this output is nothing but the, as if the content, content of memory, which is actually the sum of minterms, selected minterms, sum of minterms selected.

And how it is selected, that as it is programmed. So, these are some of selected minterms depending on the program, because it is a programmable OR, this is the OR and that is programmable, this is OR block and this is programmable. So, what actually we are getting, this is nothing but a addresses, address and the content of memory. So, this is, as if read only memory, the ROM and as the OR is programmable. So, this is also programmable OR. So, programmable PLD that is a programmable ROM or PROM.

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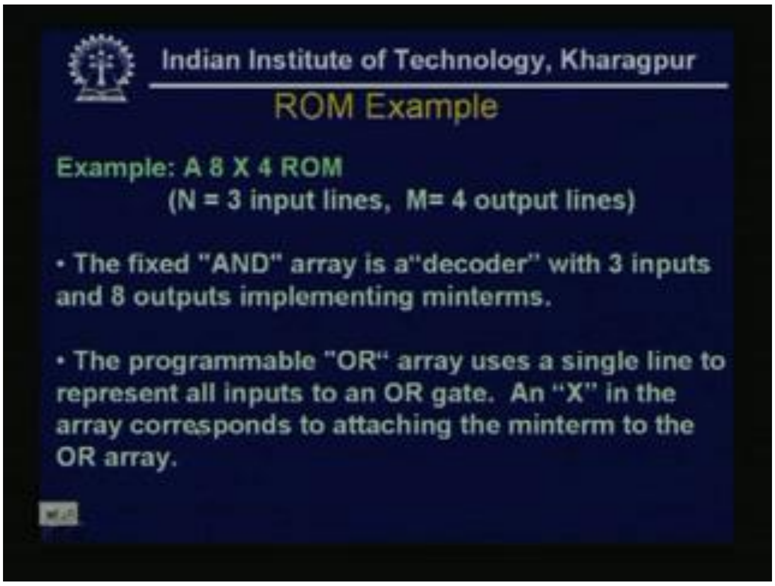

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ROM Example

Example: A 8 X 4 ROM
(N = 3 input lines, M= 4 output lines)

- The fixed "AND" array is a"decoder" with 3 inputs and 8 outputs implementing minterms.

- The programmable "OR" array uses a single line to represent all inputs to an OR gate. An "X" in the array corresponds to attaching the minterm to the OR array.

Now, you take one example, say A, we are taking a 8 by 4 ROM, so 8 by 4 ROM means, there are 8 address lines.

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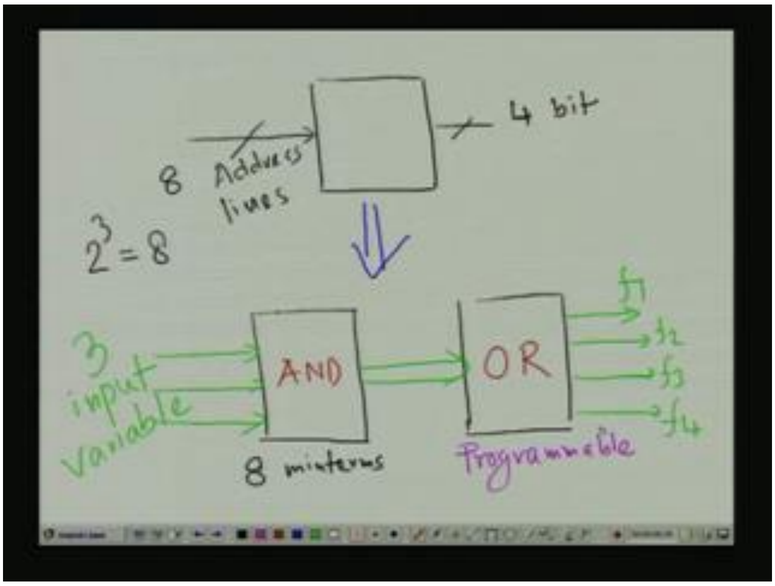

So, if we see one memory, it has 8 address lines and 4 bit content output. So, what we can do, if I want to get this thing by or I want to implement this thing by, PROM or programmable logic device, then this is my AND, this is my OR, so here 8 address lines. So, I need, I know 2 to the power 3 equal to 8, 2 to the power 3 equal to 8, so here AND gate, there will be 3 inputs, 3 input variable and number of minterms, that there will be 8 minterms, that will be fed and there are 4 bits. So, these are f 1 and f 4 and it can be programmed.

So, actually depending on the f 1, f 2, f 3, f 4 values, that means, my design required design or the design requirement, that which minterms will be selected, that will be programmed. So, this is, this part is programmable, this is programmable, which minterm will be selected, so this is my mapping, that a 8 by 4 ROM and that is, this is the programmable thing. ((Refer Time: 52:48)) Now, this fixed AND array is nothing but a decoder, because it has 3 input, 8 output.

That means, it is a 3 by 8 decoder and 8 output implementing minterms, the programmable OR array, uses a single line to represent all inputs to an OR gate and cross in the array corresponds to attaching the minterm to the OR array. That means, a cross means, it is a one there, that means, that particular or we can tell the, it is fused or we can tell the switching element, transistor or diode that there, that is on, whatever we call, in different level of design specification. And the, how the programming is turned on the programmable OR array.

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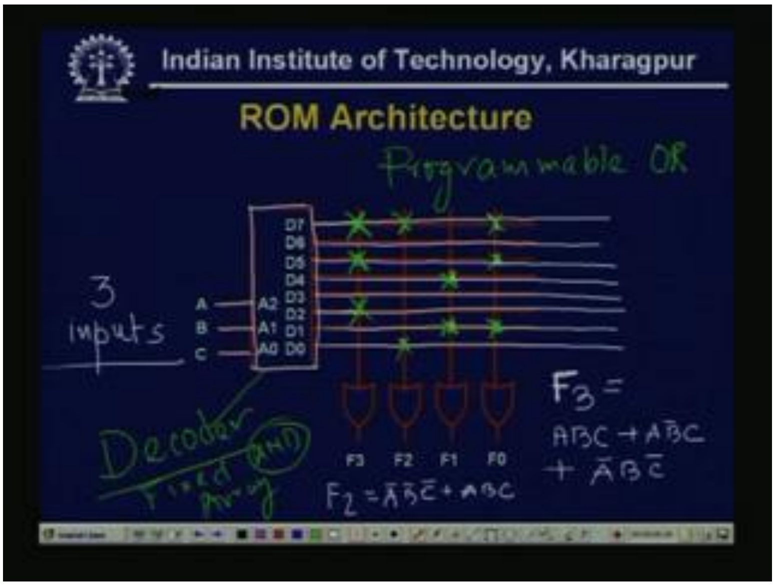

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ROM Architecture

So, we see the design, see, if we draw, so this is my 3 by 8, so this is a nothing but a 3 by 8 decoder, it has 3 inputs, say A, B, C and there are 3 inputs. Now, there are, a 3 by 8 decoder, so 8 output lines 2, 3, 4, 5, 6, 7,8, there are 4 output lines. So, this is my, as if this decoder, this is the, this is the decoder, this give me the fixed AND gate, AND array, fixed AND array and this is my programmable OR, this portion is my programmable OR array.

So, F 3, see here, there is a cross point, this is one cross, this is one cross, this is one cross. So, what is my F 3, see my F 3 is the, this minterm consisting, coming from the D 7, that means my A,B,C, say if it is 1, 1, 1 in that way we take. So, this is ABC plus, say D 5 means 5,1, 0, 1 means A B bar C plus the D 2, means 0, 1,0, so A bar B C bar, so my F 3 the one, one of the output is ABC plus A bar B C plus A bar B C bar. Similarly, F 2 we are seeing that, this is the, this two are the.

So, what is my F 2, then my F 2 is D 0 means, A bar B bar C bar all 0, plus ABC, my F 1, this 0, 0, 1 means A bar B bar C plus 1, 0, 0 means A B bar C bar, my F 0 is this cross term, plus this minterm, plus this minterm. In this way we can draw this thing, now we see today’s quiz questions.

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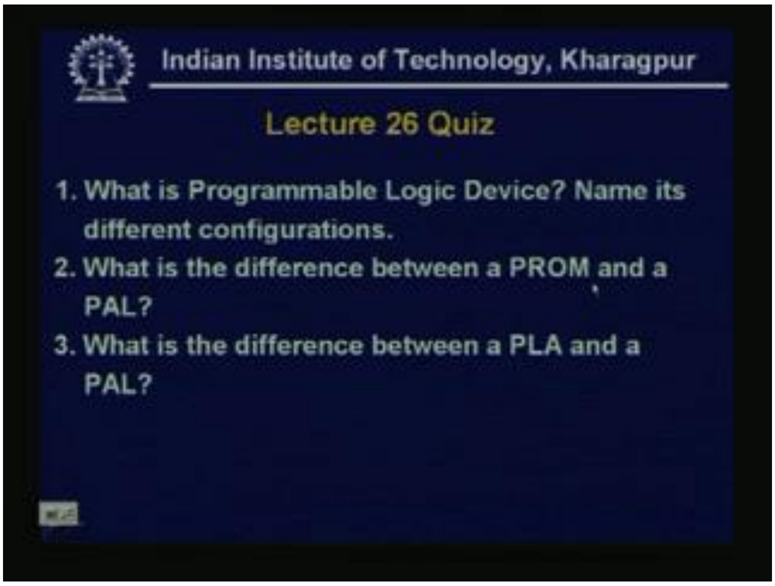

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Lecture 26 Quiz

1. What is Programmable Logic Device? Name its different configurations.
2. What is the difference between a PROM and a PAL?
3. What is the difference between a PLA and a PAL?

Say, what is programmable logic device? Name its different configuration as I discussed, What is the difference between PROM and a PAL? What is the difference between a PLA and a PAL? So, mainly the different configurations and the what are the differences between the different configurations, that are the main quiz questions of lecture 26.

Thank you.

In last class, we have started the discussion on programmable logic devices, so far we have read the, what do you mean by programmable logic devices and the different configurations. Now, we will continue this class the same thing, the programmable logic device, but before that, quickly we see the last class, the quiz questions of the last lecture. So, first question is, what is programmable logic device? Name its different configurations, so programmable logic devices.