Digital System Design
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Lecture - 22
Design of Sequential Modules

Last day, we have learned to design a sequential modules or actually what do we mean by sequential circuits and how we can store one bit memory or how the sequential modules are used as a memory. Then, we have seen the construction of the design of the SR latch, the clocked latch, the D flip flop etcetera.

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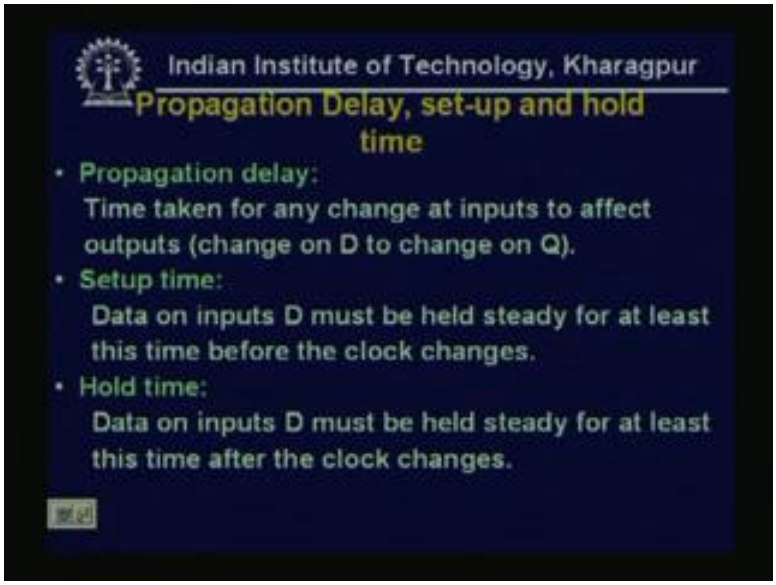

Now, today we will continue the discussion on the sequential modules the other different type of sequential modules that are being used in real life circuits. But before that we will see that what do you mean by the propagation delay setup time, hold time and actually how these times are affecting the actual value of the output line. So, first we see the propagation delay, it is defined as the time taken for any change at inputs to affect outputs. So, if we consider 1 D flip flop, then change on D that will affect the change on Q. Now, the time taken to propagate this affect from D to Q we are calling that is the propagation delay.

Now, setup time the data on inputs D must be held steady for at least sometime before the clock changes, so that we can get the fall free output. And this time before the clock changes the time for which it is needed to keep steady the data inputs of the inputs at the input line it is called the setup time. Similarly, the hold time, hold means the previous value holds at the output line last time we have learnt that thing.

So, after the clock changes the time needed to keep steady the input lines or the inputs at the line D is called the hold time. So, data on inputs D must be held steady for at least this time after the clock changes.

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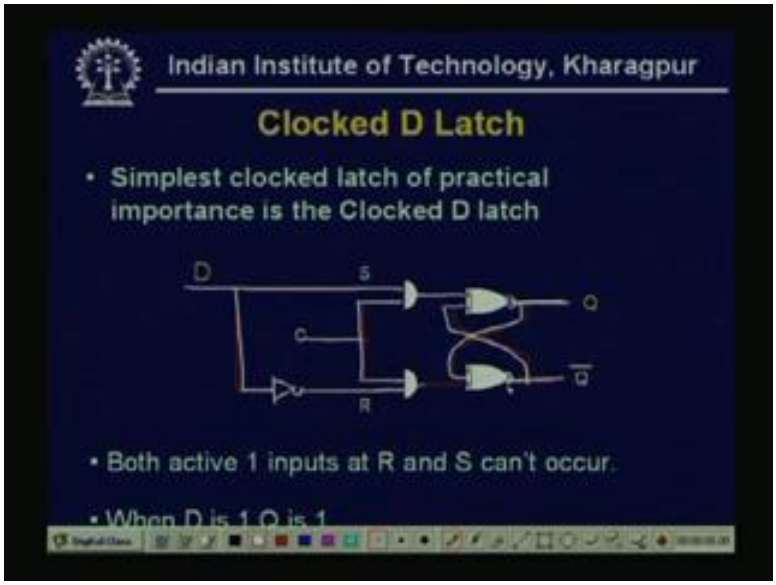

Now, if we see on the last day what we have seen the D flip flop again that it has only 1 input and another inverted input that means, from the same input it is as the R. And the clock is fed at the both the AND gate and then it is actually our SR latch that NOR gate, two cross coupled NOR gates. So, this already we have seen last day. Now, with respect to this or the timing specifications of the D latch if we see, then what will be the propagation delay setup time and the hold time that, we will be checking.

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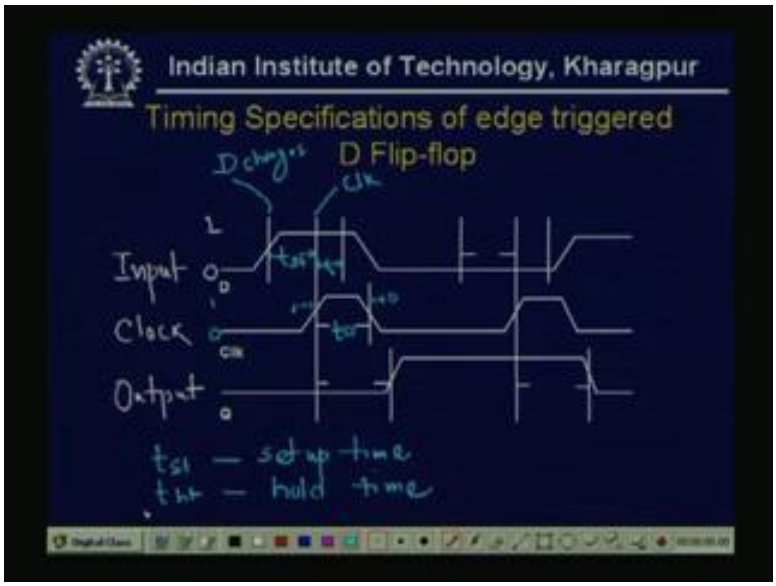

See these are the timing specification, now first this is my input line D, this is my clock and this is the output Q, now the D changes from 0 to 1. So, this is the line that when the D changes or this is the time when D or the input changes, see the clock changes from 0 to 1 this is the time, so this is my clock changes. So, this should be because, setup time we have define that the time that when it is keep steady before the clock changes that means, the inputs D inputs. So, this is should be my t setup, so this is my t s t that t s t is my setup time.

Now, after the clock changes the again input should be steady, so here it is after the clock changes. So, this is my t setup and this should be that hold time that means, t h t this is the hold time. Now, this is my the for the clock signal that see the clock changes 0 to 1 and this is clock this is 0 to 1 and this is my 1 to 0. So, this is my t w the clock width or clock time Now, the propagation delay now we have defined again if we see that how we have defined the propagation delay what happened see, I cannot do that. See propagation delay we have taken the time taken for any change at inputs to affect the outputs. So, here we must see the input and the output.

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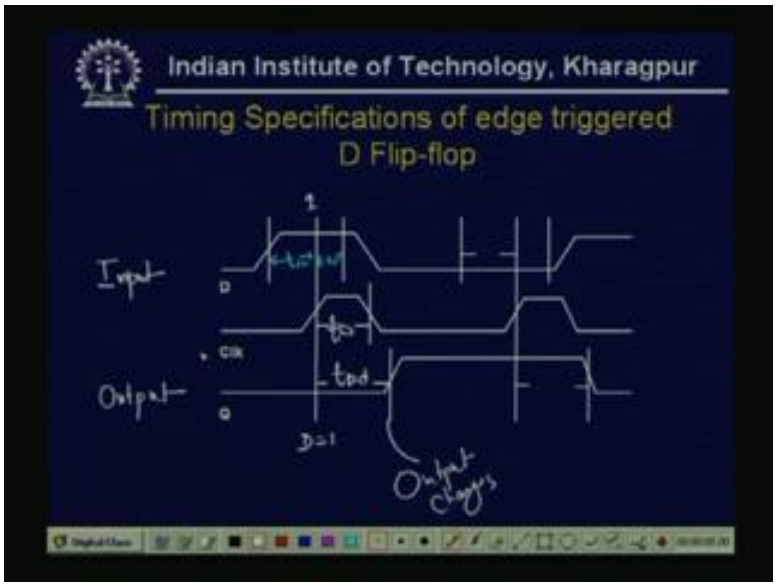

So, if we see now the input and the see now the input changes at this time and the, but the output changes. So, this is my Q this Q changes at this position, so this is my output changes. Now, if we see that this is my 0 to 1 and that the mid position this is by D equal to D becomes 1, so this is my propagation delay that t p d the propagation delay time. So, again if we write this is the t setup time this is the t hold time and this is the propagation time and this is my t w the clock time.

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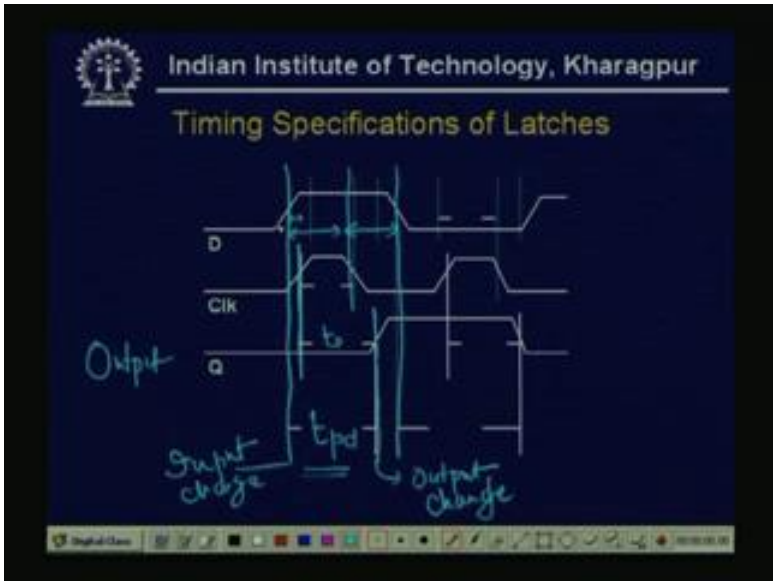

Now, if we consider the latch, If we consider the latch then similarly that this is again D and clock if we give that, so this is a clock latch. Then, similarly, the here the D changes from 0 to ,1 the clock changes from 0 to 1 this is the position. Here the clock changes from 1 to 0 and here the D changes from 1 to 0. Now, similarly that when D changes from 0 to 1 here the Q changes that means, my output the output changes from 0 to 1 is this position.

So, now see for the latch that this is the this is the input change and this is my output change and this time difference we have defined as the propagation delay t p d. Because the time taken to affect the change of inputs to the change of outputs. So, this is my time, now when the clock changes this is the time the clock changes and this is the time the output changes. So, this is again with respect to clock the propagation changes t p and as usual this is my setup time. That after the before the clock changes this should be the setup time and hold time, these are the 2 times.

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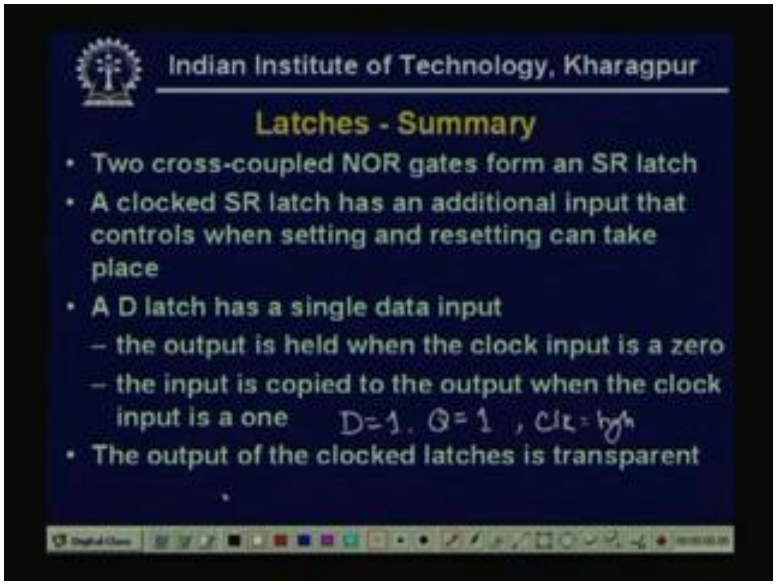

Now, so far we have discuss the latches, so if we summarize what we have read about the latches that two cross coupled NOR gates form an S R latch the set and reset latch. A clocked S R latch has an additional input that controls when setting and resetting can be taking place. A D latch has a single data input the output is held when the clock input is 0, the input is copied to the output when the clock input is in 1. Because we have seen

that when clock is 1, the D equal to 1, if D equal to 1 then Q equal to 1, When the clock is clock is high, now the output of the clock latches is transparent.

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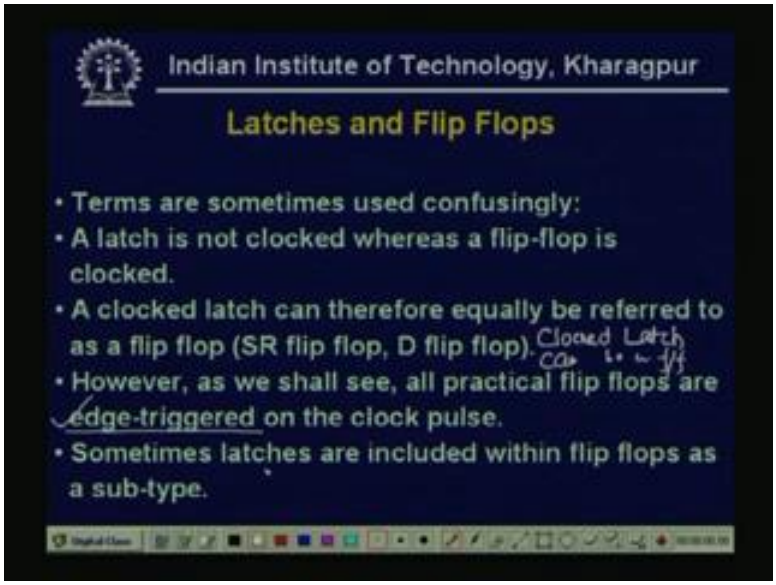

Now, we see that latches and flip flops, so these terms are sometimes used confusingly. So, we must clear this a the what is the difference between this two, see normally a latch is not clocked whereas, a flip flop is always clocked. So, initially when we have define the SR latch there was no clock only this is a two cross coupled NOR gate was connected. And S and R that 2 inputs are there, so a clock latch can therefore, equally be referred to as a flip flop, so S R flip flop, D flip flop.

We can tell now, clocked S R latch is the S R flip flop clocked, D latch is the D flip flop, so I can write that clocked latch clocked latch is a can be a flip flop. However, we will see that all practical flip flops are edge-triggered, another conversion is there that normally the flip flops are used in real life circuit they are edge triggered. And sometime latches included and the within flip flops as a subtype. So, sometimes it is a level triggered flip flop is also called or the level triggered latch. So, sometimes latches are also included within flip flops as a subtype.

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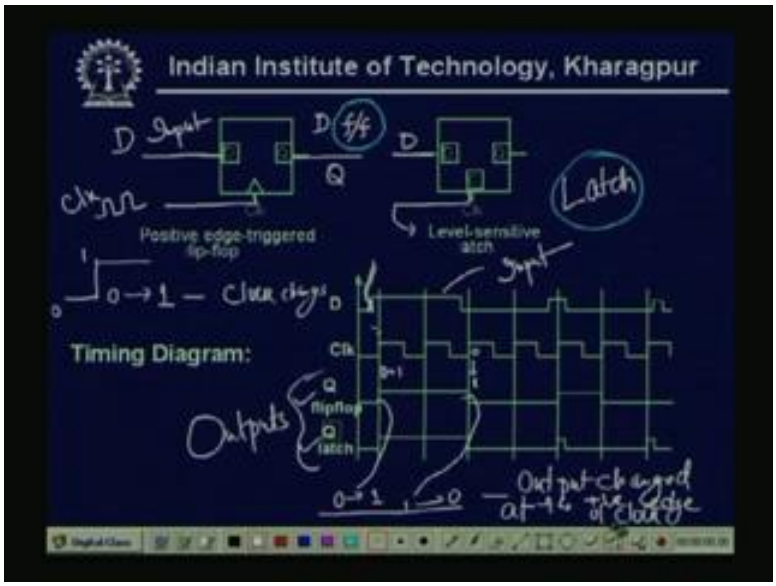

So, we see that it is a positive edge triggered flip flop, so this is a normal D flip flop this is my D input, this is a this is a D flip flop and this is the Q output. One clock is there clock input and this is the positive edge triggered that means, when this is a edge that means, this is a 0 to 1 this is 0, this is 1. So, this becomes a positive edge triggered that means, whenever the clock changes from 0 to 1 the clock changes 0 to 1 then only then only the D input is enabled and it will affect the output.

Now, it is a level sensitive latch, so this is the edge triggered and this is a level sensitive, so again we can tell that this here also clock is 1 input, but this is a level sensitive this is not edge. Similarly, this is the D input this is a this is a level sensitive latch, so this we can call that latch and this we can call a flip flop and this is a latch. Now, if we see that timing diagram of the flip flop and latch see this is my input D input.

These are my clocks and this is Q means these are the outputs we have taken one for the flip flop another for the latch. Now, if we see the timing diagram then see the D changes from 0 to 1 and the clock changes slightly after that. So, only the effect will be the Q will be changing from 0 to 1, when the clock will change not the not here when the D has changed from 0 to 1. The here D has change to 0 to 1, but clock has change slightly after that see here. So, the output will change when the it will be a 0 to 1 edge triggered 0 to 1 the edge triggered clock that time the output will be 1.

Now, D becomes 1, so again it is it becomes 1 see here D becomes 1 to 0, so that change is shown at the output line, when actually the Q is changed from 0 to 1 or 1 to 0. Here it is again it is a 0 to 1 next visit will be there if we it is a positive edge triggered then it is a 0 to 1. So, when the it is a 0 to 1 that time only the output changes from 1 to 0, so here it is a output changes here, the output changes 0 to 1 here the output changes 1 to 0.

And see both the times when the output changes that at the positive edge positive edge of clock positive edge of clock. So, this is that flip flop, so that means, this is a flip flop is a we can tell the flip flop is a edge-triggered flip flop. Now, we see that what will happen for the latch see if it is latch that means, it should be a level sensitive not the edge.

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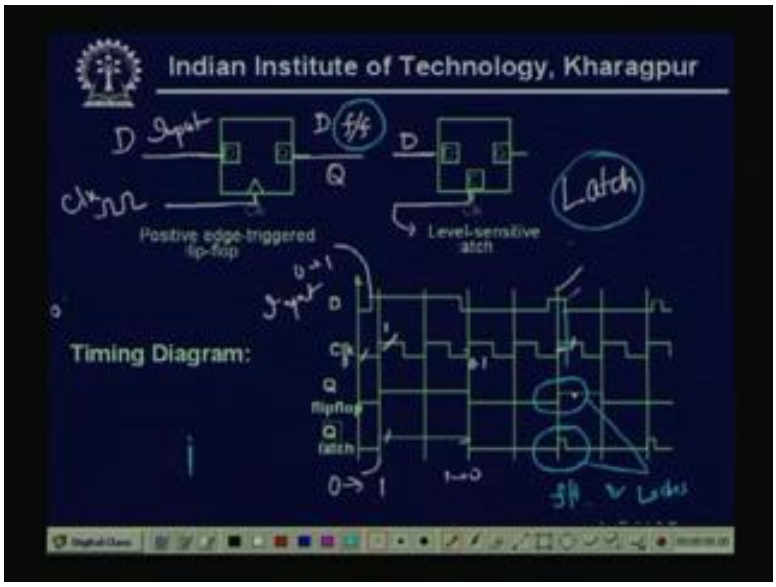

Now, again the D changes here the D changes at this position 0 to 1 the input changes input changes, but the clock here it is a level this is a 1 level, this is a 0 level. So, this is 1 this is 0 So, as it is a level sensitive, so the latch will it becomes 1, so the latch output becomes 0 to 1. Now, the similarly the D becomes slightly D becomes 1 to 0 slightly before the clock changes 0 to 1 see here also the clock level changes 0 to 1 level, so the first time that latch changes from 1 to 0.

See in this case, in this position the out output of flip flop and output of the latch are same. Now, if we see that the next data input, when the data input changes from 1 to 0 and 1 to 0, now at this position see this data becomes data is 1 data is one, but the latch say as it is a level sensitive. So, the when the clock becomes a 1 then only it is see this

position it is changes that means, I can write in this way. See here this data changes from 1 to data changes from 1 to 0 and data changes from 1 to 0. But see it is a clock level not the clock edge, but still the as it is a level sensitive, so as the level becomes 1. So, the D changes.

But, if we see the output of the flip flop as it is edge triggered and the edge have, edge has not changed the clock output edge has not changed. It becomes 1, so the Q flip flop is not changed. So, here there is no effect, so we consider this position and this position these two differs in flip flop and latches, here as edge has not changed. So, that is why it is unchanged as here edge has not changed, but level is 1, so as D changes that the latch output changes here.

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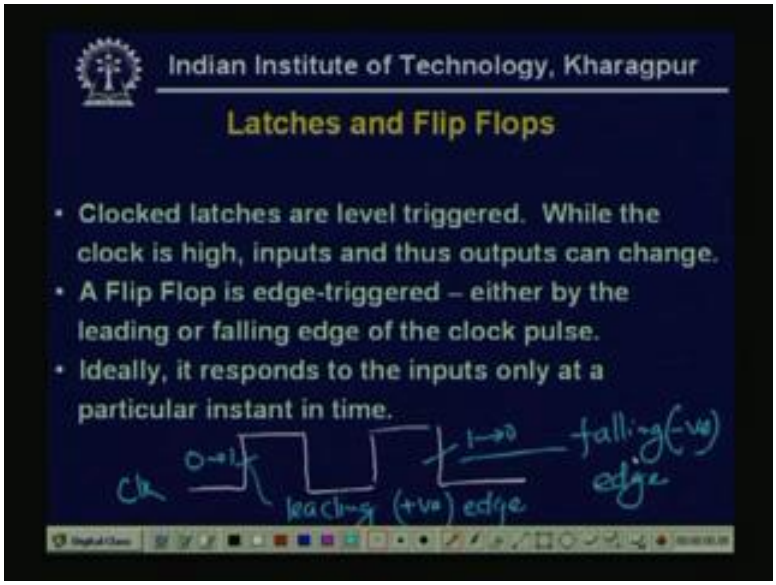

So, now clock latches are level triggered just now what we have seen, while the clock is high inputs and thus outputs can change. A flip flop is edge triggered either by leading or falling edge means the positive or negative edge-triggered of the clock pulse. Now, if it is a I take 1 clock this is 1 clock pulse. So, here in this edge the clock becomes 0 to 1, this we are calling the leading edge, this is leading edge or positive edge triggered. Here, this becomes 1 to 0 this we are calling the falling edge or negative edge triggered. Now, ideally it response to the inputs only at a particular instant of time.

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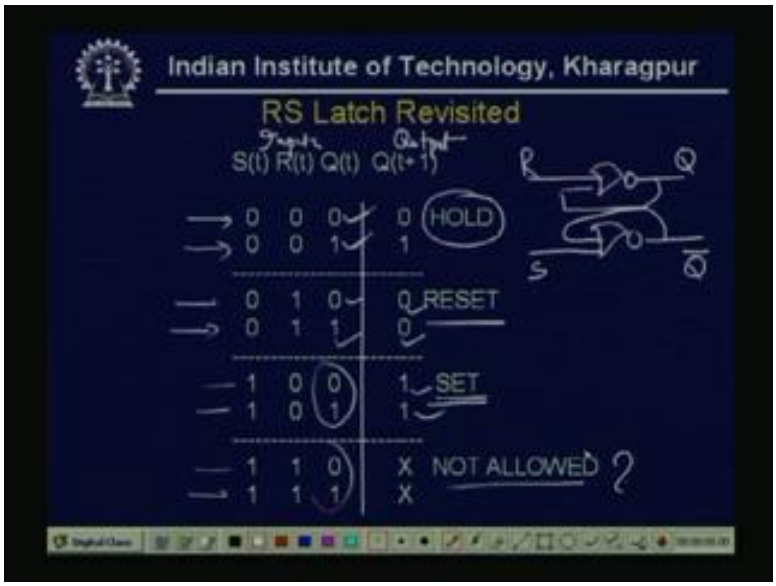

Now, again if we see the R S latch last day we have seen again if we remember the diagram. So, it was simply two NOR gates this is one R input, one is input another input is feedback this is Q and Q bar. It was the now if we draw the truth table, say that Q means the Q t and Q t plus 1 means say at any instant of time t we are considering the inputs of this. So, this is at 1 instant of time that this is my these are my inputs and this is the output, now both S and R 0 0 0 that time that state can be present state can be 0 or 1.

Now, whatever be the value we have seen that if R and S is both are 0 0 then the it should be the next state should be the present or current state, should be the previous state or next state, should be the present state that means this, is a hold condition. So, whatever the Q t value the Q t plus 1 value are the same that means, it is 0 and 1. Now, when S and R value 0 on 0 1 then if Q t is 0 that means, that presence at t'th instant of time thus Q value is 0 then output is 0. Even if it is 1, but the R S value 0 1 the output is 0, so this is my reset condition.

Similarly, when it is 1 0 whatever be the value of Q, the next state will be 1 and that we are defined as the set. If it is 1 1 whatever be the value of Qt then it is not allowed or last day we have define the undetectable or unpredictable the question given question was that means, it is not allowed. So, already last day we have seen this is of the truth table of the S R latch.

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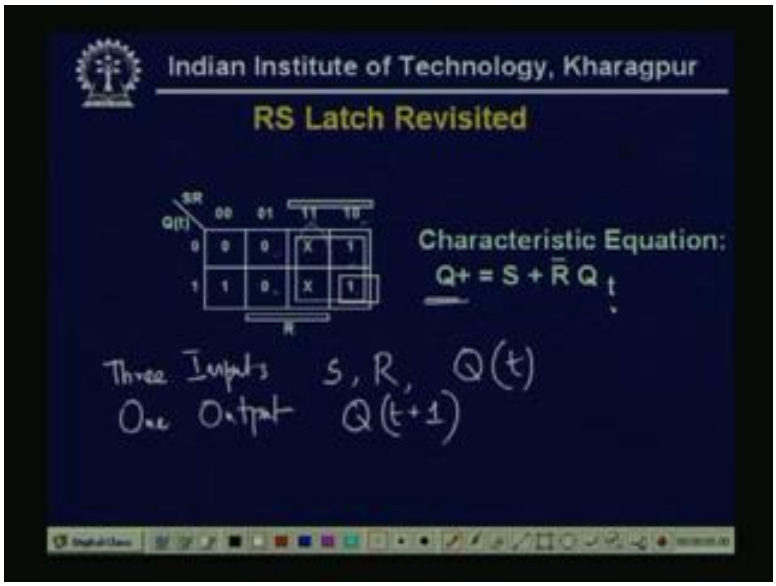

Now, if this input and output this truth table always we can draw a Karnaugh map for that. So, there are 3 inputs the S R and Q t and only 1 output Q t plus 1 say the next state. So, the if it is 0 0 0 just we put that value if it is 0 0 0 0 or 1 actually, Q t value is Qt plus 1 So, 0 1 this is 0 1, if it is S R is 0 1 always it should be 0 0, if it is 1 0 always it should be 1 1 and if it is 1 1 this is my cross means undefined other undetectable.

So, from here if we from the Karnaugh map we can derive the characteristic equation as, the next state or the or the next output is the S plus R compliment of Q t. Means, the next state will be the R 1 into the present state. So, this should be the characteristic equation of the SR latch.

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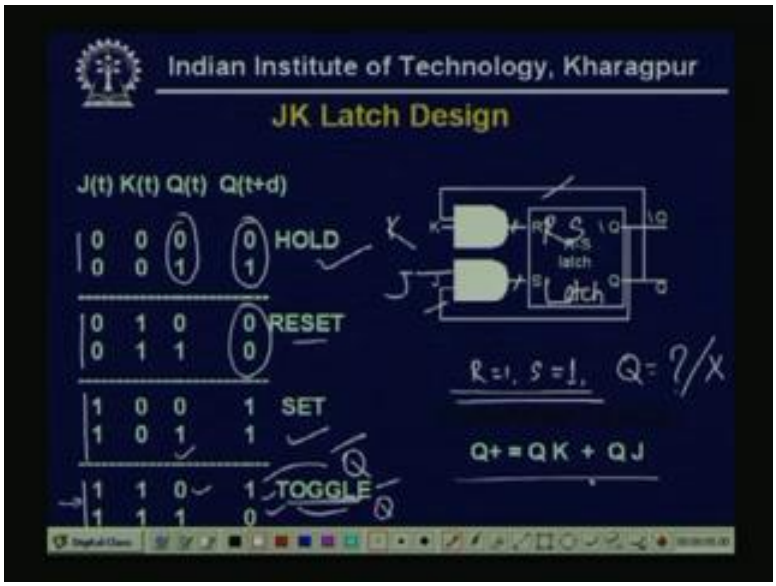

Now, we see another design of latch, so that we can avoid these confusing states. Now here the we have to fed the output in such a way, so that, never the input or the R S values can be 1 1, because what we have seen that if the if the R S value becomes 1. If my R equal to 1 and S equal to 1 then only this Q becomes unpredictable. Or, so we want to avoid this states we want to avoid, D flip flop is one simplest solution. Another simple solution is that J K, see here we have taken 2 inputs J and K and that is fed the two AND gate.

So, is this is these are my these are my J and this is my J and this is my K input, now here this 2 output of the and gate they are treated as the R S, R input and the S input. So, this now this becomes a RS latch this is my latch, so this is my RS latch. So, the output Q and Q bar that what we can do that output is feedback as the input of AND gate. So, this is 1 and the other output it is feedback through the input, so these are the this is the simple circuit.

Now, if we see the truth table of the J K latch then it has again J K has values 0 0 0 1 1 0 1 1 and for each of the cases this both the 1 0 0, the present state of the of the view we can tell that at the time instant t the Q value should be can be 0 1. Now, whatever be the case if it is 0 1 the Q t plus t means the next time it will be a 0 1, it is equals, so this is a hold state. Similarly, if it is a 0 1 0 1 then always it become 0 0 that is a reset state, if J K

value is 1 0 then whatever be, the value of Q it is a 1, so it is set now we see that what is when J K J equal to 1 and K equal to 1.

See if J equal to 1 and K equal to 1 then if the Q t value is 0, then actually this is 1 0. That means, when Q is 0 the next Qt plus t that next state will be 1, which is compliment of Q bar. Again when it is 1 it will be 0 that means, Q bar, so these we can see that this is a toggle means the compliment and characteristics equation will be that Q K plus Q bar J Q K plus Q J.

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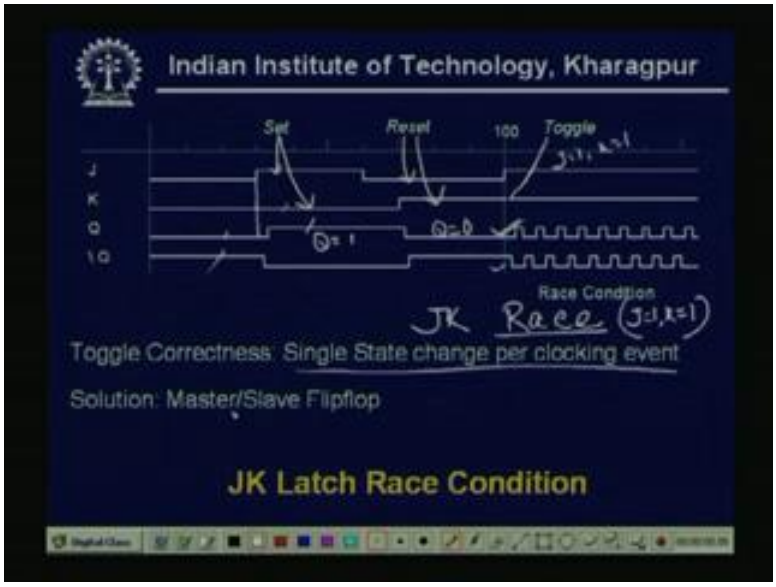

Now, if we see that the timing diagram of the or timing specification or timing diagram of the J K latch. Then see this is J input, so up to this time this becomes J becomes 0 and K is also 0, so Q becomes 0 this is 1 Q compliment. Now, see that J is 1 K is zero, so 1 0 means this is a set condition, so Q is 1, so this is a set, so this we can tell this is a set condition these two are giving a set. Now, when J is 0 and Q is K is 1 so that means, J is 0 and K is 1, so it will give Q equal to 0, so this is reset.

This is Q equal to 1 set this is Q equal to 0 reset, now J equal to 1 and K equal to 1, so this is the J equal to 1 K equal to 1. Now, see here what will happen that, Q becomes because it is the feedback, so that it will be 1 0 1 0 this type of thing will happen at both the because, it is a compliment of Q the 2 outputs are 1 is compliment of other. So, both will toggle means that it will be 1 0 0 1 1 0 1 0 1 0 1 0 like that, we define this as the that

race condition of J K, so this phase this is called the race when J equal to 1 K equal to 1 this will appear and this is called as J K race, means the output toggles.

Now, this is the single state change per single state change per clocking event and solution is another flip flop, so again we have to modify the circuit. So, that at J equal to 1 and K equal to 1 this situation will never happen that means, this J equal to this output should not be toggle and it is a master slave flip flop.

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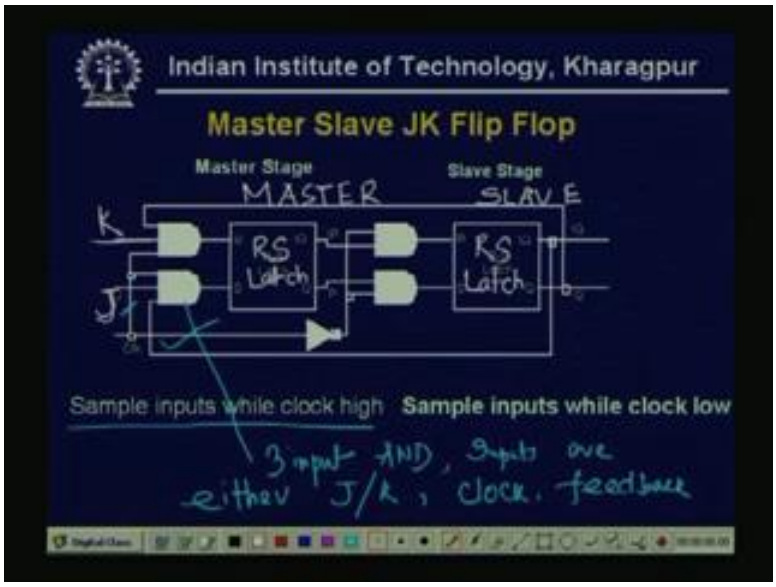

Now, we see the construction of master slave flip flop, so first we take 2 R S latch, so this is 1 R S latch. Now, again it has 2 inputs because it is 1 R S latch, so actually 2 J K flip flops are attached and the clock is see here this is very important portion that the clock is inverted. So, the first R S latch the clock feeds as it is whereas, for the second latch the clock is being inverted. And for this type of flip flop see the AND gate it is a 3 input AND gate instead of, so this is a 3 input AND gate instead of 2 input.

And the inputs are either J or K, the clock and the feedback, see if we this is this is the sample inputs while clock is high that means, it will be enables the input only when the clock becomes high. So, the first R S latch will take the input when clock is high, now see when this clock is high or when the first 1 is taking the inputs or it is operating. Then the second clock or the clock input of the second RS latch that becomes 0, because it is inverted. And if it is 0 if the clock is 0 then we know that from functions of R S latch that it will hold the previous state.

So, here when the first R S latch is operating, that it is second one is holding the previous state. Now, what will happen in the next time when this clock becomes negative or the clock becomes low. Then it will not… the first RS latch the input will not reach, but the second one as it is inverted for the second RS latch the clock input becomes high and as the clock input becomes high, so now, it will take the input from the previous R S latch. So, but the input of the second R S latch is the output of the first R S latch. So, that means, the output of the first R S latch or the output of the first latch is pass to the second R S latch and it is the output of the second one.

So, means that when 1 is operating another is latched and that is why it is called the first one is called the master stage this is a master flip flop. So, this latch is the master and this is the this latch is the slave. So, mainly that clock input is inverted when one clock is high. That means, 1 1 latch is being operated the second latch is holding the previous state, so this is the main concept of the master slave JK flip flop.

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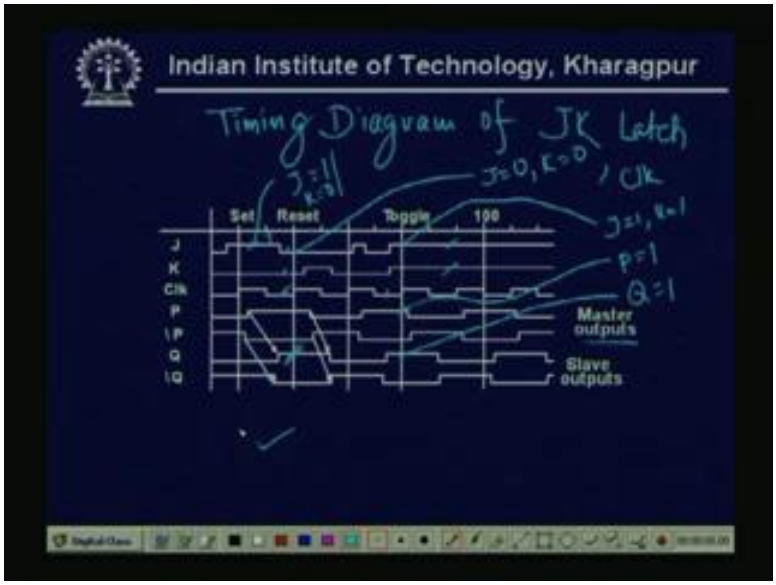

Now, again if we see the timing specification the timing diagram of J K latch then see that this is the J input the first one is taken as the J input, now second one is K input. So, here the J is 1 or take J is 1 K is 0, now as the clock is low whatever be the thing the clock is low, so which is a set condition. Now, here when clock becomes high this situation this condition that J is 0 here see here, better we see here, see this situation here J is 0 K is also 0 and that time that clock say that clock becomes 0 to 1.

So, here it is just before that the clock was 0 just before that, so here this is the situation when J is 0 k is 0 clock is 0, so it holds the previous one. So, what will be the value of Q, see here that Q becomes 1 that means, this is a reset Q and this is a Q compliment. That means, that that previous output or the output of the first latch this P first latch comes here and again the second output of the other output second output of the previous latch that comes here. Now, what will happen when J equal to 1 and K equal to 1, so just we see these condition.

See here J equal to 1 K equal to 1, so just before that clock was 0, now when the clock becomes 0 to 1 that means, it is a edge triggered. Now, the output of the first latch becomes 1, P becomes 1, now Q becomes 1 and here obviously, it is a compliment of it, so Q equal to 0. So, see that P and P compliment these are my master outputs and this, so the here that P equal to 1 and here Q equal to 1, now when P becomes 0 and still Q becomes 1.

And see here even the J and K are become 1 they are not changing the inputs are not changing. But these values are changing, see the input becomes stable the J equal to 1 and K equal to 1 they are fixed. But, still the output of the first latch that becomes 0 1 0 and the slave output also that is also that 1 0 1 in that way it is changing.

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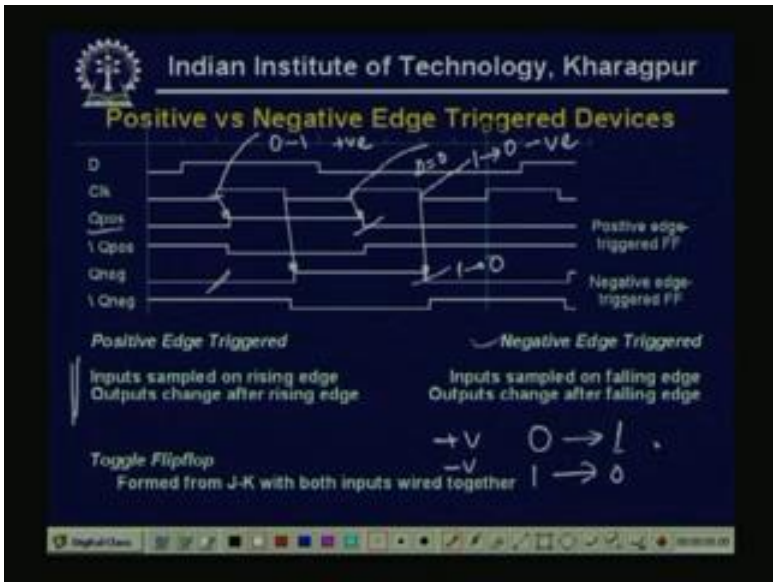

Now, already I have mention that flip flop is a edge triggered device, so that can be a positive edge triggered or it can be a negative edge triggered. So, now we see that what is

the positive and negative. So, if we consider a D flip flop then again that if it is a D this is my D flip flop. So, D becomes 0 to 1 and this clock becomes clock is 0 to 1 here clock becomes 0 to 1, so clock becomes 0 to 1 here this becomes 0 to 1 positive edge triggered.

Now, then only the Q see the output will change similarly, when the clock changes from 0 to 1 here then only the output will change. So, input sample on rising edge and outputs change after rising edge this is this has been shown here rising edge is a positive edge. Now, if it is a negative edge triggered the input sample on falling edge see here this is a falling edge means. Here this is a clock 1 to 0 and then that for the negative say if it is a negative say here it is not it is not changing.

So, for negative even it is a 0 to 1 the clock has changed here, but the negative edge it is changed it has not changed, again the output has not changed here. But, when it is a when it is a 1 to 0 that means, this is my negative edge triggered then the D chain D becomes here, D is 0 and the clock as the clock changes. So, the negative edge triggered output, negative edge triggered flip flop or the output of the negative edge triggered flip flop has been changed from 1 to 0.

So, for positive edge triggered flip flop only from 0 to when it will be 0 to 1 the output will change. When for the negative edge triggered negative edge triggered if it is 1 to 0 then the output will change.

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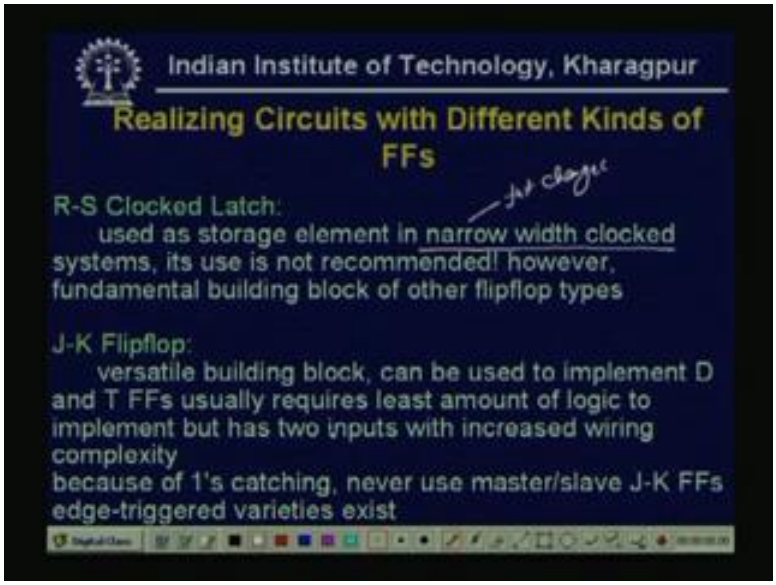

Now, so far we have discuss the different type of latch and the flip flop and now, if we summarize we see that in real life circuits what are the different kinds of flip flops are being used to realize the large circuit. So, first we have seen that 1 is that RS clocked latch, so this is used as storage element in narrow with clock systems, where it narrow width means it is a it first changes or the memory if it is a memory or storage where it keeps only for a small time. So, its use is not recommended however, fundamental building block of other flip flop types, so just for some alarm, so it can be used, so only for narrow width clocked it can be used.

Now, the JK flip flop it is versatile building block and can be use to implement D and T flip flop usually request least amount of logic to implement, but has 2 inputs with increased wiring complexity. So, because of 1's catching never uses master slave JK flip flops and this is edge-triggered varieties exist. So, normal J K flip flops can be used as D flip flop and T flip flop and that is the main use.

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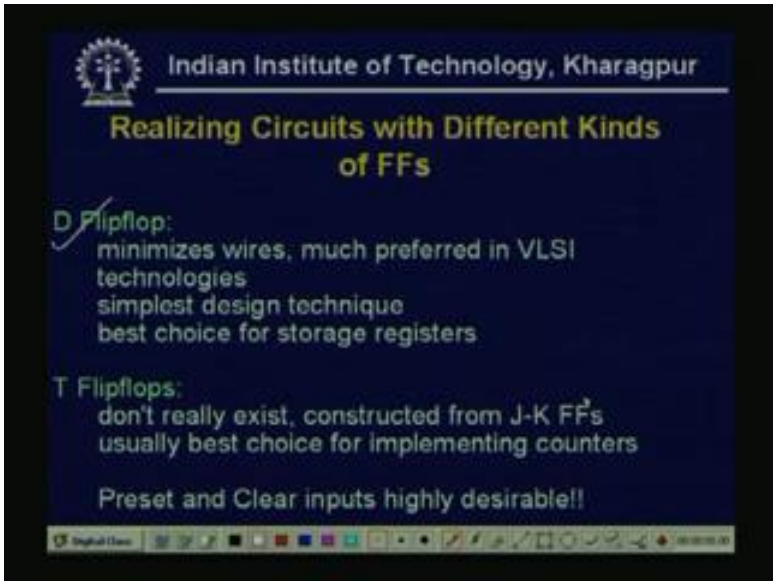

Now, the simple D flip flop, so it minimizes wire because we have seen that it is it is a simplest kind much preferred in VLSI technologies. Because it is very efficient and takes very less hardware simplest design technique and best choice for storage registers. That means, for one bit storage this is the number 1 the D flip flop. Normally, T flip flops do not really exist this is the, same flip flops means a toggle type of flip flops and, but

constructed from JK flip flops, because we have seen that JK flip flop mainly toggles and usually best choice for implementing counters.

Normally, for whatever be the type we reset and clear that means, one reset and the clear inputs are highly desirable. So, whatever the flip flop implementation or whatever type of flip flop we use that we prefer that one clear line and one reset line.

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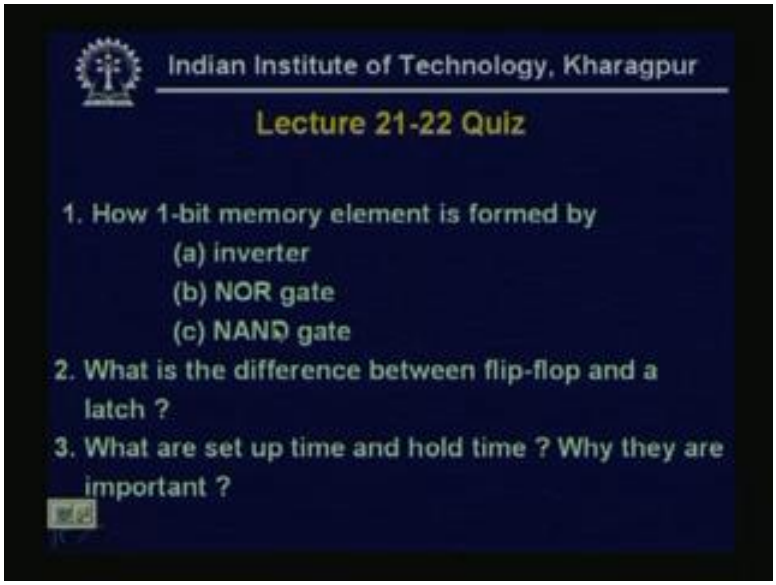

So, now the today's lecture and the last day's lecture there can be some of the quiz questions, that how one bit memory element is formed by inverter NOR gate and NAND gate. The second question is what is the difference between flip flop and a latch? What are the setup time and hold time? And why they are important in real life circuitry? So, these are the three quiz questions that are mainly based on the last 2 lectures. Here, we end the class.

Thank you.

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Lecture - 23
Design of Registers and Counters

Last day, we have learned how to design the different type of flip flops the D flip flops RS flip flop the JK flip flop and what is that problem or what are the advantages and disadvantages of different type of flip flops. Now today, we will see how the more complex equations circuits can be designed using the different type of flip flops.

Now, this more complex sequential circuits they contain mainly the registers and counters shifters mainly the storage elements. So, first we see the design of registers and counters in this lecture.

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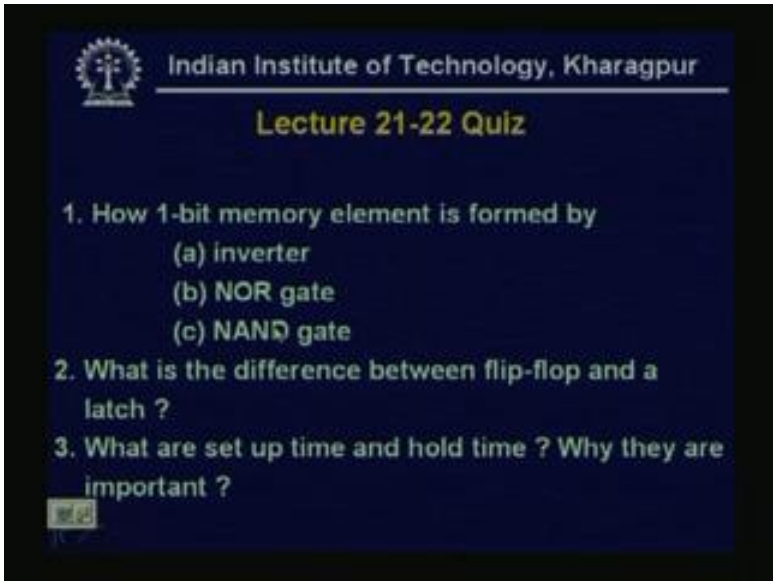

Before that, we quickly see the answers of the quiz questions based on that lecture 21 and 22. Now, the first question was the how one bit memory element is formed by inverter NOR gate NAND gate, we have read in the last lecture that.

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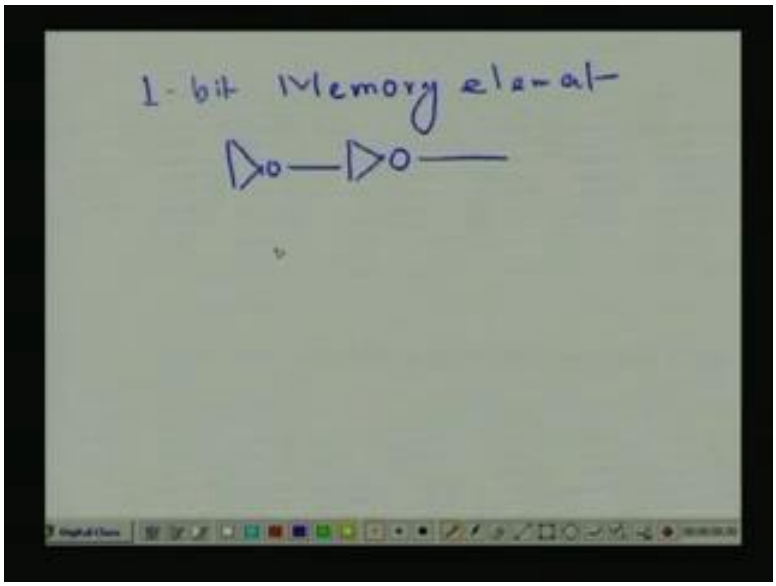

The one bit memory element that is by using inverter one NAND gate and if it is cascaded with another inverter that means, 1 NOT gate and another NOT gate.