Digital System Design
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Lecture - 20
Logic Design with PLA

Today, we will continue the discussion that last day. We are doing mainly the logic design with programmable arrays.

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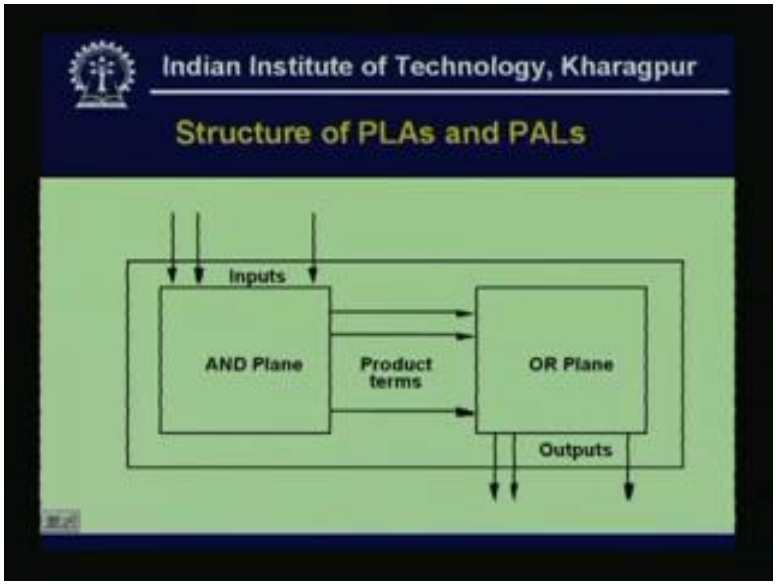

Now today, we will see that the logic design with PLA's, Last time, we have seen that mainly the programmable arrays or programmable array logics can be constructed by defining two planes the AND plane OR plane. The AND plane generates the all the product terms and the product terms are fed to the OR plane, OR plane generates the output.

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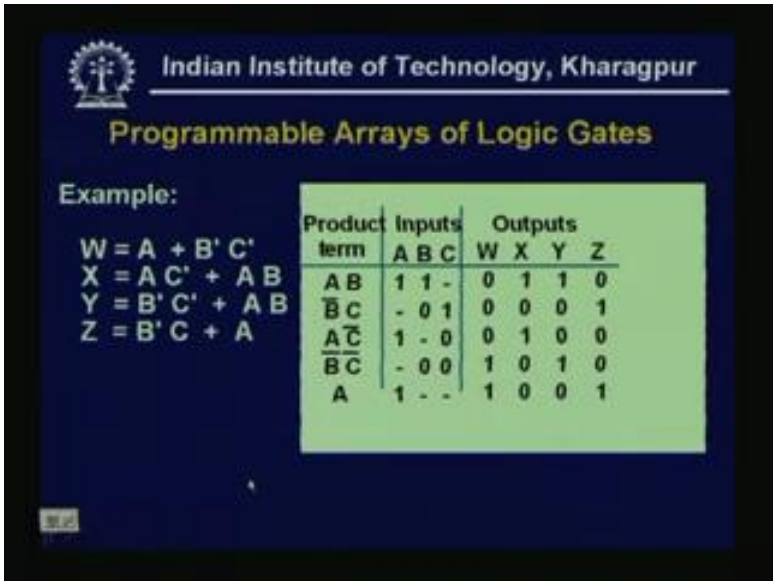

We discuss this particular example and we have seen, how it realizes the different output expressions.

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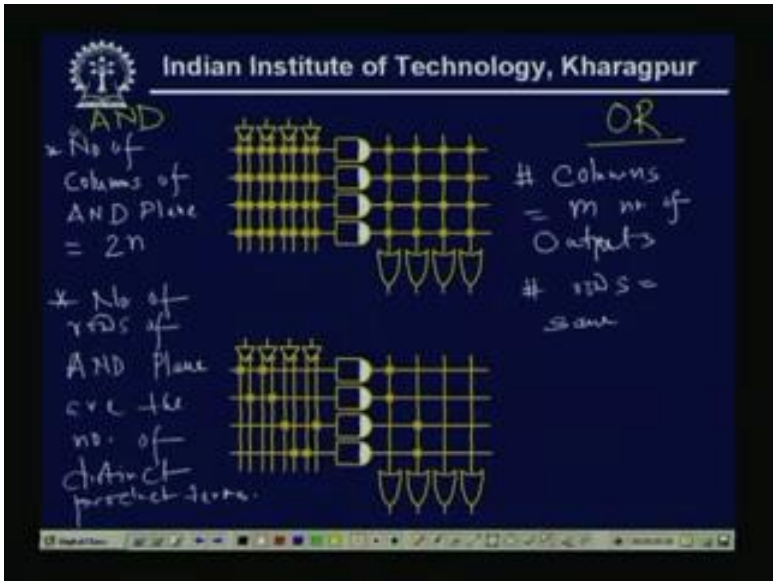

This is the overall structure of AND plane and OR plane, that particular example this should be the realization. Now, what we are discussing that alternative representation of the AND plane and the OR plane. See here that AND plane, if is a n variable input, what we have seen, that if it a n variable input, then the number of columns of AND plane number of columns of AND plane equal to 2 n.

And, the number of rows of AND plane are the distinct or the number of distinct product terms. So, this is for my AND plane for my OR plane the number of columns and the number of output say m number of outputs. The number of row are same, it is the distinct number of product terms now these are same.

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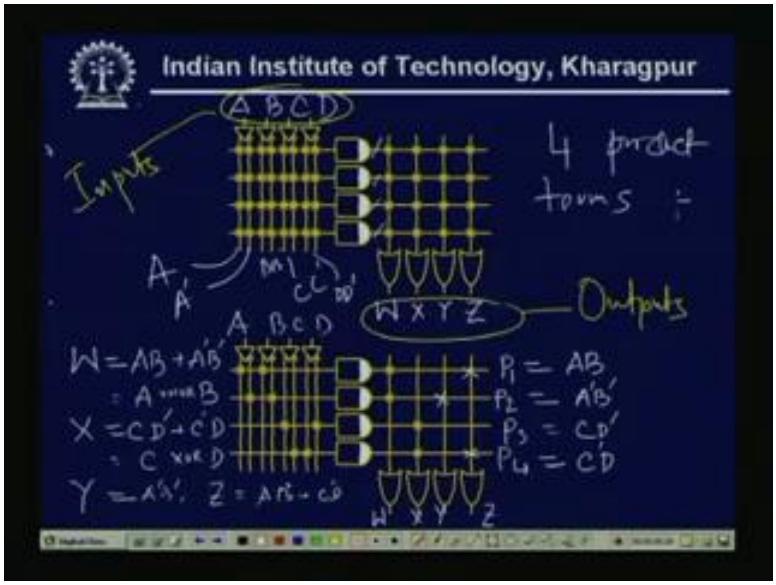

Now, if we can represent this thing alternate way, say these are my 4 variable input. So, if the inputs are say A B C D, then actually this is the A input and this is A compliment. Similarly, B B compliment C C compliment like that and D D complement, see here the number of product terms are only 4, because there are 4 AND gates are given. So, these are my four rows it means that four product terms and there are four output because there are in the OR plane there are 4 columns. Say these are W X Y Z, these are my outputs and this A B C D are my inputs.

Now, if I take a particular example, then see what this circuit realizes, say again if we see that this is my A B C D, then the first AND gate output or the first product terms that P 1 equal to this is AB. Then the second product terms P 2 equal to this is A bar B bar, third product terms is CD bar. So, P 3 equal to CD bar, P 4 is equal to C bar D.

Now, if represent the four outputs are W X Y and Z, then what will be the W X Y X representation, W will be equal to say these are in 1 column, if 2 cross or 2 1 exist means we have to consider these 2 product terms P 1 and P 2. That means, this is AB plus A bar B bar which is nothing but, A XNOR B, X is P 3, P 4 means CD bar plus C bar D which is nothing but C XOR D, Y is say there is no Y.

Similarly, there is no Z, because the product terms here there is no product term is selected. So, Y and Z is not their; that means, here there are only for this circuit there are only two outputs, but if say this is 1 1 cross is here that means, 1 1 exist. Then, obviously, Y equal to P 2 means only A bar B bar. Similarly, if 1 Z is Z line in the Z column that the crosses are there in P 1 product line and P 4 product line, then this is Z is AB plus C bar D. So, this is the way that, how we realize the logic function using PLA.

Or the reverse thing we have discuss that given this PLA this PLA is actually realizes the four outputs W X Y Z and these outputs are W is XNOR B X is C XOR D and if the some YZ and like that. So, what we have seen that not only that 1 complex combinational function, but also the simple gates can also be realized by using PLA.

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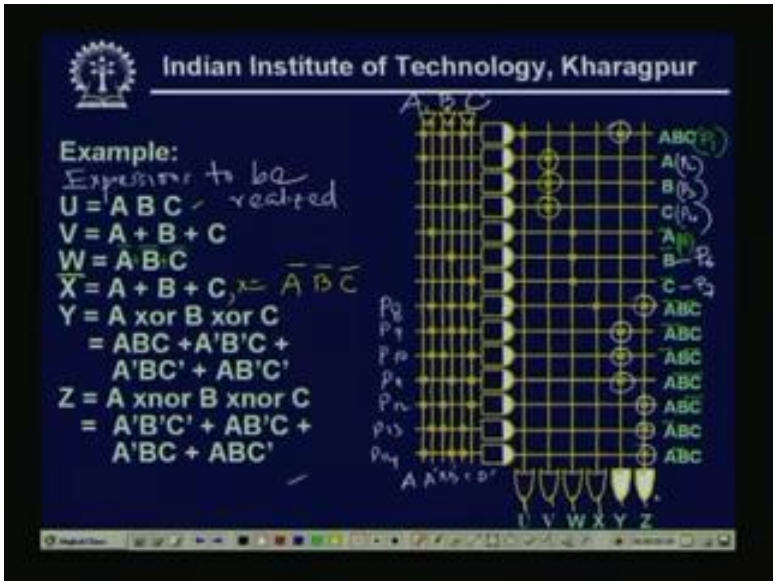

Now, we take one example, one slightly bigger example, see there are six output functions to be realized using PLA and the outputs or the expressions are given like that, so these are my expression to be realized. Now, the first expression we study and we see that there are only three inputs A B C, so in the AND plane there will be 6 columns and these are A B C. And that means, A complement AA complement B B complement CC complement this 6 columns are there in the AND plane.

See, how many distinct min terms are their here, see here there are 1 2 3 4 again this is common. So, 4 this is common, 4 min terms and here this is common and 3 7 and here 4 another 4, so there will be 11 min terms.

So now, we have given some more we see that, what are the distinct min terms are there, see first is that our first 1 is A B C, this min terms is my ABC. Second the product terms we can tell so my P 1 equal to this is my P 1, P 2 is simple A, P 3 is B, P 4 is C. Now, P 5 is A complement this is my P 5, P 6 is B complement, this is my P 6, P 7 is C complement.

Now, P 8 is see A bar B bar C bar, this is A bar B bar C bar, similarly P 9 is A bar B bar C A bar B bar C. Next 1 is A bar B C or A bar B C bar A bar B C bar, this line, this product term is A this is B bar and this is C bar, A B bar C bar, this is A, this is B and this is C bar, so A B C bar. Next is A A bar BC A bar BC, last 1 is A A, this is B bar and this is C, AB bar C, so these are my product terms. So, this is P 7 this is my P 8 P 9 P 10 P 11 P 12 P 13 and P 14, so 14 product lines are their; that means, 14 rows.

Now, there are six outputs say first we see that U is ABC only one product terms. So, that is only P 1 and that this is my this is my U. V is A plus B plus C, so there will be 3 cross or 3 ones. So, this is A A B C and this is my V equal to A plus B plus C, W is again ABC. So, again W is A complement here, we see the W is A bar A bar plus B bar plus C bar. So, actually it will be A bar plus B bar plus C bar this will be my W.

X is A bar B bar C bar only 1 term and that is A bar B bar C bar, so X is actually this is A plus B plus C, because if I take that X complement that will be ABC. So, what we can give that, X is A bar B bar C bar or X complement is what we can write this, X complement is A plus B plus C.

Now, Y is A XOR B XOR C, A XOR B XOR C if we break or if we apply the rules, then it is actually ABC plus A bar B bar C plus A bar BC bar plus AB bar C bar. We know that this is actually the sum of full adder. Now, see that how it realizes the Y, see that Y is see A bar BC A bar B bar C A bar BC bar AB bar C bar and ABC. So, Y is nothing but A XOR B XOR C the three inputs XOR.

And, Z is is AB C bar A bar BC AB bar C and A bar B bar C bar which is nothing but A XNOR B XNOR C the three input XNOR. So, Y and Z represents or realizes three input XOR and 3 input XNOR respectively. So, this is one example that, how we three variable function, or a set of three variable function can be realized.

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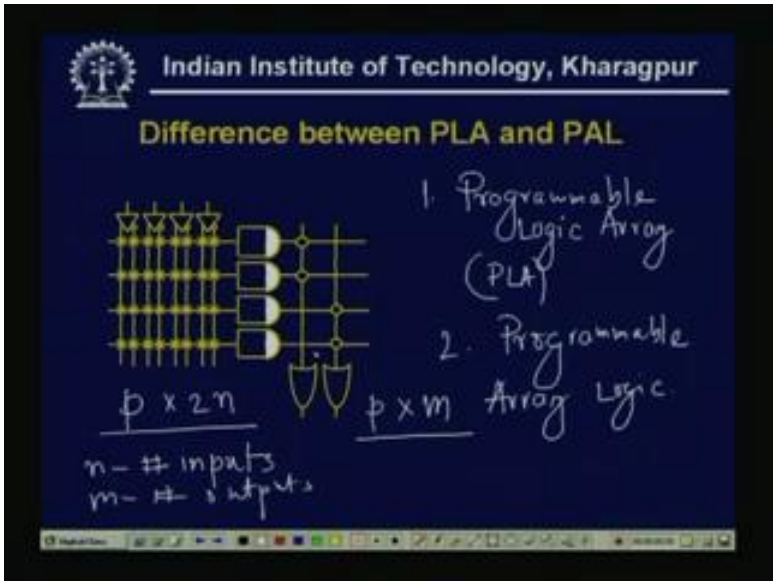

Now, we have two different type of programmable array logic 1 is called the programmable logic array, programmable array logic or PLA and another is programmable. Now, what is the difference between two, so far we have discussed, where both the AND planes and OR planes can be programmed. Tat means given some n input lines or 12 number of columns in the AND gate and say the different product terms can be P, then the AND plane size is AND plane size is P by P by 2 n.

And, the OR plane size is say P by m, where n is the number of input variable and m is number of output variable outputs. So, both are both can be programmed. Now, if it is restricted that only the AND plane can be programmed, but the OR plane is very much restricted, means the one output can only take a particular combination of the set up product terms. Then, means, the AND plane is programmed, but the OR plane is fixed then it is called a programmable array logic PAL. So, the difference is when both AND plane and OR plane are programmed we called this is a PLA and if it is for PLA.

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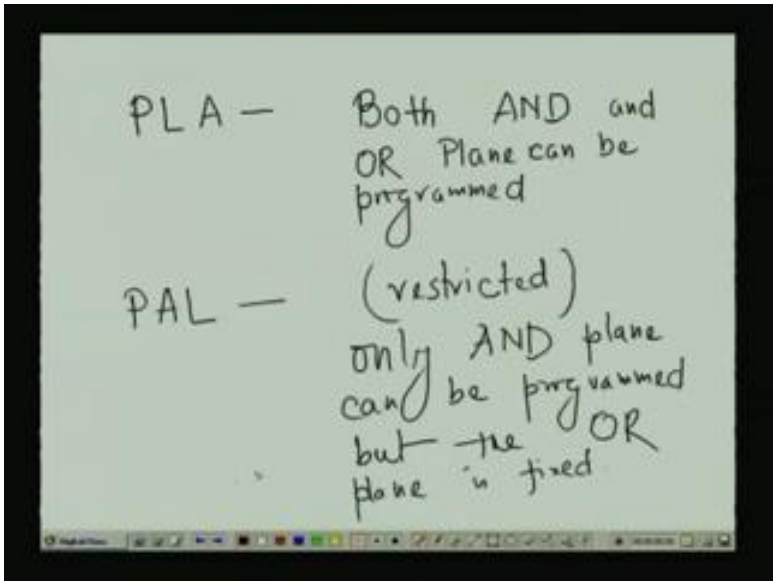

PLA, both AND and OR plane can be programmed whereas for PAL it is a restricted design or restricted with respect to the PLA mean only AND plane can be programmed, but the OR plane is fixed. So, this is one this type of structure.

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A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Now, we take another real life example that BCD to gray code converter, already we heave discuss this example and the output functions are realized in different way. Now, if there are 4 bit inputs A B C D, the outputs will be that between every pair that there will be a unit distance code and the gray code will be it is shown in this way. Now, there

are four outputs, so if I use that Karno maps for realizing that, what will be my function for W X and Y and Z, so we will see that for W there are five ones.

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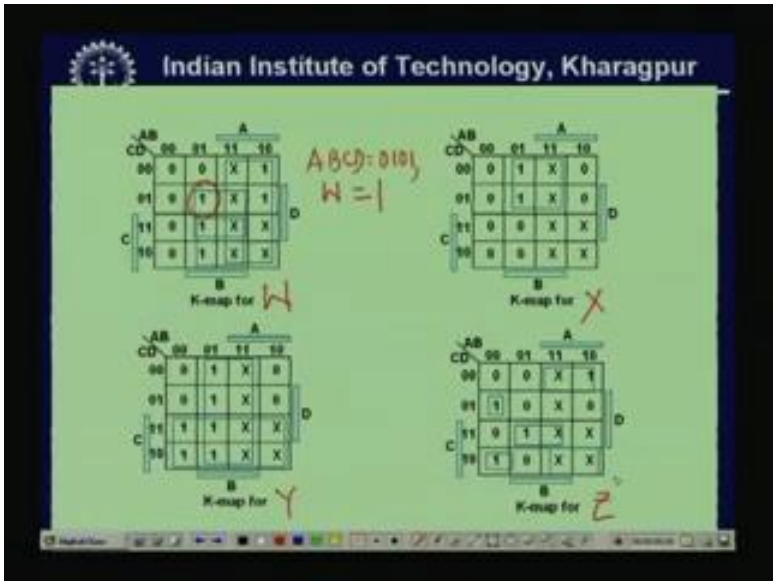

And see this is for my K map for W, see these are the five ones. That means, when A B C D value are when A B C D value are 0 1 0 0 say this 1 or or say 0 1 0 1 take. Then, my W equal to 1. Similarly, when that A B C D is 0 1 1 1, W is 1, this is 0 1 1 0, then W is 1. In that way, we can just proved the, or we can draw the Karno map for W, similarly we can draw the Karno map for X Y and Z.

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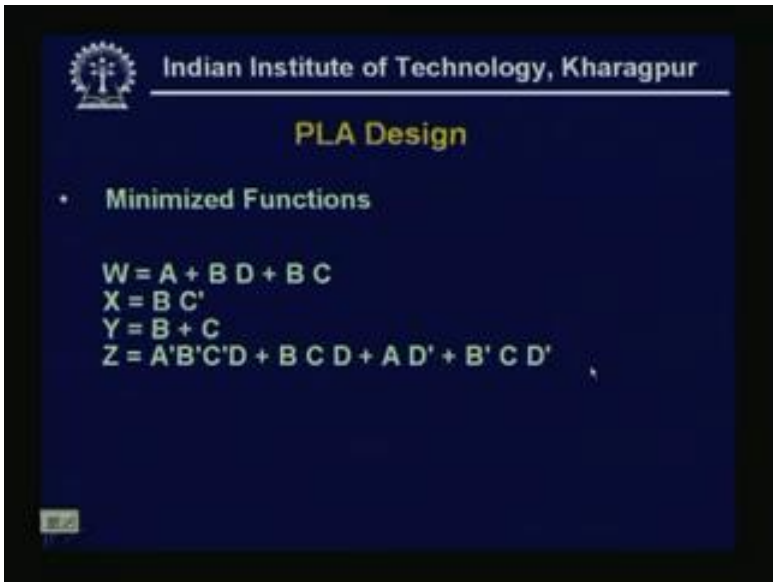

Now, if we realize or if we minimize the functions then we will get the solution as. Now, if we realize or if we minimize the functions then we will get the solution as the W is A plus BD plus BC by minimizing the Karno maps, X is BC dash Y is B plus C, because we will be getting here.

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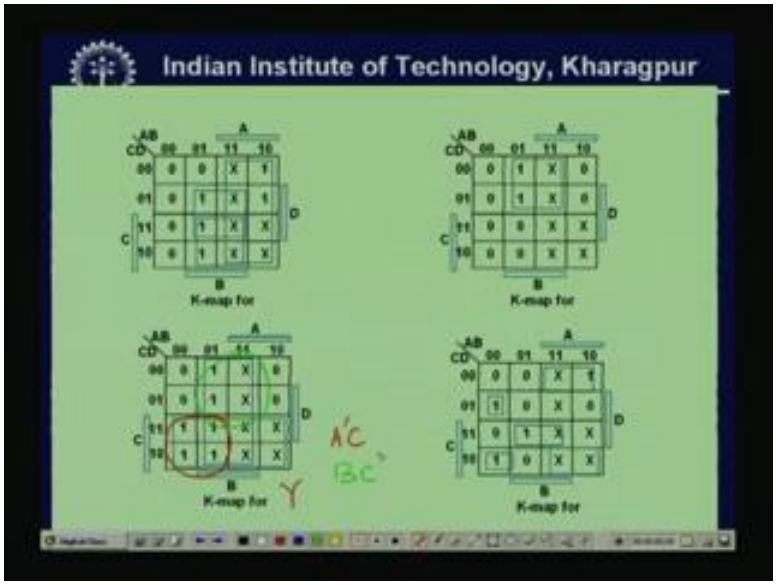

See for that for K map for Y actually we have given here it is a what, this will be that A bar for this column it will be A bar and this is for C. Similarly, if we take this one part these are 2 do not case, then will be getting that B and C bar.

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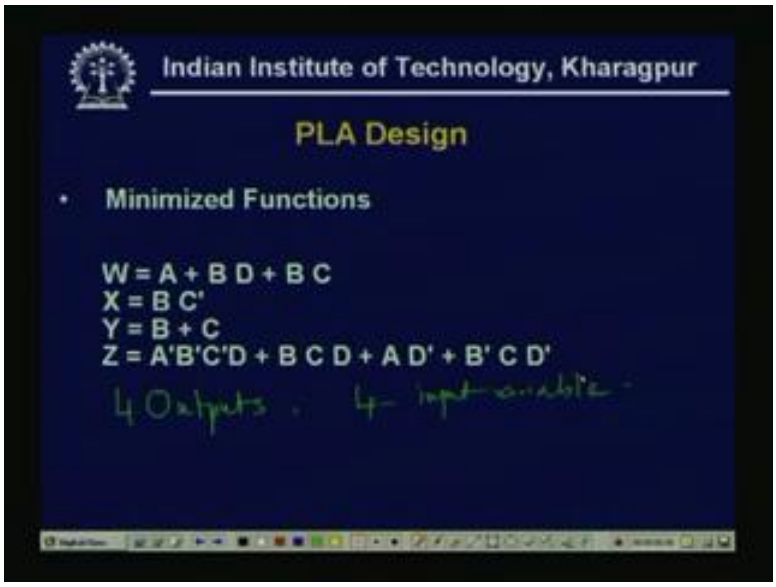

Now similarly, the Z will be getting that A bar B bar C bar D plus BCD plus AD bar plus B bar CD bar. Now, if we mainly that this is now will becomes a very simple function that there are four outputs. So, there are four outputs this A B C D, four input variable functions.

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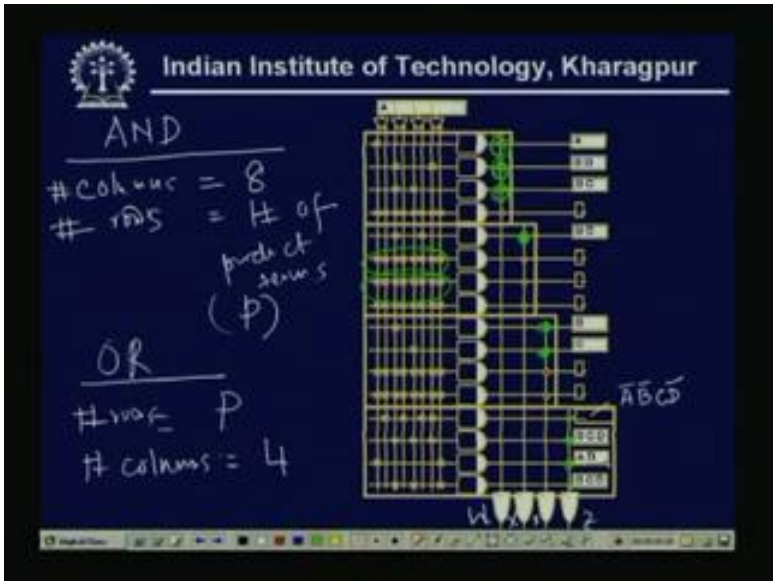

Now, how we can design the PLA, see there are four inputs the for the AND plane if we see the AND plane. Then the columns 8, number of rows the actually the number of different or distinct product term it can be more, but at least we need the different number of distinct product terms say P.

Now for OR plane, the number of rows are same P and number of columns are output, there are four outputs. Now, if we see that the W X Y Z, W is A plus BD plus BC, so this is W X Y and Z. Now, what will be W, W is A plus BD plus BC, we see that OR input is actually this is a three input OR and this will be that A BD and BC, these three product terms will be the three inputs of the OR gate which whose output is W. Similarly, the X is simple BC dash. So, X will be simply BC dash. So, it will be only one line BC dash, see here, actually all possible combinations are kept and see it it does not realizes any product terms, similarly these also. This is actually only one single input.

Then, it is B plus C. So, X is simple B plus C and Z is AB A dash B dash C dash D BCD. So, Z is BCD AD bar BCD bar and this is C A bar B bar C bar D bar means this is my A bar B bar C bar A bar B bar CD bar now C bar D. So, these will be the A A bar B bar CD bar, so Z is the sum of this four terms, so this is the PLA realization or the design

of BCD to gray code converter using the PLA design. Now, another array type of structure that that is also programmable that can be used for the logic design the combination circuits and this is nothing but a memory.

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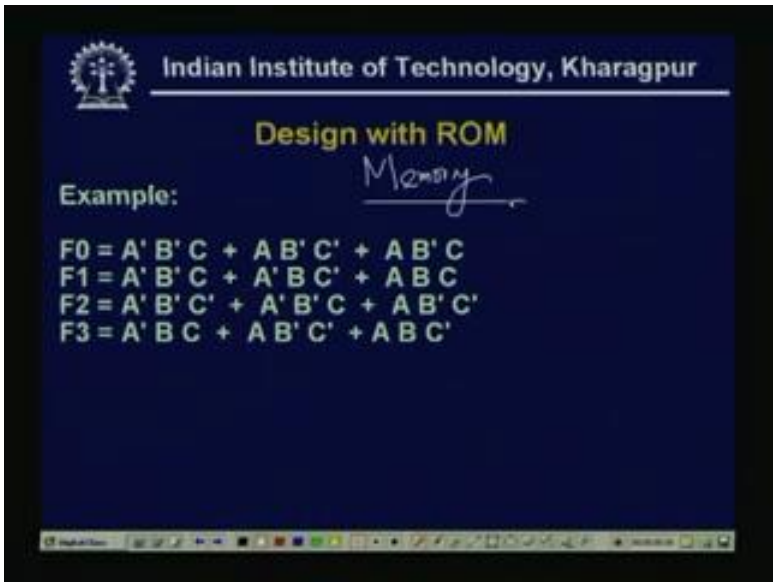

So, we will see that, how memory can be used as the logic design. Again here we have seen, we have taken three variable examples having four output expression of it and we will see how this can be designed using a memory.

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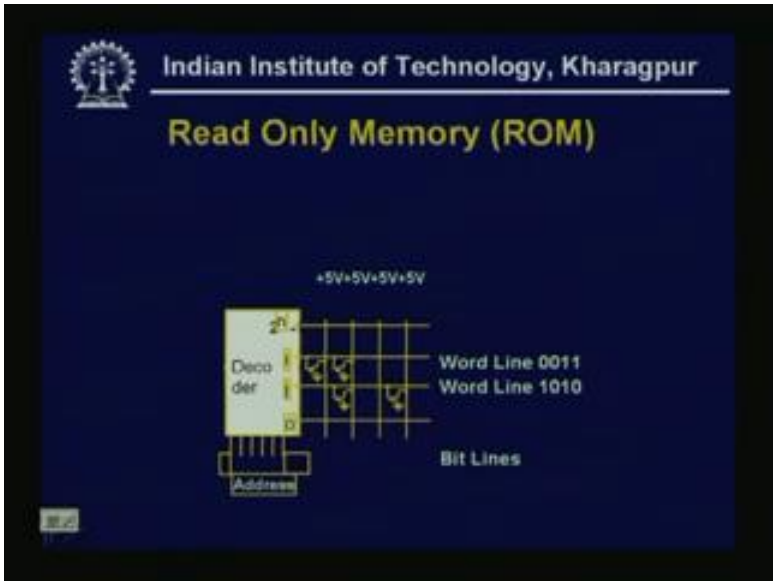

But before that, we see that how the memory structure is so normally this is a read only memory. See that here, there are some decoder lines where the decoder input are the memory addresses. That means, say if we if we write in this way.

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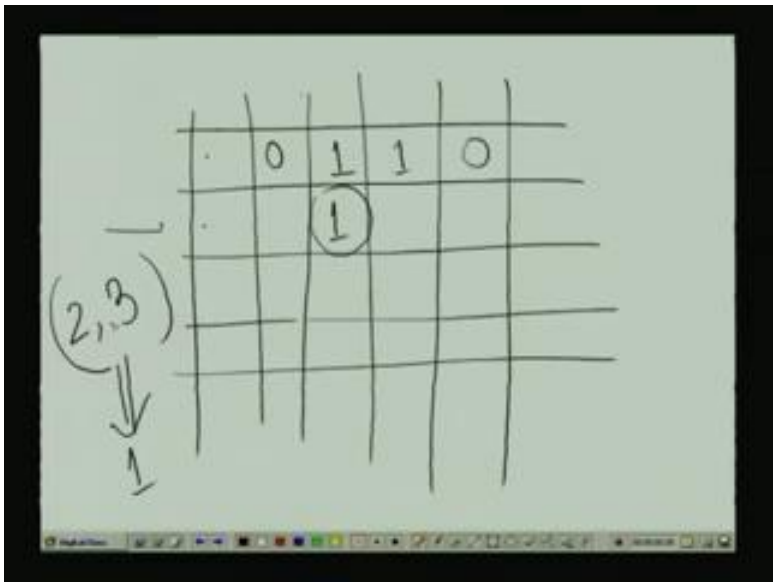

As if this is two dimensional structures again the 2 D arrays, say there are 2 D arrays and say here either 0 or 1 are kept in each element. Now, why we are calling this is a memory, because if 1 is here, I can select this by taking the row and column. Say this is my matrix type of form say this is second row and third column; that means, second 2 3, second row and third column it will give one output the content of this thing. Now, these we are calling this 2 3 determines the position of that particular element that we are telling as we are define as the address.

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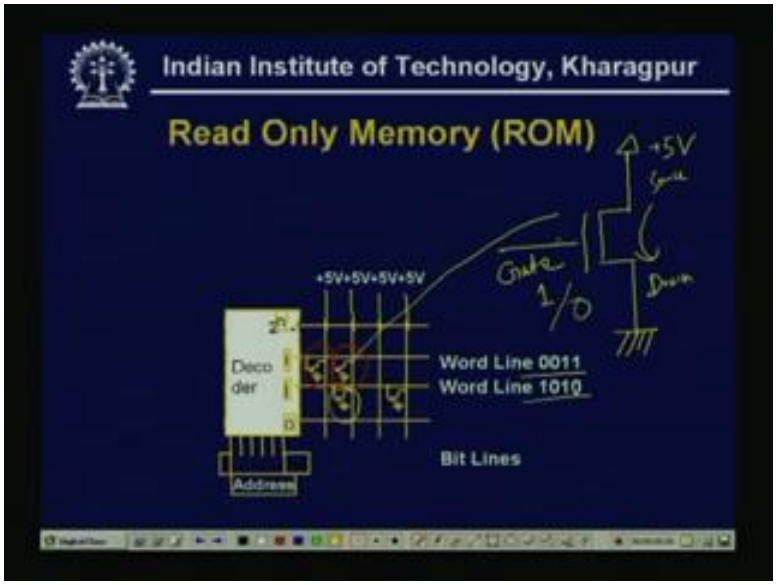

See here, these are the addresses and if it is n address lines, then this will be a 0 to 2 the power n minus 1 that many number of output lines. Now, this output lines they are called as word line, they are see here this is a word line 0 0 1 1 means that here, this is will be treated as 0, this will be treated as 0 or 0 0 1 1. So, this will be actually this column lines they are connected to 5 volt supply all are connected to 5 volt supply.

So, this is a one, so this connection if we draw this will be like that say as if one transistor is here, this is a plus 5 volt supply. Now, this is called the source and drain and this is gate. Now, if we apply the gate as 1, then it will be connected. If it is 0, then it will not be connected; that means, it is a open thing.

So, see if now this is that I is applied to this line is 1, then actually this transistor is 1, we get 0 again. Here, we get a 0 otherwise it will be a direct 1 and 1 line, so this will be a word line 0 0 1 1. Similarly, for this word line, it is called this is 1, this is 0 1 0 1 0, this is 1 0 1 0.

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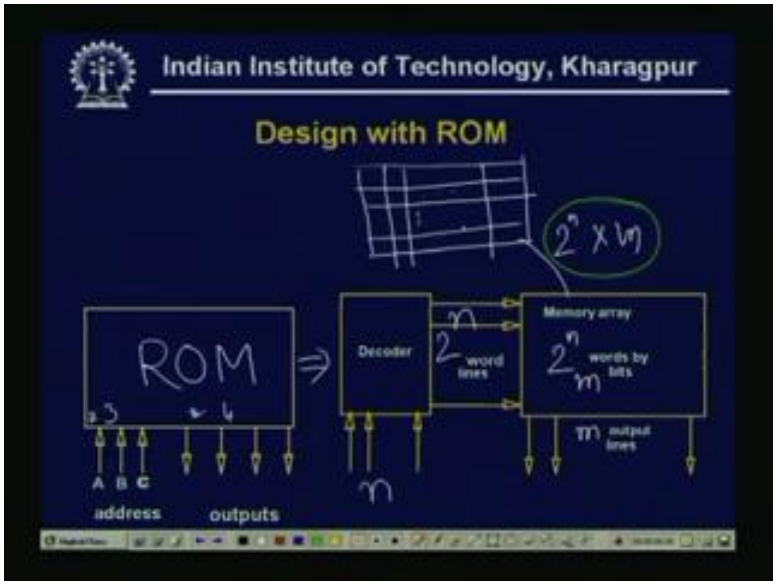

Now in this way, we can define that the ROM structure, now how this ROM can be used for the designing circuit, say this is my ROM with three inputs and four outputs. Now, this can be first this can be realized as if it is a decoder. So, decoder input is n the number of word lines are 2 to the power n and this is a 2 to the power n words by m that many number of bits if it is has m output lines. So, if we see actually here, there are 2 to the power n by m that many number of words are there.

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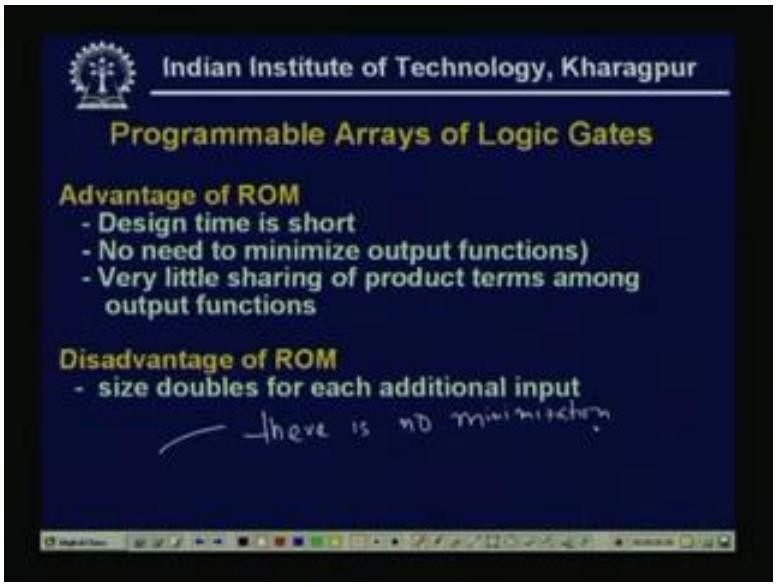

Now, the programmable arrays of logic gates, see that advantage of ROM is that design time is short and no need to minimize output functions. It is a very little sharing of

product terms among output functions. See here, that actually all the min terms or all the products terms are exist, so there is no need to minimize the output function.

And here, it is very because all possible combinations or all possible, outputs are available in the arrays, what we are calling that memory. Then very little sharing of product terms among output functions are necessary or actually it will it is done. Now, the disadvantage of ROM is that its size doubles for each additional input, why, because as there is no minimization. So for, ROM actually there is no minimization, so the product terms are almost not shared.

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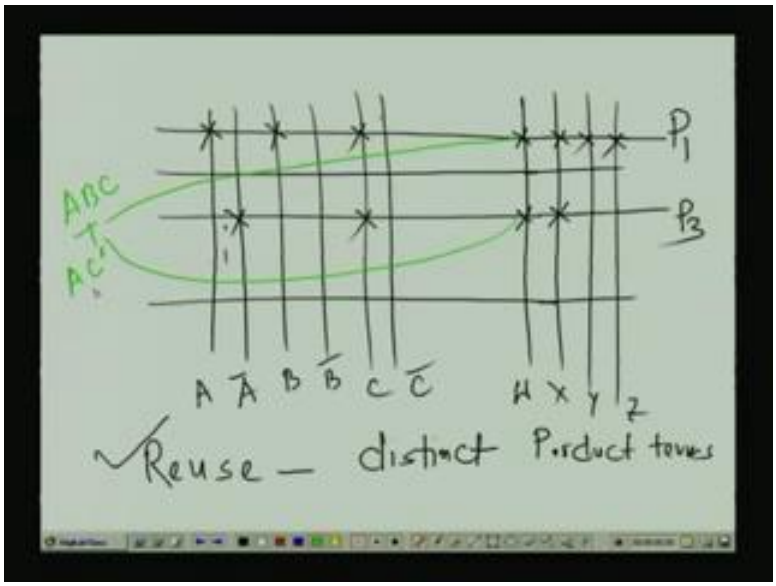

See, why this is happen in, see I have in the PLA type o structure PLA type of structure or whatever we call the PAL or PLA. Actually this is a reuse why see here if it is three input. So, I have 6 such column and why we are telling this is a reuse, because I am taking the distinct product terms; that means, only the product terms for say for all m outputs. Say, if I have 4 W X Y Z these four outputs are there, then one product term can be shared by each output and these we are calling the reuse of product terms or reuse of min terms.

See that say ABC, this A B C this is my first product term P 1, now W can use this product term ABC, X can use this product term ABC, Y can use the same product term, Z can also use the same product terms, because the output lines are actually the columns the vertical lines. So, they are not affected if in 1 row that all possible ones are there.

So, similarly say another say a compliment C, this is my say P 3, so A complement C can be used by again X or W. Now in this situation, W is actually the sum of the ABC plus A C complement, now this ABC or this P 3 can be used or can be shared by X. Now, what we are seeing, that is the column 1 cross point or the multiple cross point in 1 column means that it is a sharing of the product terms.

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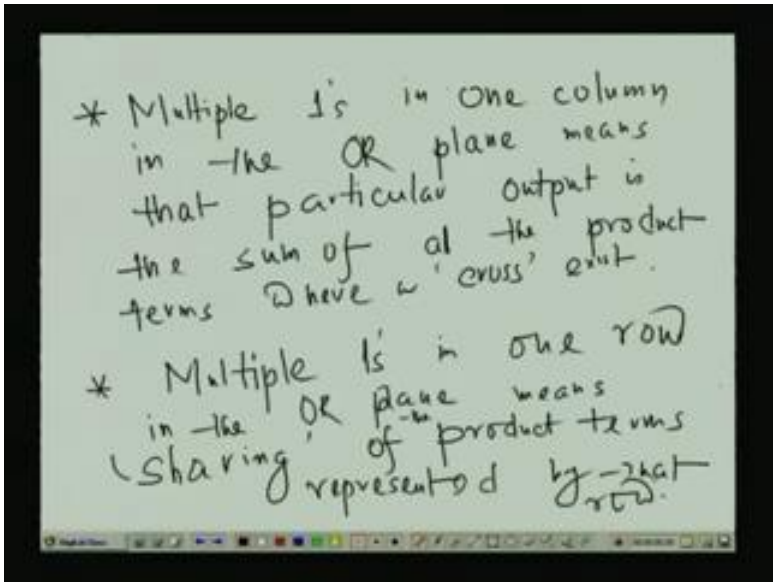

So, what we are we have discussed in the last class also, that the multiple ones in the or in one column in the OR plane means that particular output is the sum of all the product term, where a cross exist. But, multiple ones in one row in the OR plane means; that means, the sharing of that product terms represented by that row.

In the last class already we have discussed, that one cross point in the rows in a AND plane or one cross point in the column in 1 AND plane means what? So this is for the PLA's and PAL's that where both the AND plane and OR plane are programmed.

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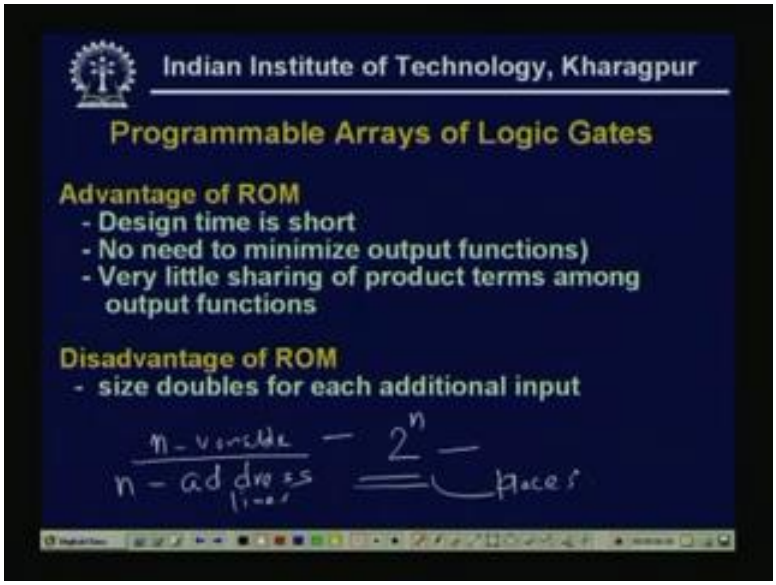

So, what we have, that actually that in the AND plane or in the OR plane. That means, PLA's or PAL's that only that product terms which we need or which exist in that set of particular expressions to be realized only depending on that array size should be taken or the number of rows or number of columns that will be selected.

Now for ROM, because this is a storage type of thing. So, here for a particular inputs or number of inputs that all possible, output adjust lines should be there. That means, if it is a n variable we know that if it is for a n variable function or n input you can tell. Then, this all 2 to the power n also to the power n products or this time this means that all this is the for n input. This is my that for n addresses that many places as their, where either 0 or 1 is kept. So, this n variable or we can tell that address lines, so for a n address lines there are 2 to the power n such places.

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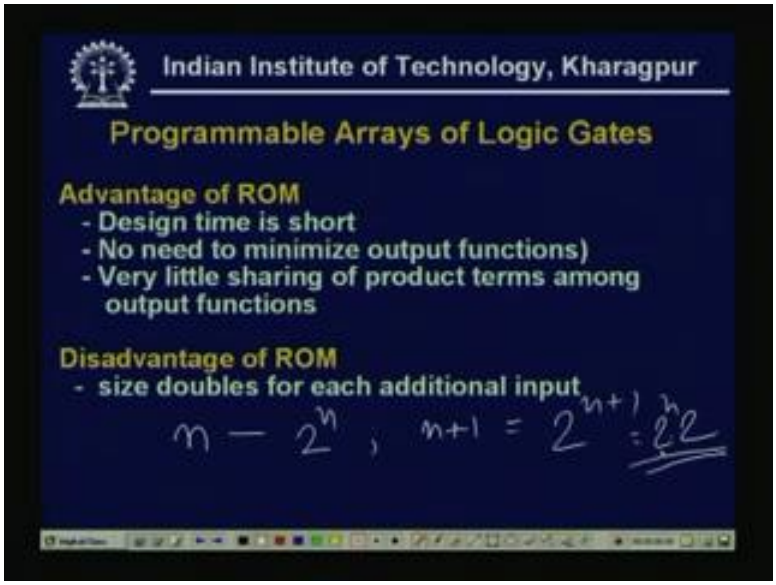

Now, size doubles for each additional input, why, because each additional input… That means, it will be it as it is for n. It is 2 to the power n for n variable or n input line it is 2 to the power n for n plus 1 it will be 2 to the power n plus 1 means 2 to the power n into 2. So, that for n variable, what will be the a, for a n input lines what will be the, size of the ROM and then for n plus 1. That means, if we increase only one additional input, then the size will be double. So, this is the one of the disadvantage of the ROM that means, size is too large.

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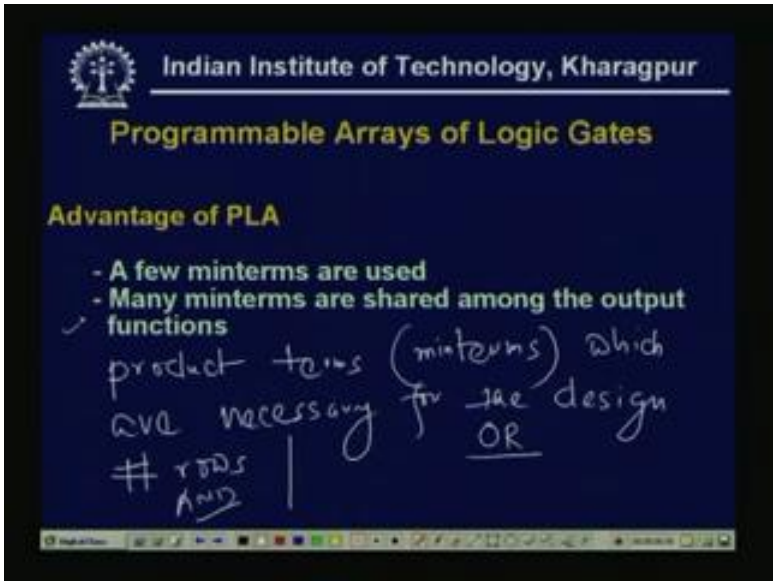

Now the advantage of PLA, say already we have that both the AND plane and the OR plane that can be programmed and a few min terms are used and many min terms are shared among the output functions. Already, we have seen that only that product terms which are available or the min terms of the function, product terms which are distinct and necessary, which are necessary for the design only. We will select that many number of rows that money number of rows in the AND plane.

And, in the OR plane this is in the AND plane and in the OR plane, what we have seen, that in the OR plane also from this number of rows or this many number of product terms that output lines can share this min terms. Already we have seen that many min terms are shared among the output functions. So, this is the advantage of PLA. So, the PLA size can be minimized,, but the ROM size that memory that is always fixed.

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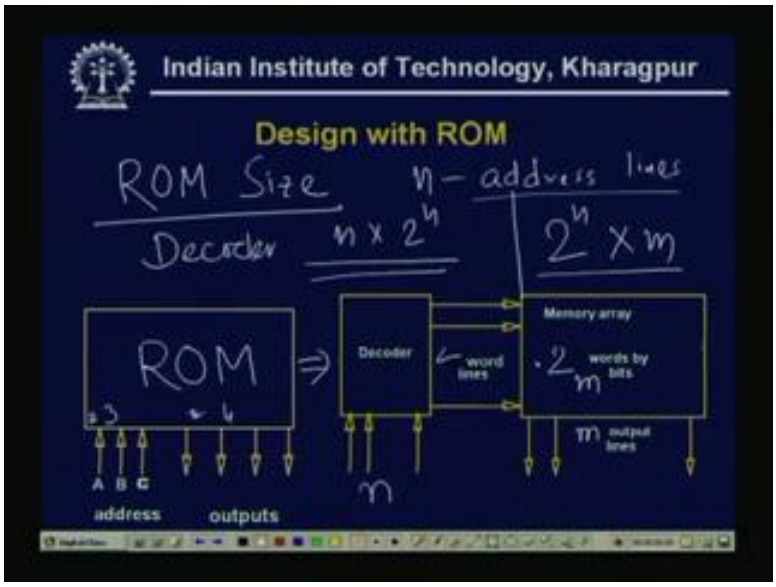

So, that ROM size that what we have seen, see that if it is a ROM, then for that n address lines that this will be the decoder will be a n 2 to the power n decoder. So, if we write for ROM that or what will be ROM size, say this is a n address lines or sometimes we call this is a bits address bits. So, this will be that decoder is that n by 2 to the power n and this memory array that will be 2 to the power n by m, where that m is the output? This is fixed, so this is the maximum that for n input lines, that number of this is a n column 2 to the power n rows and this is m columns.

So, the if we see the total design structure then this will be the this is the this is my size we cannot because all the this is read only memory. That means, as if all the contents for

all the places that is kept and mainly we are selecting the addresses depending on my output.

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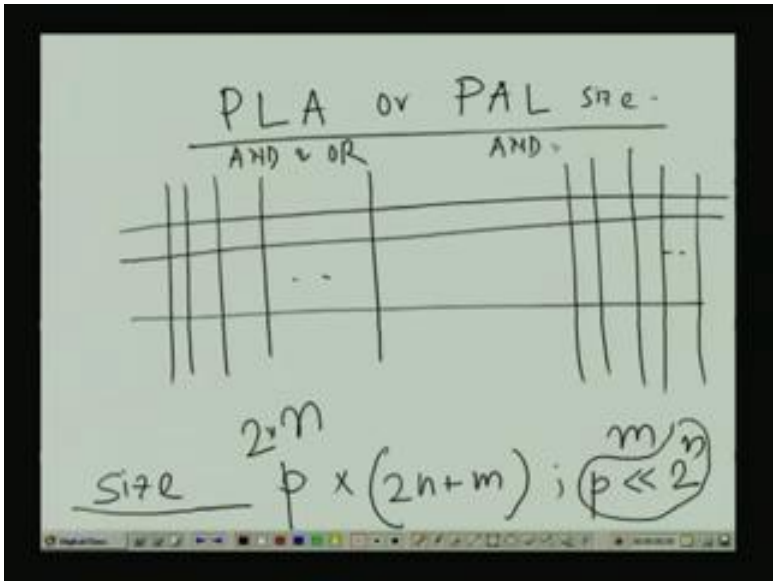

Whereas that for PLA or PAL, that is for PLA or PAL size that this size that input lines are these are 2 n, where for any n variables this is m outputs. So, this is 2 n plus m 2 n plus m columns and rows will be the only the P number of terms, where this P is very very less than the 2 to the power n.

Because in real life, from these all possible product terms 2 to the power n these are all possible product terms from 2 to the power n only a few P product terms are used, so this is my size. So, in real life always the PAL or PLA are advantageous than ROM design.

Another, this is that PLA is more programmable, because here the OR AND the AND plane and the OR plane both are programmed AND and OR plane. Here, the AND plane the only AND plane is programmed, but the not the OR plane, so here this PAL and ROM can also be used for design.

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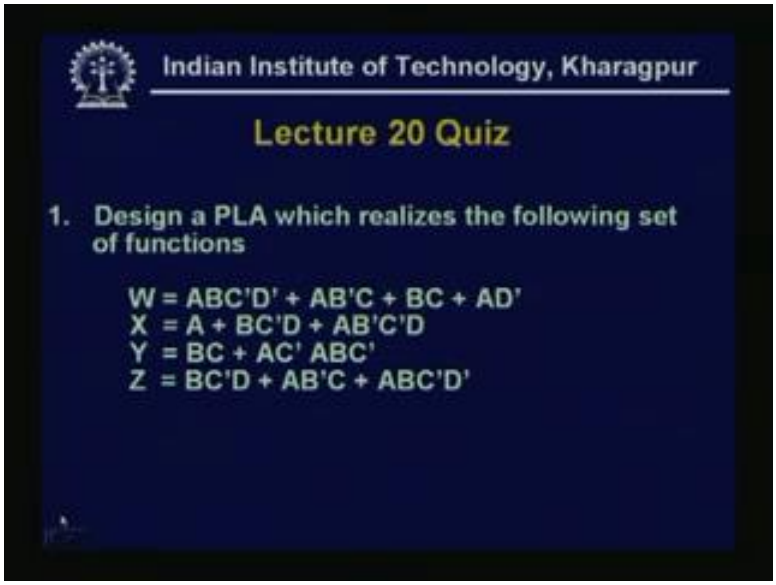

Now, we see that the 1 quiz question for this lecture 20, this is design a PLA which realizes the following set of functions and this is the four output functions that W is ABC bar D bar plus AB bar C plus BC plus AD bar, X is A plus BC bar D ABC AB bar C bar D. Y is BC plus AC bar plus ABC bar, Z is BC bar D plus AB bar C plus ABC bar D bar. This is a four input variables their and four output variables, so this is 1, we have to design the PLA which realizes this four output functions is a quiz for this class

Thank you.