Digital Systems Design.
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Lecture - 19
Combinational Logic Design using
Programmable Arrays of Logic Gates

In the last few lectures, we have learnt how the combinational circuits can be designed using functional blocks or the fundamental circuits like decoder, multiplexer, adders etcetera. Last day, we have seen the some generalized structure of realizing combination circuits using multiplexer. Now today, we will read another type of combinational logic design using programmable arrays of logic gates.

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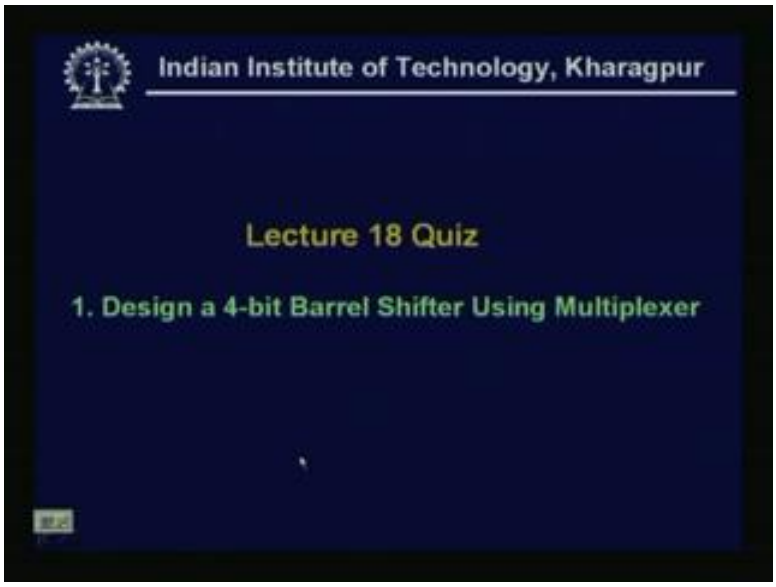

But before that, we start that programmable arrays quickly we solve the last days quiz question. The question was that a design it is a 4 bit Barrel shifter using multiplexer.

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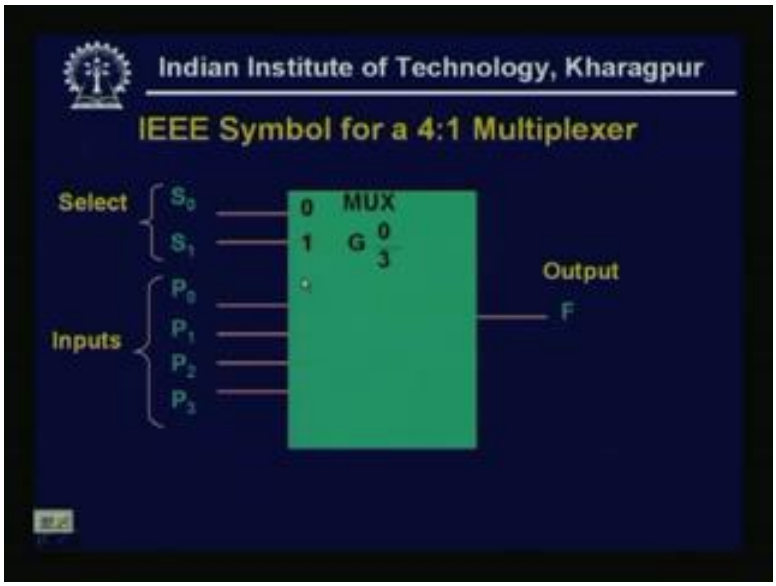

So answer, we see that all ready we have discussed the 4 2 1 multiplexer design. It has two select lines and four input lines one output lies and this is the IEEE symbol for 4 to 1 multiplexer. We will use this multiplexer to design a shifter 4 bit shifter.

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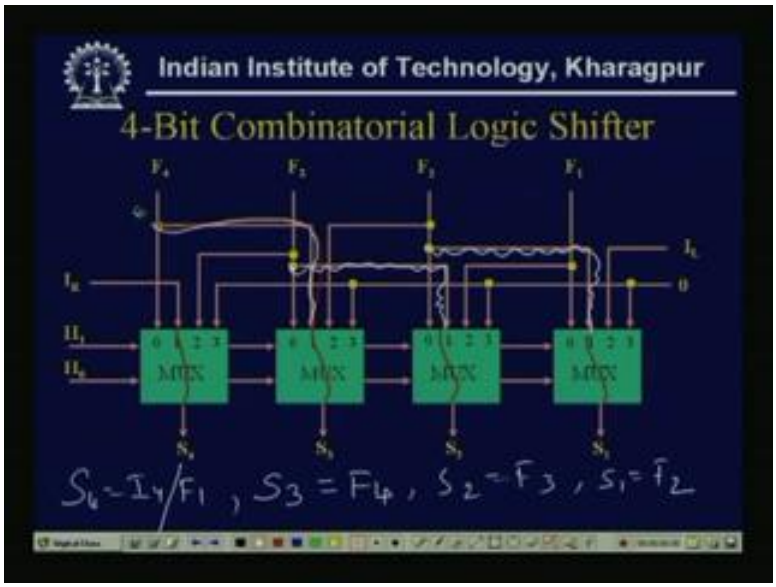

Now, first we see the normal combinational logic shifter, see this is 4 4 to 1 multiplexer we have used. This is my MUX 1 MUX 2 MUX 3 MUX 4 or reversely we can take that output S 1 S 2 S 3 S 4. And, the functions that F 1 F 2 F 3 F 4 that we want to implement or we want pass that thing as the output.

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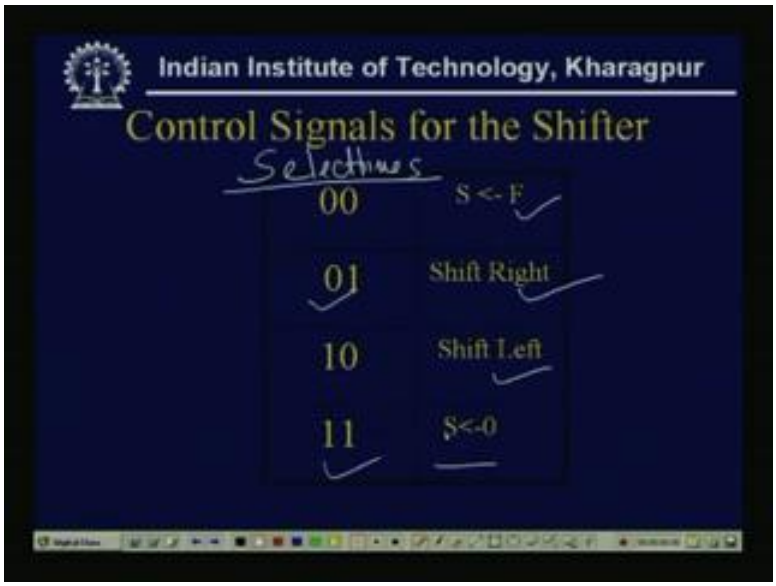

Now, there are the shifter has four different combinations it has mainly these are my select lines, so this is my S 1 S 0 select lines and this is my node of operations. So, if the select lines are 0 0, whatever we have applying in the F input, that is as it is passed to output; that means, F is passed to S. When it is 0 1, it is shift right 1 0 it is shift left and 1 1, then it is reset type of operation; that means, all zeros are passed to S.

Now we see, how the circuit behaves like that, see that H 1 is 0 is 0 0, if it is 0 0, then these select line should be or the first input line 0 should be passed as the output. Now, similarly for S j this 0 should be passed, here this should be passed, here this should be passed. So whatever, we are applying that actually the first 0 th is input and the F 1 to F 4 attached with that, so it will be S is F.

Now, when H 1 is 0 is 0 1, then the if H 1 H 0 is 0 1, then the first input that should be that one input should be passed to output this should be the situation. Now see here a input I r is fed to the first input, first input of S 3 is see this is the F 4, this is my F 4, this is the F 4 line.

Similarly, the F 3 line, see this F 3 that is fed to the first input of S 2 and for 0 1 combination of H 1 H 0 or S 1 S 0 it is passed to S 2 and the F 2 is passed to as the S 1. So, what is actually doing, it is F 4 is S 3 is F 4 S 3 becomes F 4 S 2 becomes F 3 and S 1 becomes F 2 and 1, it S 4 can be I 4 of if it is periodically connected then it can be F 1.So, it is actually 1 right shift, if it is the select lines are 0 1, it is a right shift.

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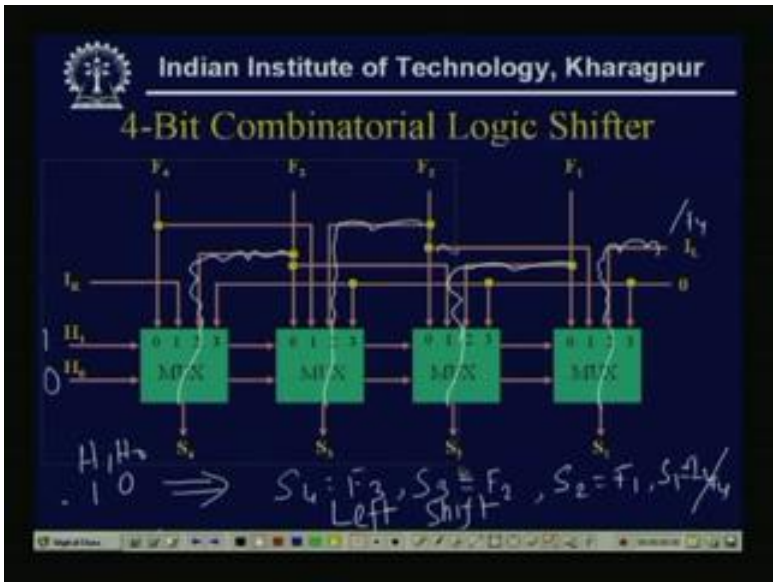

Similarly that now, if it is 1 0, we see that actually for 1 0, the second input will be fed to it is passed as output, second input. Now, what is second input, if it is select line is 1 0, then second input is see it is F 3 is passed to S 4, similarly F 2 is passed as S 3, F 1 or F 1 is passed as S 2 and a input IL or that just like the right shift it can be a four also that can be fed to S 1. So, what we achieve that for H 1 H 0 values as 1 0, we get that S 4 equal to F 3, S 3 equal to F 2, S 2 equal to F 1 and S 1 is some IL or if it is periodically connected then it can be F 4. So, it is nothing but a left shift everything is shifted left.

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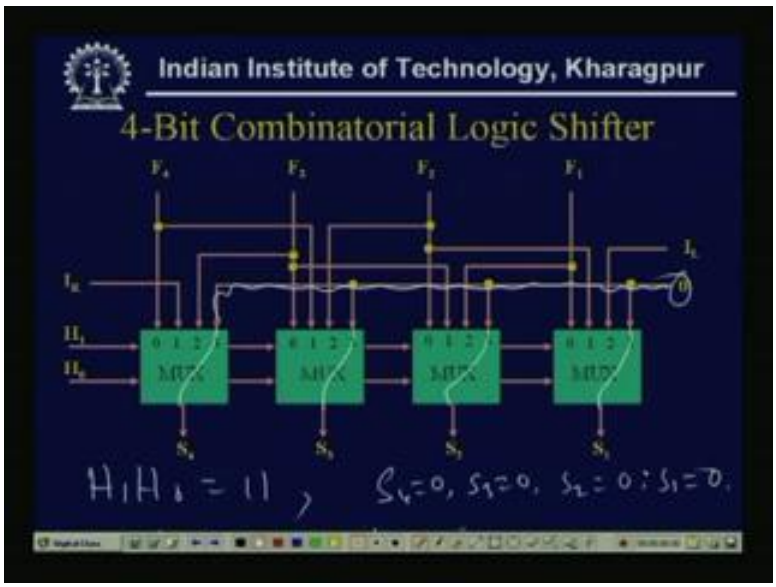

Now, we see that for select line 1 1 combination, what will happen, for select line 1 1 combination, see that this fourth input, that will be passed as output this is the situation. Now in this particular design, the fourth input is stacked with 0 some 0 input. So, this is some 0 input. So, when it will be H 1 is H 1 H 0 is 1 1, then all S 4 equal to 0 S 3 is 0 S 2 is 0 S 1 is 0, so this is some reset type of design.

So, what we see that, (Refer Slide Time: 03:08) that there are four combinations and if the select lines, if my select lines are 0 0 as it is, the inputs are passed to output 0 1. It will be shift right the 4 bit 1 0, then the 4 bits are shifted left and then if it is 1 1, then it is a reset type of thing that all outputs becomes 0. So, this is one design of the shift. Now, there are in real life practice, there are many other different type of shifter are possible. Actually barrel shifter we can design like that.

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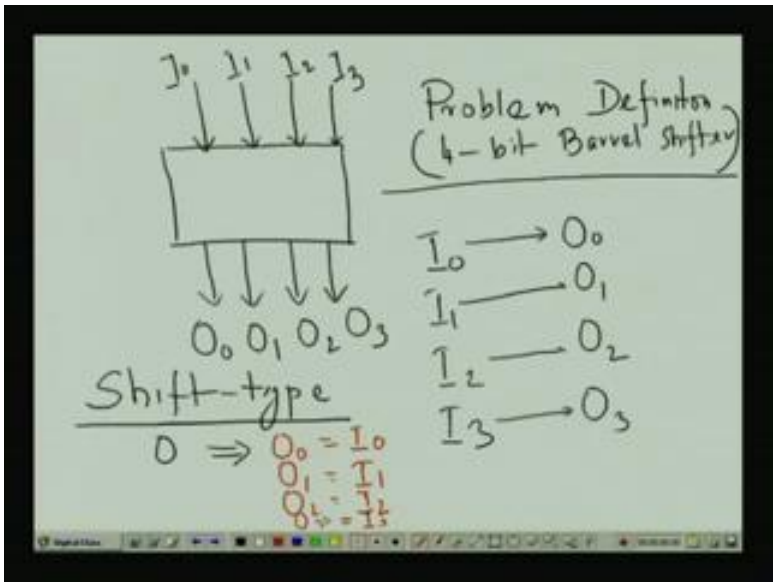

Or we can define that see if there are four inputs and there are four output, see this four inputs are I 0 I 1 I 2 I 3 and outputs are O 0 O 1 O 2 O 3. Then, the problem can be stated like that or this is my problem definition that 4 bit barrel shifter that see I 0 I 1 I 2 I 3 and see O O O 1 O 2 O 3.

Now say, for one situation that they can be different type of shifts, say I am defining shift type. If shift type is say 0 type of shift, means as it is the inputs will be passed to output. That means if it is shift at 0 it defines that I 0 or O 0 is O 0 equal to I 0 O 1 is I 1 O 2 is I 2 and O 3 is I 3. So, this is one type of shift.

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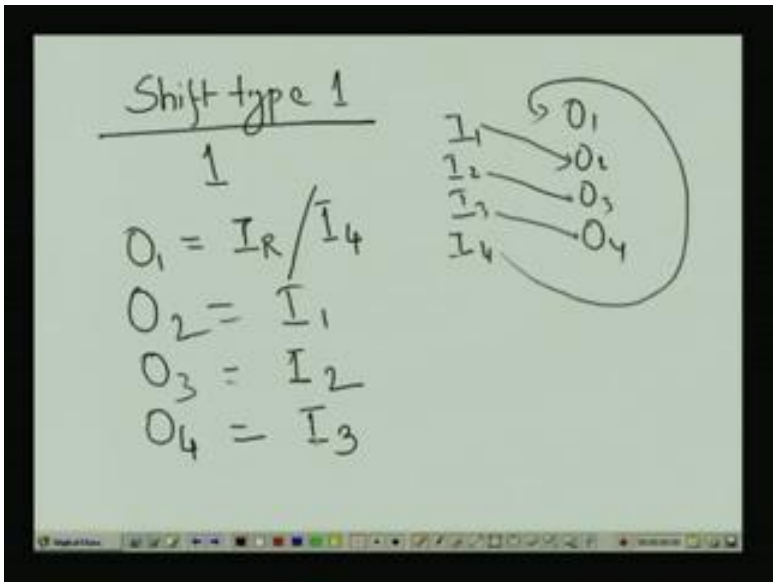

Now, if it is say I am taking shift type one shift type 1. That means it will be problem is like that say if it is I 1 I 2 I 3 I 4 O 1 O 2 O 3. Then all the bits input bits will be shifted by 1 bit. That means, this type of shifting is there that either I 4 can go here or that can be fed as 0.

So, it will be O 1 is either some it is shifted by 1, so we can tell that it can be I R or I 4. If it is periodically shifted O 2 is I 2 O 3 is or O 2 is I 1 O 2 is I 1 O 3 is I 2 O 4 is I 3. So, this is one type of that is, if it is shift type 1.

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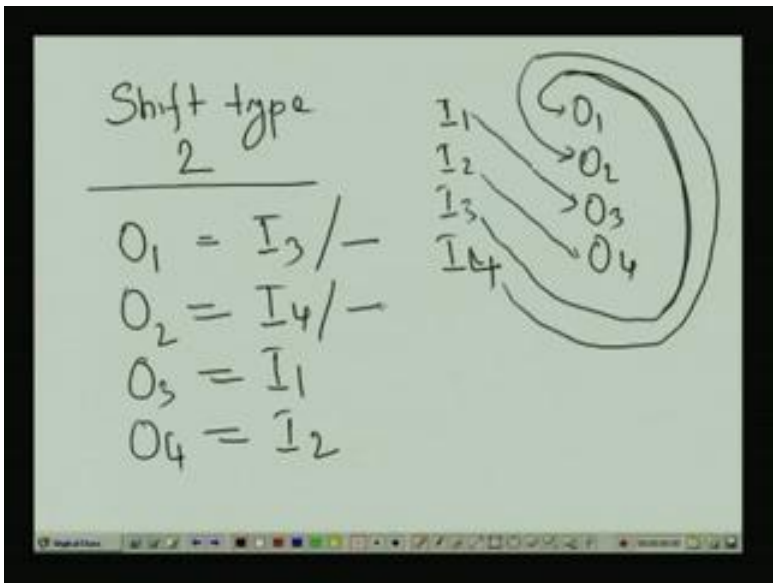

Then, it will be the, if it is shift type 2, then this type of shifting is rare O 1 O 2 O 3 O 4 and there will be two shift. That means I 1 will be shifted to O 3, I 2 will be shifted to O 4 and I 3 can be shifted to O 2 and I 4 can be shifted to O 1. There will be two shift or I 3 will be I 1 is O 3, I 2 is O 4. Actually I 3 should go to, there will be two shift, I 1 should be see that it will 2 bit shifted.

So, I 1 comes to O 3, I 2 comes to O 4, I 2 should goes to O 2 and I 3 should goes to I 3 goes to O 1 and I 4 should goes to O 2. So, this type of combination I will get, that I 1 I 2 or if I write that O 1 O 2 O 3 O 4, then O 3 will be I 1 O 4 or O 3 is I 1 O 4 is I 2. Then, O 1 should be I 3 and O 2 should be I 4 this can be different input also.

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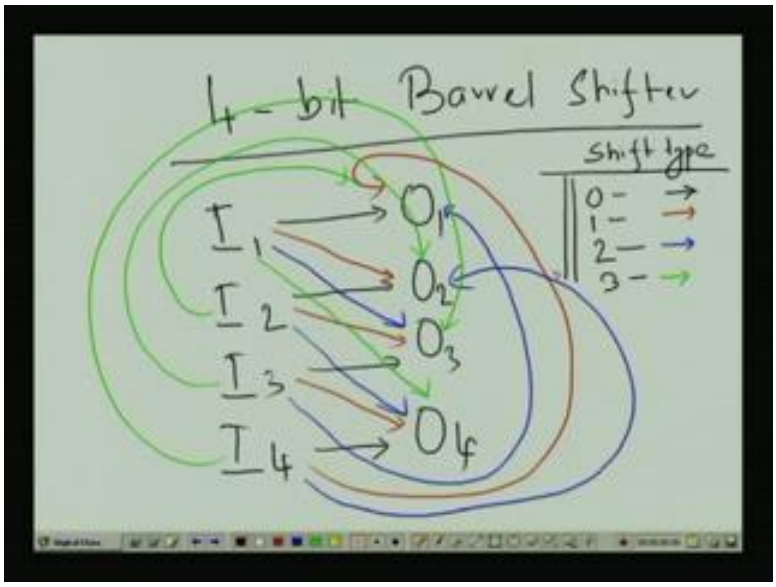

But, if it is periodically shifted then this type of shifting we want. That means now if we summarize we want a 4 bit barrel shifter like that that if it is I 1 I 2 I 3 I 4 O 1 O 2 O 3 O 4. Then, first type of shift will be that as it is I 1 will go to O 1 I 2 O 2 I 3 O 3 I 4 O 4.

Second type of shift will be I 1 will go to O 2, this is the one shift and it will go to O 1. Now, third type of shift will be I 1 will go to O 3, I 2 will go O 4 I 3 will go to O 1, I 4 will go O 2. And in that same way we can still do some more, say if it is I 1 can go to O 4 I 2 can go to O 1, I 3 can go to O 2, I 4 can go to O 4 O 3. So, this type of shifting we want.

Or if we just in color if we write that actually this shift type we can tell that shift type 0 means it is represented as a black. Then shift 1 means it is represented as a red, shift 2 means it is represented as a blue, and shift 3 is green. So, this is one type of shifter we want to decide.

So, these will be the quiz of our the current lecture that lecture 19, that again we have to design. This type of barrel shifter a 4 bit barrel shifter, where we will if we select or if we want that shift 0 1 2 3, again we call this is our this is one type of barrel shifter.

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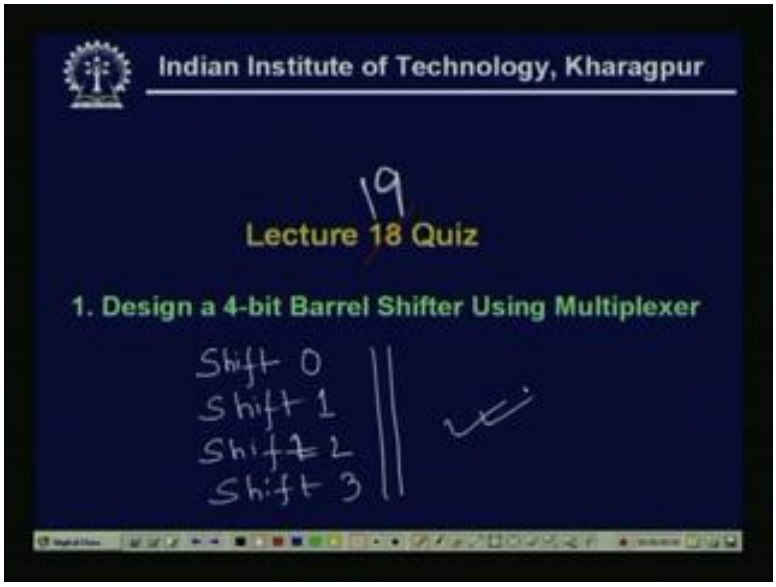

So, our lecture 19 quiz is again this is our lecture 19 quiz, that we want a design a 4 bit barrel shifter. Where the shifts, just now we defined that shift 0, shift 1, shift 2 and shift 3 and shift 3. So, this is our next quiz.

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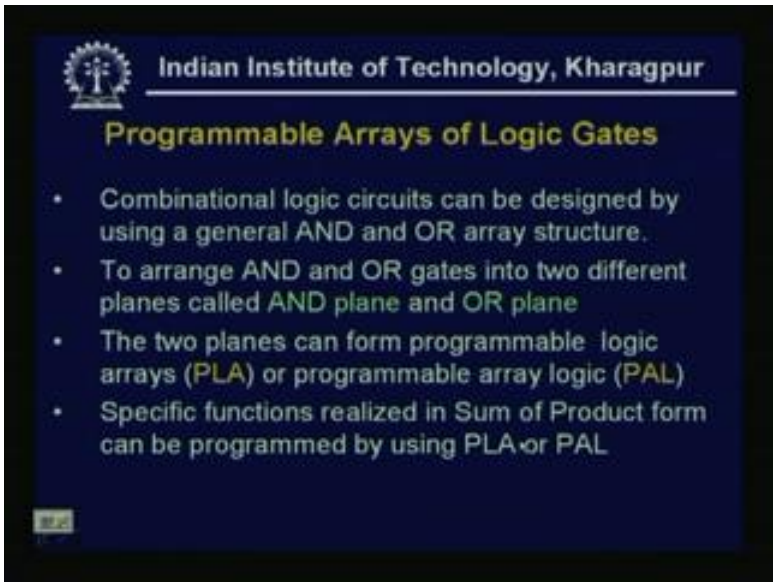

Now again, we start our new lecture; that means, that programmable logic arrays, first we define, what do you mean by programmable arrays of logic gates? See that combinational logic circuits can be designed by using general AND and OR array structures.

See what we have read that, all combinational logic can be realized by a set of functions, where the functions are represented as the sum of product form. Now, the sum of product form means what sum means our OR gate and product means, the AND gate, so mainly it is AND OR realization. Now, these AND OR realization these AND for from logic to logic or from one circuit to another these AND OR combination will differ.

Now, the concept is that if we all ready if we predefined some AND arrays and OR arrays and depending on the circuit given circuit or the circuit to be realized. If I select the AND means the product term will vary or means the min term will be varying. And now if I select a particular OR then my combination will also vary. That means, my some function will also vary.

So, I am getting a variable, sum and product terms. So, obviously, one particular design will realize a number of circuits combinational circuits only one restriction, is the total number of variables must be equal. So, to arrange AND and OR gates into two different planes called AND plane and OR plane. And, the whole structure is called the

programmable, because we can program we can change the product terms as well as the sum terms.

Now, the two planes can form programmable logic arrays or programmable array logic. We will see later what is PLA and what is PAL, but all are programmable arrays using AND planes and OR plane. Now, specific functions can be realized in sum of product form and they can be programmed by using PLA or PAL.

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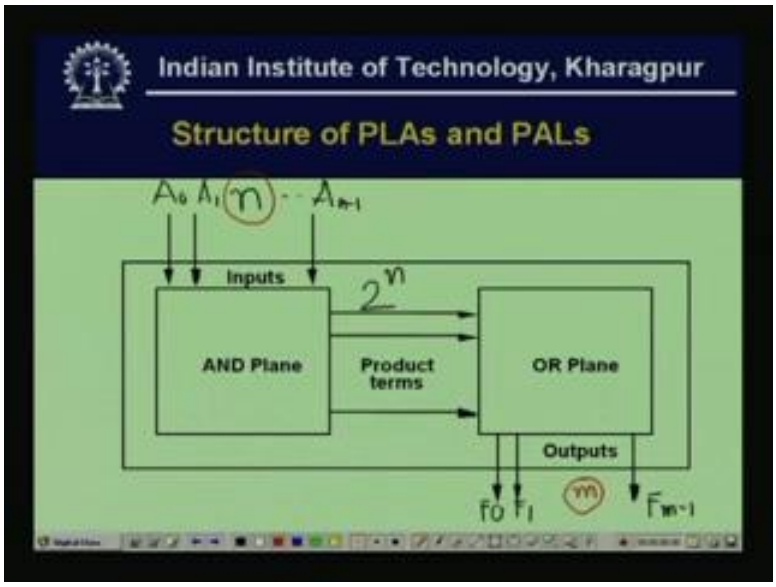

So, if we see the structure, see these are my AND planes, so if there are say there are n number of inputs. So, we know that if it is a n inputs, then there are min terms possible or the product terms can be 2 to the power n such product terms.

Now, as if these are all min terms and they are fed to the OR plane. So, among this, what is the function of this OR plane, the OR plane will select sum of the min terms from this 2 to the power n min terms. And it will or that thing or it will be taking the sum to give a output. That means if my this is A 0 A 1 to A n minus 1 up to this inputs and outputs will be say F 0 F 1 up to say some F m minus 1. That means, m number of outputs will be there n number of the inputs and m number of outputs. Now we see, how this is the programmable arrays mainly the AND arrays and OR arrays are there over a structure and now, how this programmable design now, programmable arrays can be used to realize the combinational circuits.

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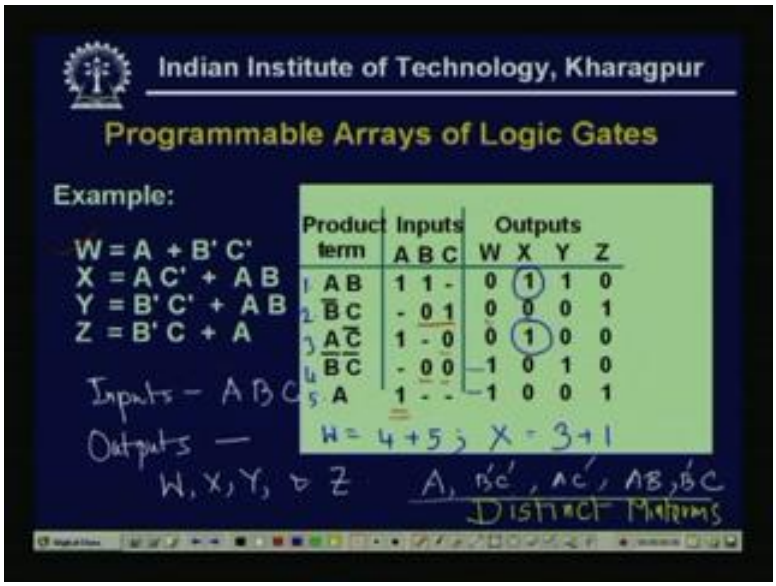

Now, we take one example, say I have three inputs and four output functions. So, this is a combinational logic, where the set of outputs are four outputs means that inputs are only A B C, outputs are W X Y and Z.

Now, say it is all ready by using Karnaugh map given the problem that it is minimized. Now, the outputs or the or output expressions are W equal to A plus B dash C dash X is A C dash plus AB Y is B dash C dash plus AB Z is B dash C plus A. Now, how first we see or we find out that, how many distinct min terms are there in this particular output. So the distinct min terms see A B dash C dash AC dash AB see again B dash C dash is there. So, it is not distinct AB is also there B dash C.

So, there are only five distinct output or distinct not output this is distinct min terms. So, if I can realize this five distinct min term then I should get the output W X Y Z. Now, see that product terms this is the product terms. So, product terms that five product terms AB B dash C AC dash B dash C dash and A.

Now, we see that how they can be or this nothing but that AND. So, AB means A AND B B dash C means that B complement this is B complement and C 2 input AND gate, AC complement AC dash means A AND C complement B dash C dash means B complement C complement and A means only one literal A. So, if these are the min terms available, then the first output W is A plus B dash C dash.

So, I have to take that if I mark this product terms as 1 2 3 4 and 5. Then the first output is actually first output is A plus B dash C dash means from here this will be W is 4 plus 5 this is 4 and 5 OR, see the output W this is the OR plane this my OR plane. So, output W is OR and the two inputs are 4 and 5 means that B dash C dash this is my B dash C dash and this is my A.

Now, similarly what will be my X, see the second column is my X and X is AC dash plus AB, so I will take that X is my 3 and AB is my 1. So, in the second column or in the column of X that where the AB term is there. That means, the first product term AB there will be 1 1 and AC dash means 3 that means 1. If 1 1 exist in the AND plane; that means, I am taking that that as the input of my AND gate. And, if in a column in the OR plane, a column consists of 1 then, that particular product term will be the input of the OR gate.

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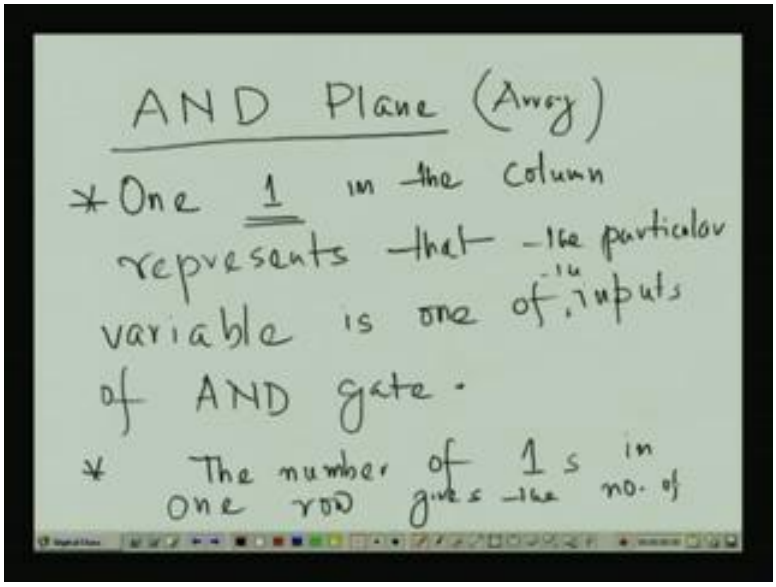

So, if we summarize, then what we can write, that and for the AND plane or we can tell AND array this is 2 D array that see that A B C. These are one row that one 1 in the column represents that the particular literal or variable is one of the input of AND gate.

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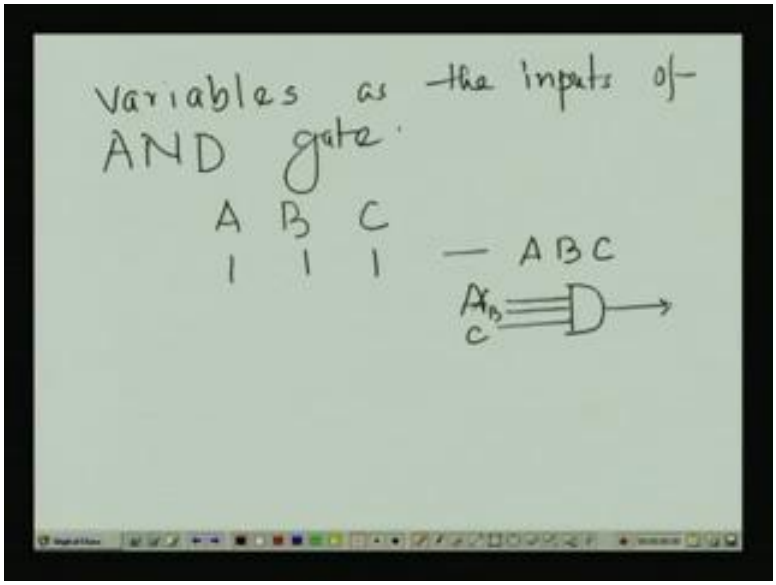

And, the number of ones in 1 row gives the number of variables as the inputs of AND gate or actually determines that the how many inputs of the AND gate is needed. That means if say ABC in 1 row all are 1. That means, it gives the term product term ABC which is actually a three input AND gate is a three input AB and C three input AND gate.

So mainly, the AND arrays the left hand side the AND arrays they are they represents that, how we can take, in a different AND combinations. Now, similarly this is my OR plane, so these are mainly the AND gates these are my AND gates this is the AND and these are my OR this sum of product forms. So, this product that will be taken from these variables complemented as well as uncomplemented and the outputs will be represented by this or of this ended output. So, if 1 1 exist similarly if 1 exist then that particular, now, it is only in the column. So, for AND it is in the OR plane.

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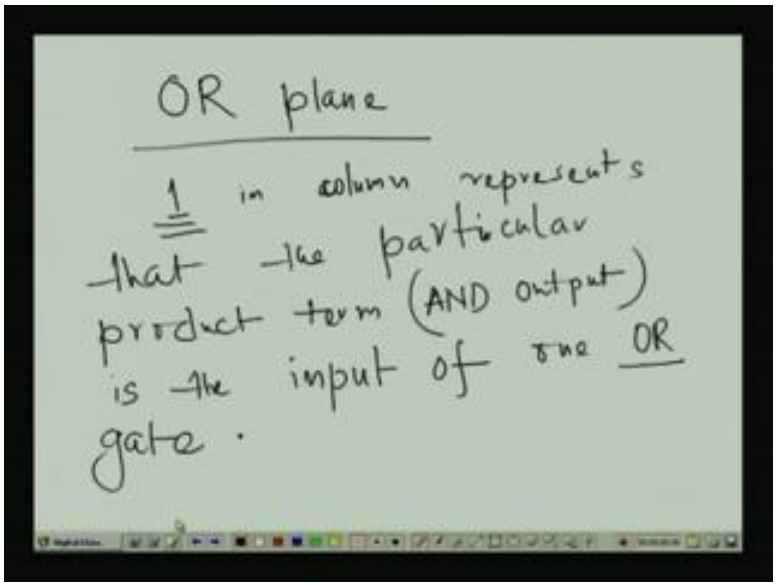

For OR plane, that 1 in a column represents that the particular product term or we can tell min term or we can tell them AND output is the input of one OR gate.

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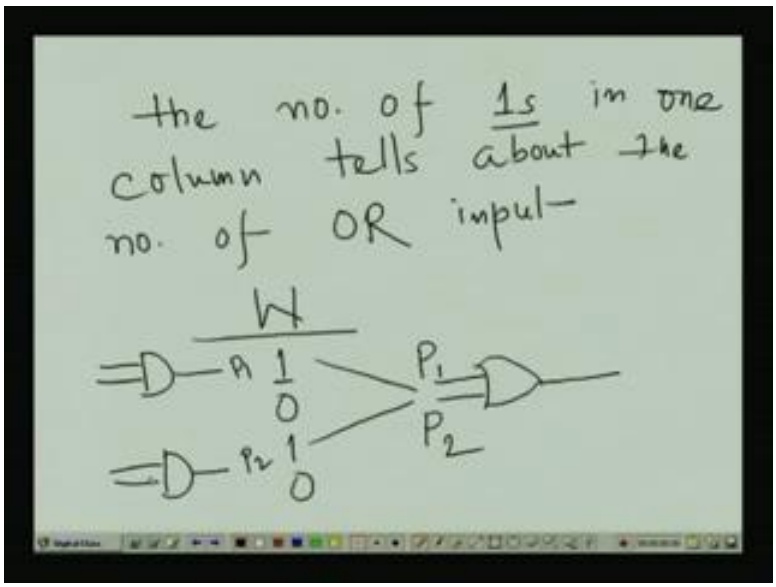

And here, the number of ones in 1s column tells about the number of OR input. That means say if I have 1 output line W and in this column there are say there are 2 ones that means I meet a two input OR gate. Say this product term say is P 1 and this product terms say is say P 2, so this is my P 1, this is my P 2. And, P 1 P 2 is actually some AND output, because these are the say some AND gate output, so this is the realization.

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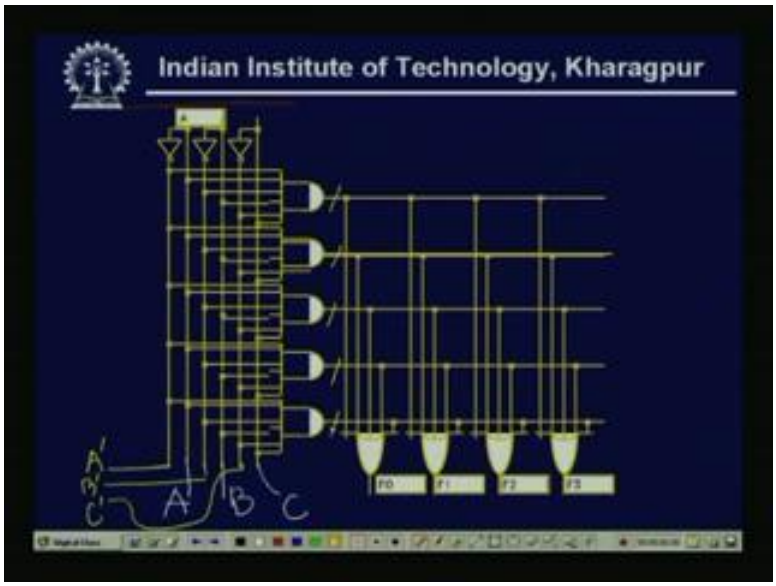

Now, we see the structure how this array structure has been done in real life. See this is these particular example say ABC are the three inputs say this is A say this B and this is my C inputs.

Now, as in the functions or the output expressions, the complement variable is also exist. So, first I realize that A bar B bar C bar by given three inverter, so these we can write as A bar this is my B bar and this is my C bar line. So, this is A bar B bar and C bar, so these are my inputs. So, if it is a three variable or three inputs, but actually when it is implemented in real life as if we are assuming that six inputs are available three complemented variables or and the three are uncomplemented 1.

Now, these ABC and A dash B dash C dash are fed accordingly as all ready we have seen in the example, this is my AND gate. So, there are five distinct product terms, we have seen that there are five distinct min terms A B dash C dash AC dash AB B dash C. So, these min terms are actually generated by this, see here this is a AND gate this is one AND gate. So, these five distinct min terms they we will be available here. Now, and there are four outputs, where the four outputs are W X Y Z first 1 is A plus B dash C dash.

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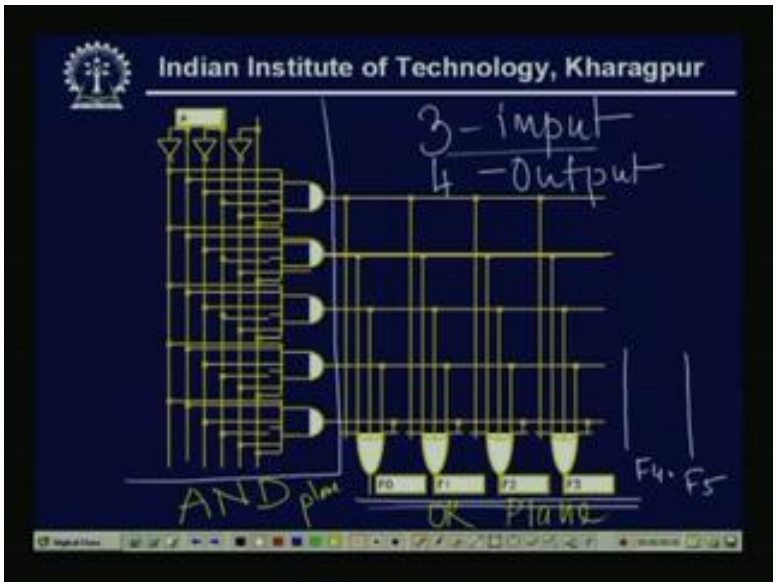

So, W is first we that generalized thing that this is my AND plane and then we will discuss that part, this is my AND plane and this is my OR plane. So, why it is programmable, because this is for 3 input this is a structure for three input and 4 output programmable design.

So, any 3 input variable product term or min terms I can get by using this 5 AND. And then as all any min terms or any product terms are available, then any combination of OR combination I can get from this all possible product terms. And I can realize the any 4 output from this all possible 3 input product terms. So, this is a totally variable structure that variable means that I can get any product terms from this 3 input variable I can get any 4 output from here. But, what we can do, that if it is 5 output or 6 outputs then I can add in the OR plane I can add some more I can add say F 4, I can add F 5 like that.

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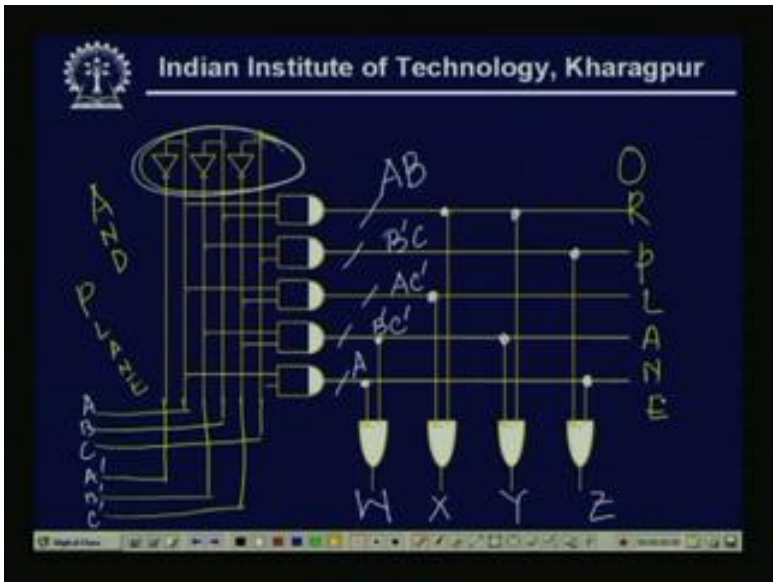

Now, we see that what example, we have discussed it is more concrete, say again if we draw that the A B C lines say this is my A this is my B and this is my C line . So, this is A B C. Now, first what is done, that A complement B complement and C complement that also has been realized by using this inverters. These are the inverters, so this is my A complement B complement C complement.

Now for this particular example say, what these AND gate output of this AND gate, the first AND gate. See it is taking B as one of the input and A bar or A, A and B. That means, this is my AB. Similarly, what is this output, see this is C and this is B bar. So, this is B bar C these output is this is C bar and this is A. So, this is my AC bar.

This is that, these 1 is B bar and this is C bar, so this output is B bar C bar, this output is simple only one actually input gate, this is A. So, this is my AND plane and this AND plane they are generating this five distinct product terms that we actually need for to evaluate my output expression W X Y Z.

Now, what was W, we remember that W was W was A plus B dash C dash similarly X is AC dash plus AB. We see W is my A plus B dash C dash, if this is my W it should be 1 input should be A and B dash C dash. Similarly, the X is AB plus AC dash, this is my X Y is AB plus B dash C dash and Z is the B dash C plus A A plus B dash C dash. So, this is my OR plane.

So here, this if I want to represent this as the matrix, then what I can do, that actually if one particular variable is the input of 1 AND gate, then I will put a 1 or say cross in that position otherwise I will give a 0. So now, how many rows and columns it has, see then in the AND plane the number of columns will be the twice that of input variable and the number of rows will be the number of distinct min terms exist in that particular function that I want to realize.

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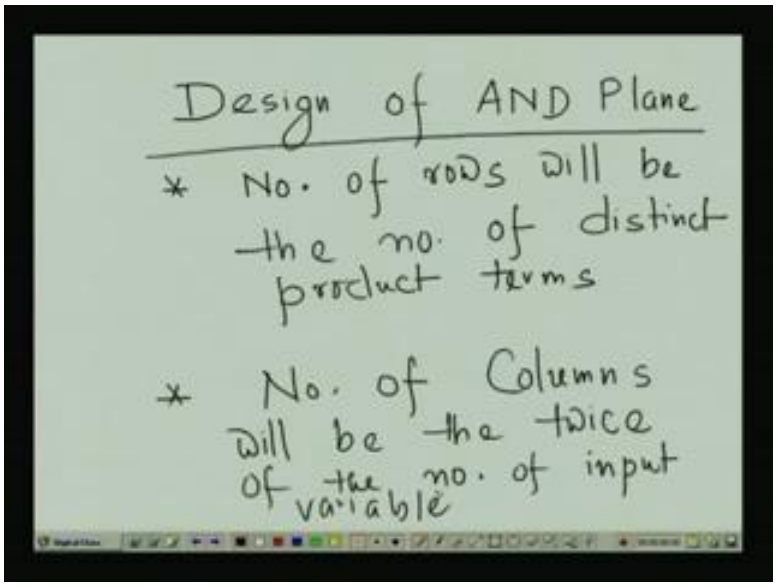

So, if now I can that design the AND plane, 1 is the number of rows will be the number of distinct min terms all product. And, number of columns will be the twice as that of twice of the number of input variable, why it is twice, because I need complemented as well as uncomplemented variables input variables.

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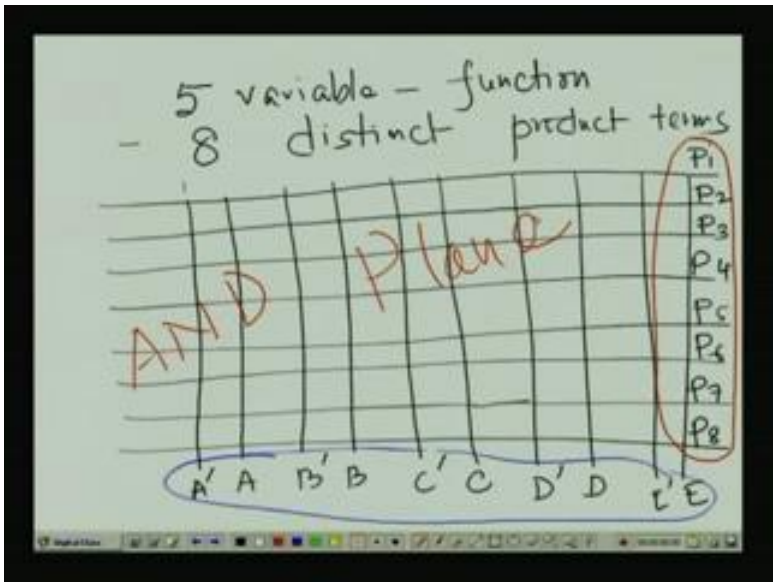

So, for 5 variables inputs, say if 5 variable function which has say 8 distinct product terms, then the AND plane should be that number of columns are 10 that and there will be 8 rows. So now, if I give the name, then I am telling this is my A A bar B B bar C C bar D D bar E E bar, these are my 10 variables.

And, that 8 distinct product terms, it will generate say that P 1 P 2 P 3 P 4 P 5 P 6 P 7 and P 8, these are my 8 product terms and these are my 10 input variables. So, this is the structure of my AND plane.

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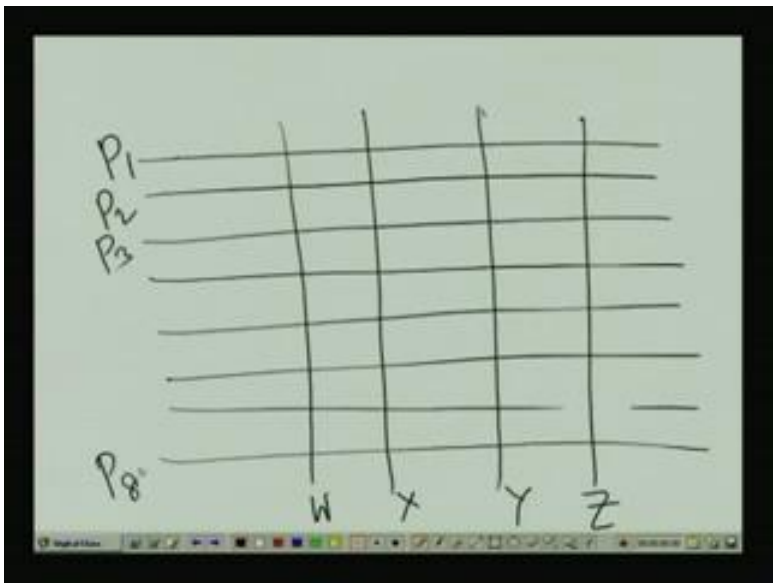

Now, what will be the structure of the OR plane, then OR plane that product terms will be same say that 8 product terms will be there. And, say I have 4 output, then this 4 output will be the this column say W X W X Y Z these are my outputs and this P 1 P 2 P 3 to P 8. We will finish this lecture here and we will continue in the next class.

Thank you.

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Lecture - 20
Logic Design with PLA

Today, we will continue the discussion that last day. We were doing mainly the logic design with programmable arrays.

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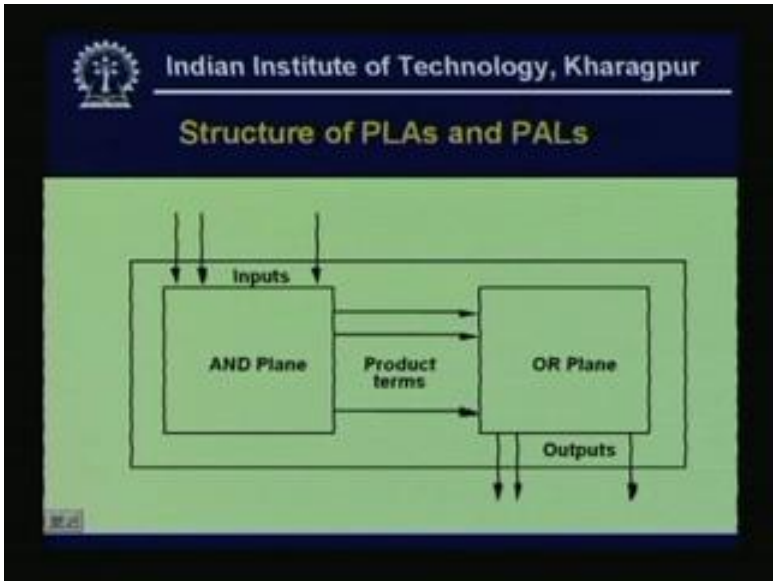

Now, today we will see that the logic design with PLA's.