Digital Systems Design
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Lecture - 15
Design of Common Digital Elements

In this class we will learn the Design of some of the Common Digital Elements. Mainly these elements are frequently used or very popularly used for all the other digital designs or the some bigger circuits.

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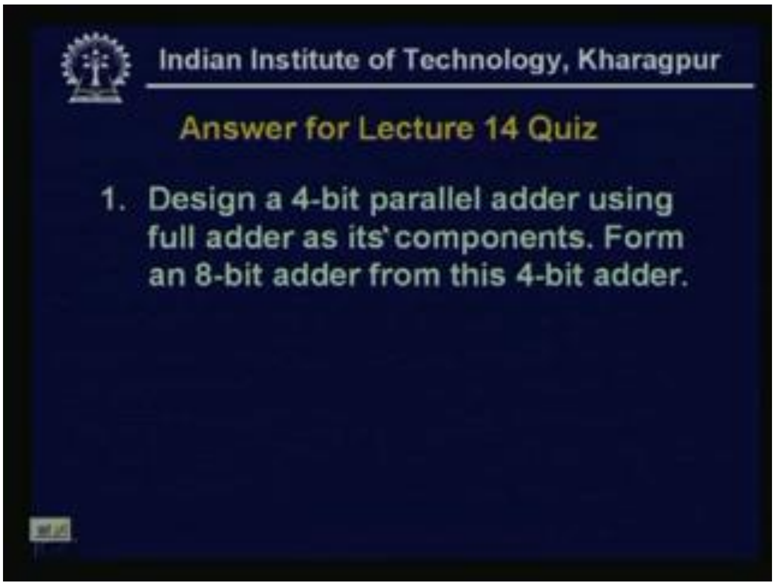

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Answer for Lecture 14 Quiz

1. Design a 4-bit parallel adder using full adder as its' components. Form an 8-bit adder from this 4-bit adder.

Now, before we start the design these elements, first we will see the last days quiz question. So, the question was the design a, it is a design of a 4 bit parallel adder using full adder as it is components and then from an 8 bit adder from this 4 bit adder.

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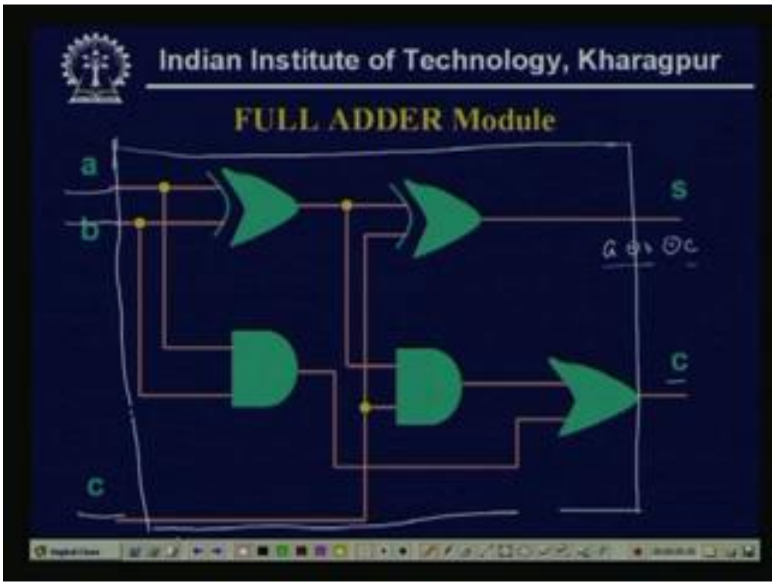

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FULL ADDER Module

Now, all ready we have read the full adder module, it is that sum form a XOR or b XOR c, sum was a XOR b XOR c the a b are operands and c is the carrying and this is the current carrying, which is a b plus b c plus c. Now, this is one module all ready we discussed what we can see, as if this is say one module, we are thinking as if this is one module whose. So, this is a black box there are 2 inputs a b another input c; that means, there are 3 inputs and 2 outputs s and c.

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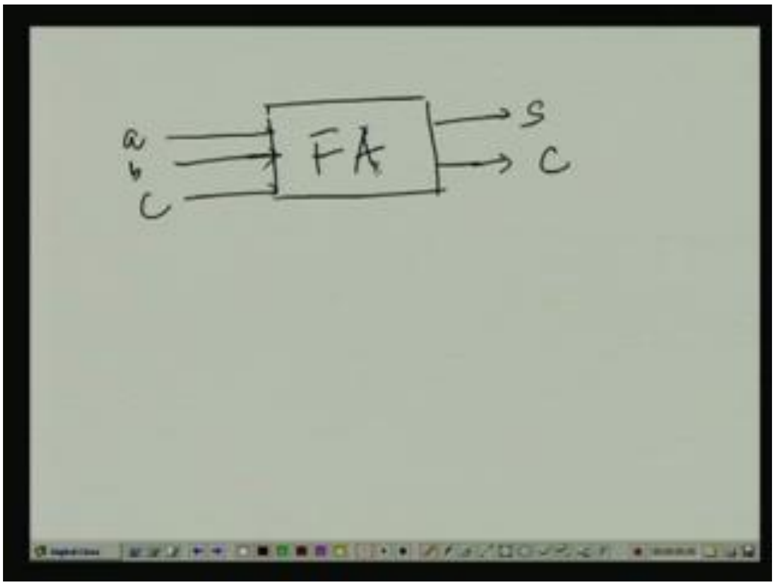

So, what we can see as if the whole circuitry is in between, this a, b, c, s and carry sum and carry and this we are calling a Full Adder FA, this is my full adder module.

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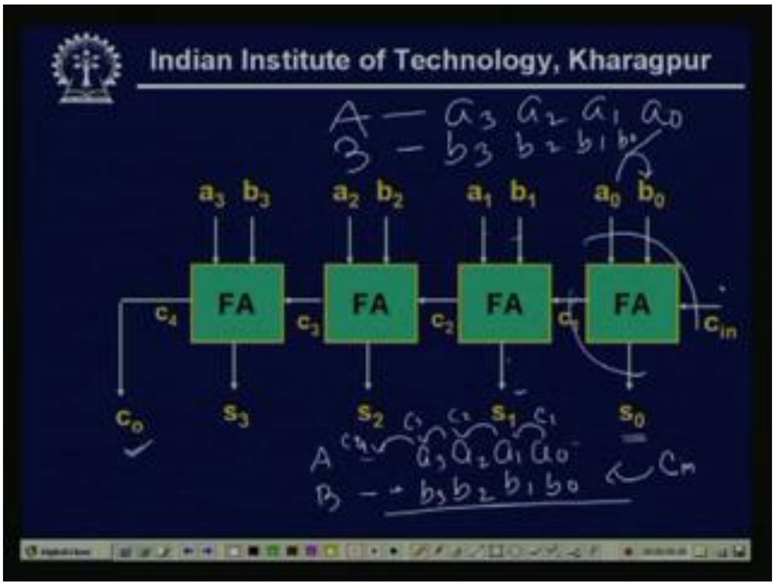

Now, this is a 4 bit full adder; that means, I have to add a 3 say A is 4 bit, a 3, a 2, a 1, a 0 and B as b 3, b 2, b 1, b 0 these we will add. So, the initial carrying we are considering as C in and for here the carries are c 1, here the carry is c 2, this is c 3 and c 4, this is the notations of the addition modular or this 4 bit add. Now, that just now we have drawn a full adder module, we have taken 4 such full adder module, what we have seen that one full adder module. There are 3 inputs and 2 outputs see these are the 3 inputs, two operands a 0, b 0.

That means, now these from a, so A that a 3, a 2, a 1, a 0 as if this a 0 is coming here and B b 3, b 2, b 1, b 0 this b is say a 0, b 0 this two are fed to the first full adder module. And this is the initial carry, so these are the 3 inputs, the 2 outputs are this is the first bit sum; that means, the sum of 0'th bit is 0 and the carry of the first bit; that means, carry of the sum of the first bits c 1. Now, it is fed to the second full adder module, where the operands are the a 1, b 1 means the second bit of the two operands.

Again see here for that second full adder module also there are 3 inputs a 1, b 1 and the c 1 means the previous carrying and it generates 2 output c 2 and s 1, so s 1 is the second sum or the second bit sum and c 2 is the second carry bit. Similarly, it is fed to the third full adder module and a 2, b 2 is the input s 2, c 3 are the outputs and the for the fourth the a 3, b 3 are the up to operands and s 3 and the final carry we are calling that this is c 0 or that this is my final carry 0.

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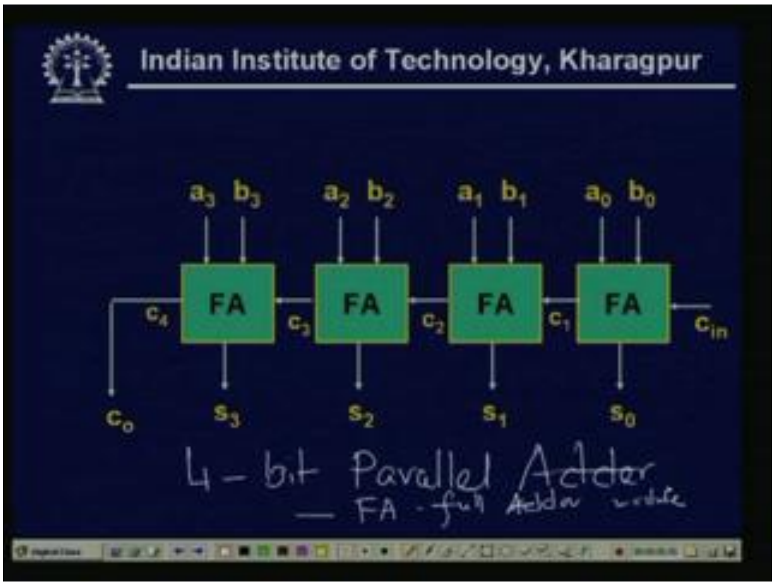

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So, now this is my 4 bit parallel adder we can tell that this is the 4 bit parallel adder, which was drawn from taking the full adder as the module and FA is the full adder module. Now, the second part was that taking now I will take these as a module, so this is a 4 bit adder and from there sum 8 bit adder we have to draw.

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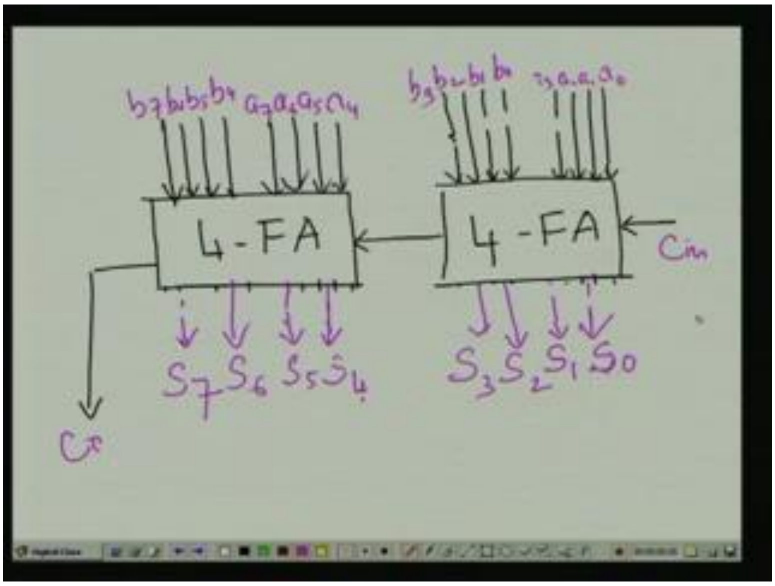

$b_7 b_6 b_5 b_4$ $a_7 a_6 a_5 a_4$
$b_3 b_2 b_1 b_0$ $a_3 a_2 a_1 a_0$
4-FA
4-FA
Cin
$S_7 S_6 S_5 S_4$
$S_3 S_2 S_1 S_0$
Co

Now, we see, so that means here now this 4 bit I am writing 4 FA means this is a 4 bit full adder, another 4 FA we have taken because, for 8 bit we need. Now, there are 4 inputs for the 4 bit actually there are 4 a’s and 4 b’s. Similarly, see for 8 bit adder that the inputs are see these are my a 0, a 1, a 2, a 3 then a 4, a 5, a 6 a 7. And these are the b inputs b 0, b 1, b 2, b 3 and these are b 4, b 5, b 6, b 7, so 0 to 7 these are the inputs.

Again this is my carry in and these are my sum bit s 0, s 1, to s 7 and similarly, here now these are here there will be 4 because, the we have taken the 4 bit adder. So, there will be for a 0, b 0 summing it will generate s 0 for a 1, b 1 it is s 1, a 2, b 2 it will be s 2, a 3, b 3 it will be s 3. Similarly, for a 4, b 4 it will be s 4, s 5, s 6 and s 7 and this is my carry out. So, in the previous case we have taken the full adder as the module and then we have designed or we framed a 4 bit adder and now taking 2 4 bit adder. We have done a 1 8 bit adder and now here that 4 bit full adder, as if these are the module or these are the elements.

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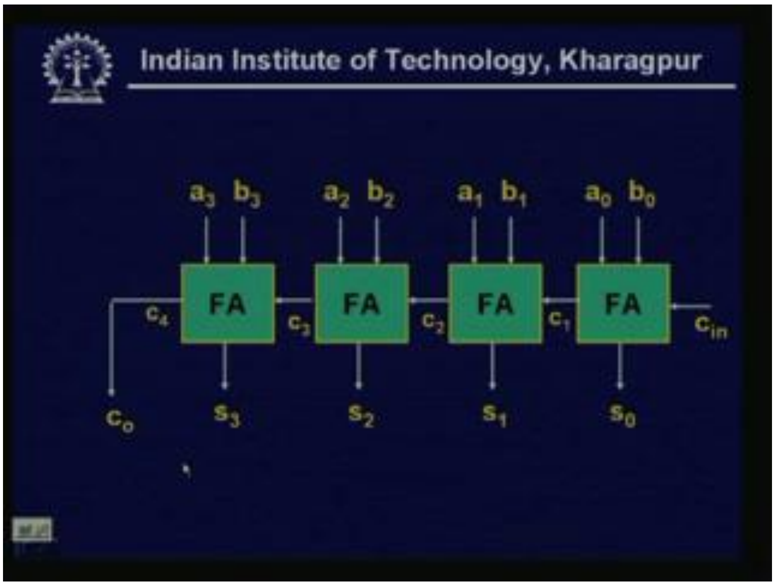
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Now, this just now what we discussed that as if full adder is the module taken for designing a bigger circuit or when we are designing a 8 bit adder, we are taking the 4 bit adder as the module for designing the circuits. So, in this way we can take one smaller or from some smaller gates first we design another bigger module that can be the component of another bigger circuit.

So, in digital design there are some traditional elements and normally for bigger circuits or all real life circuits, these elements are being used these are some specific functionalities and these are being used. So, this class we read some of this type of elements, this we are calling that the common digital elements.

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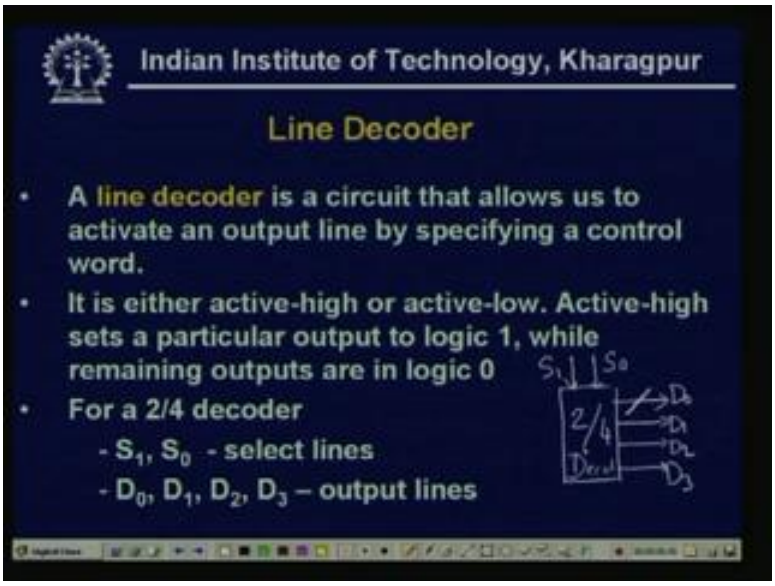

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Line Decoder

- A line decoder is a circuit that allows us to activate an output line by specifying a control word.
- It is either active-high or active-low. Active-high sets a particular output to logic 1, while remaining outputs are in logic 0
- For a 2/4 decoder
  - S_1, S_0 - select lines
  - D_0, D_1, D_2, D_3 – output lines

So, first when will read is a line decoder, so first we define what do we mean by a line decoder. Say line decoder or simply we can tell decoder is a circuit that allow us to activate and output line by specifying a control word. It is either active-high or active-low, means the output, output can be active-high or active-low. Active-high means, it sets the particular output to logic 1, while the remaining outputs are in logic 0, for a 2 by 4 decoder 2 by 4 means, so this is a line decoder.

So, what we can do see the for a line decoder, if we draw that see there are this block diagram level if we draw that thing, then there will be 2 control lines, we are telling these are S 1 and S 0 and output, there are 4 output lines these are D 0, D 1, D 2, D 3. Now, these are called the S 0, S 1 we are calling select lines. So, by applying a particular pattern in the S 1, S 0 lines we are calling the controllers to the select lines. What we can do, one particular output lines can be made high or low, so this is the function of the decoder, so this is my 2 to 4 decoder.

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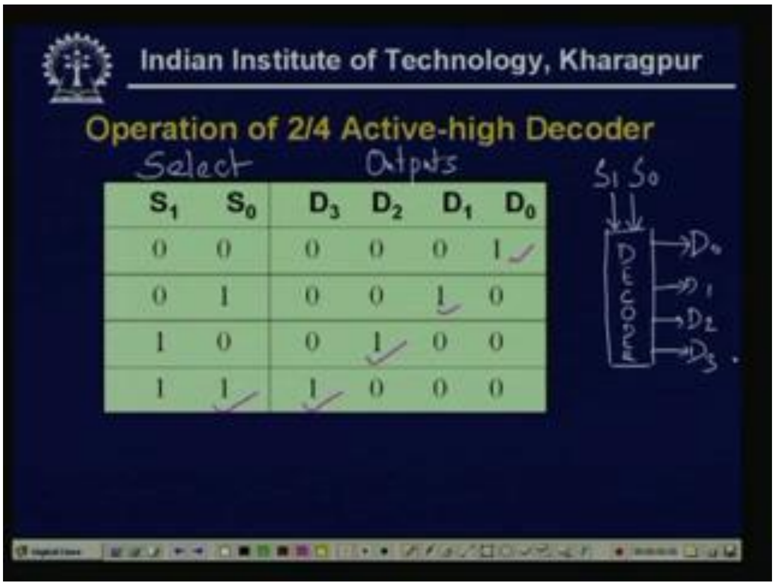

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Operation of 2/4 Active-high Decoder

Select		Outputs			
S_1	S_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1 ✓
0	1	0	0	1 ✓	0
1	0	0	1 ✓	0	0
1	1 ✓	1 ✓	0	0	0

Now, if we write the operation see we have again, that if I draw this is my decoder the 2 select lines S 1, S 0 and this is my D 0, D 1, D 2, D 3, see here one these are the control bits. So, these are my select lines, these are my output, now if we put 0, 0 in the select lines then D 0 will be active-high, if it is 0 1 then D 1 will be active-high, if it is 1 0. That means, S 1 is 1 S 0 is 0, then D 2 will active-high; that means, logic 1 active-high means this will be logic 1 and if S 1 0 is 1 1 then D 3 will be active-high.

So, this is the operation or what we can tell that again the input, output relationship because, my select line is nothing but, the input output relationship of this particular element. So, now we have to draw the circuit, so in the same way here there are actually has a 4 outputs and this is the 2 inputs. So, for 2 input I can draw the map and I can because, this is the retrieval situation and from there I can make the expression, but here it is very simple because, if it is 0 0 this is 1.

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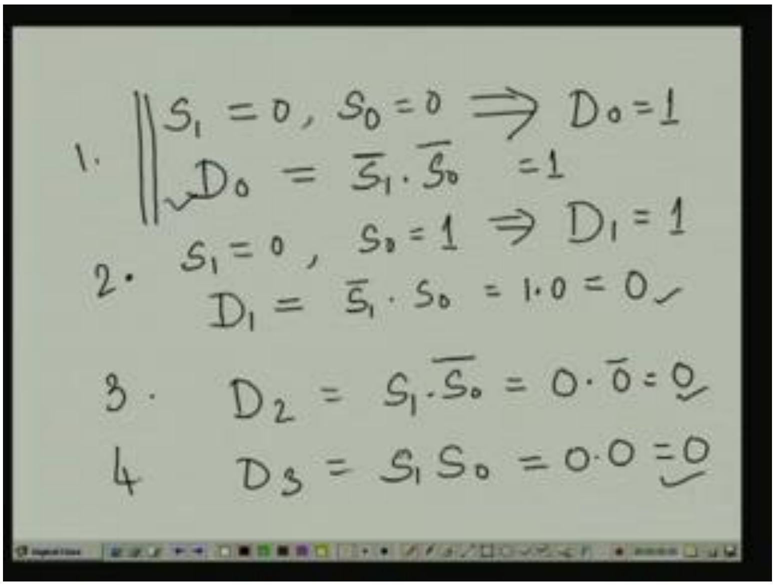

1. $S_1 = 0,\ S_0 = 0 \Rightarrow D_0 = 1$

$\checkmark D_0 = \overline{S_1} \cdot \overline{S_0} = 1$

2. $S_1 = 0,\ S_0 = 1 \Rightarrow D_1 = 1$

$D_1 = \overline{S_1} \cdot S_0 = 1 \cdot 0 = 0 \checkmark$

3. $D_2 = S_1 \cdot \overline{S_0} = 0 \cdot \overline{0} = 0$

4 $D_3 = S_1 S_0 = 0 \cdot 0 = 0$

So, how we can write that thing this is 0 0 this can be a see that S 1 is 0, S 2 is 0, then it is giving my D 0 equal to 1. So, I can write D 0 equal to S 1 sorry we have given S 0 S 1. So, this is S 0 I can put D 0 is S 1 bar dot S 0 bar, so this is the when S 1 equal to 0, S 0 equal to 1. Case 2 is S 1 is 0 and S 0 is 1, this proves that D 1 equal to... So, that means, D 1 is S 1 bar dot S 0 and in the similar way I can tell that D 2 is S 1 dot S 0 bar and D 3 is S 1 S 0.

Now, one thing is that when one particular output lines; that means, any one that D 0, D 1, D 2, D 3 will be active-high, then the remaining three must be active-low means that it will be logic 0. Now, see this is when 0 0 when D 0 is selected; that means, D 0 is 1. Then what is the status of D 1, D 2 and D 3 because, they must be 0, see that S 0 is 0, S 1 is 0 bar, so this is 1 dot 0 means this is 0 logic 0.

Similarly, this is S 1 is 0 and this is 0 bar, so this is 0 and this is 0 0, so this will be 0, so it is valid. And for the other cases also; that means, when the select line will be 1 0 here S 1 equal to 0 0, when it is D 1 will be high. So, D 1 will be high, when S 1 0 is 0 1 that time that other D 0, D 2, D 3 they will be logic low or logic 0, similar thing will happen for D 2, D 3 also.

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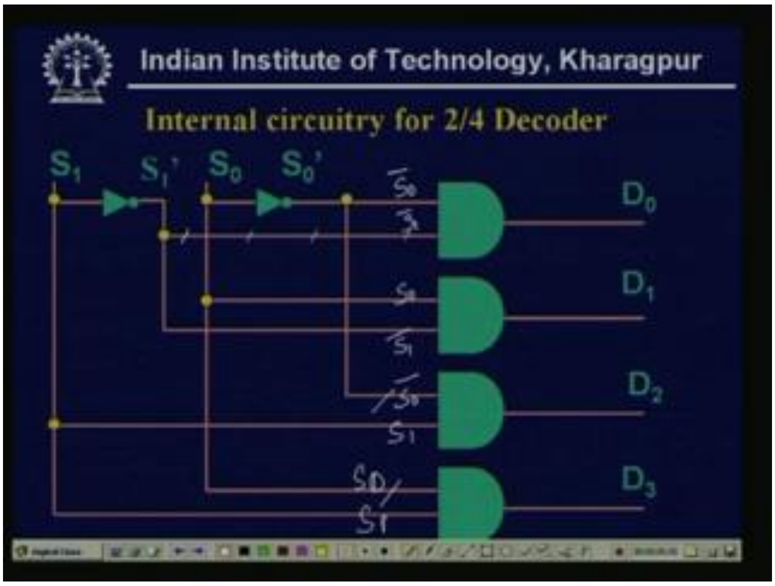

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Internal circuitry for 2/4 Decoder

So, the internal circuitry mainly does this thing, that this S 0 bar, S 1 bar, S 1 bar is 0, now see that the control circuit is like that, see here D 0 will be active-high or D 0 equal to 1 when S 1 bar is 0 bar. So, this see here S 1 is fed to 1 inverter; that means, this is my S 1 bar this and S 0 inverted, so this is my S 0 bar, S 1 bar, then D 0 will be 1. Similarly, D 1 this will be S 1 bar S 0, for D 2 this is S 0 bar because, the input is taken from the inverter output NOT gate, output of the NOT gate.

So, this is S 0 bar and this is simple S 1, whereas for D 3 this is as it is S 1, S 0 and S 1, so this is my decoder design a 2 to 4 decoder. Now, similarly what we can do for that 3 to 8 decoder we can then that time then it will be a 3 bit control line or 3 bit select line and that 8 bit output line; that means, it will it directs the path to anyone of the 8 bit. So, NOR output, normally this is a n to 2 to the power n decoder, we can design and the circuit will be similar.

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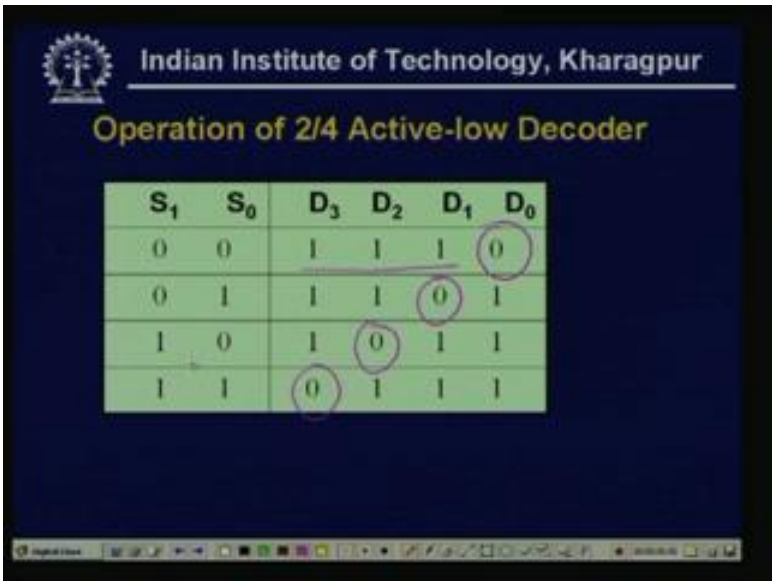

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Operation of 2/4 Active-low Decoder

S_1	S_0	D_3	D_2	D_1	D_0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

Now, if it is active-low, active-low means for the same select line or the same control bits on the select lines the one particularly output line will be active-low and remaining will be 0. That means, when S 1 is 0 is 0 0 that only D 0 will be 0 and all D 3, D 2, D 1, will be 1, similarly when S 1, S 0 is 0 1 only D 1 will be 0 remaining 3 outputs are 0, when it is 1 0 D 2 will be 0, when 1 1 then D 3 will be 0 and the same thing applies.

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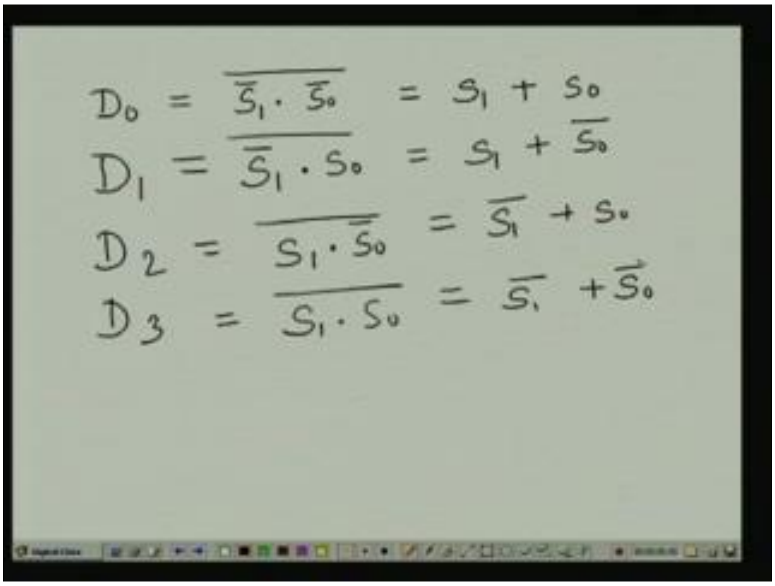

$$D_0 = \overline{\bar{S}_1 \cdot \bar{S}_0} = S_1 + S_0$$
$$D_1 = \overline{\bar{S}_1 \cdot S_0} = S_1 + \bar{S}_0$$
$$D_2 = \overline{S_1 \cdot \bar{S}_0} = \bar{S}_1 + S_0$$
$$D_3 = \overline{S_1 \cdot S_0} = \bar{S}_1 + \bar{S}_0$$

Then, what will be the circuit see now the circuit is see if we can draw; that means, now what about the D 0 functions. So, D 0 functions will be S 1 bar dot S 0 bar overall complimented because, earlier it was active-high now it is simply the active-low means 1 bar. And for the active-high decoder in the last case when we have consider for the D 0 the select line was S 1 bar S 0 bar. So, it is complement of S 1 bar dot S 0 bar which is nothing but, S 1 plus S 0; that means, the OR.

Similarly, the D 1 will be the S 1 bar S 0 that bar; that means, S 1 plus S 0 bar D 2 will be S 1 dot S 0 bar complement of; that means, and D 3 will be S 1 dot S 0 bar means S 1 plus S 0. Now, we can see that or we can notice that thing that mainly that for active-high, the select line or the output expression when the select line are of the inputs are changed for the active-high it was AND and for the active-low it becomes the OR. Another thing for D 0 the input variables, where complemented where here the input variables have become uncomplemented.

And the total reversing we are getting because, for the active-high decoder the input variables where uncomplimented and AND gate. Whereas, for the active low decoder the input lines are complemented and the AND becomes OR, so these are this is the situation.

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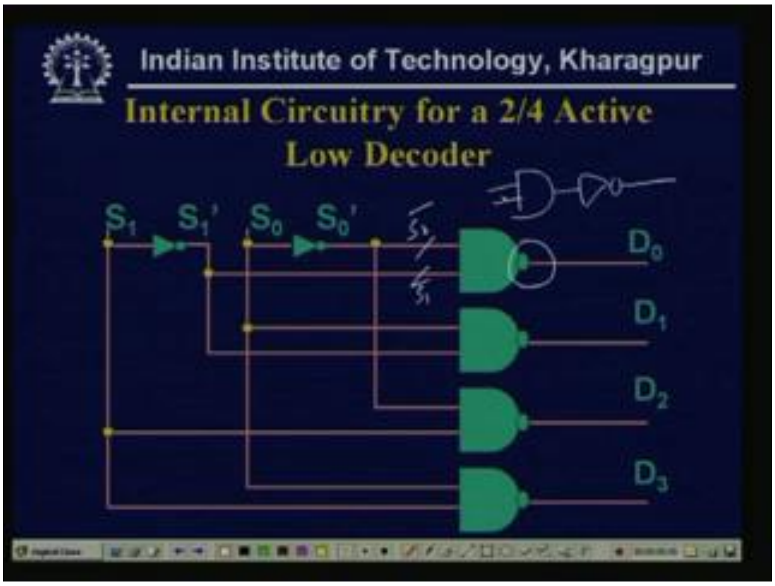

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Internal Circuitry for a 2/4 Active Low Decoder

Now, we see that how where, when it is designed actually as if that same select line is given, see for this thing that S 1 bar, S 0 bar. So, here we have given S 0 bar, S 1 bar as simply that from either case. That as if D 0 is complemented because, it was active-low means that for the active-high case it was one was generated as if this one becomes 0, so it is complemented. So, the circuit remains as it is only the AND becomes the NAND; that means, every AND now changed is a AND followed by a inverter which is nothing but, a NAND circuit.

Because, as if the only the last output line has the complemented… So this is the simple modification or with the simple change that active-high 2 to 4 active high decoder can be changed to active-low decoder.

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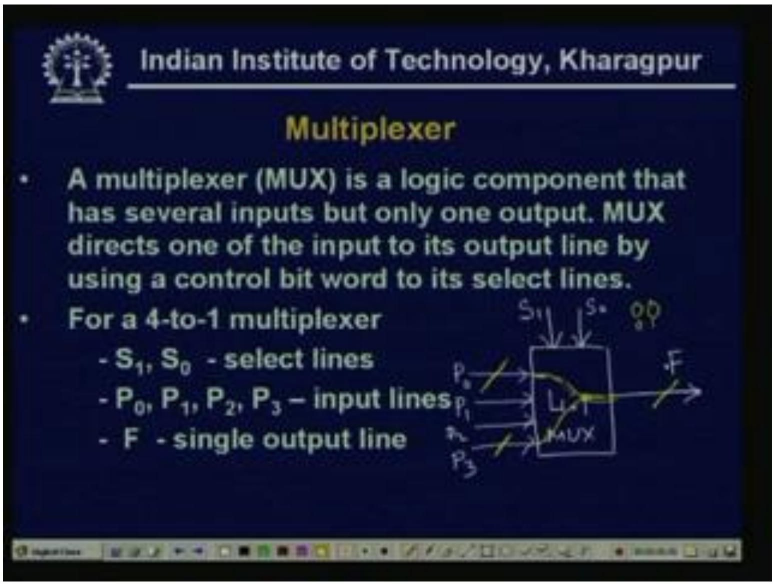

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Multiplexer

- A multiplexer (MUX) is a logic component that has several inputs but only one output. MUX directs one of the input to its output line by using a control bit word to its select lines.
- For a 4-to-1 multiplexer
  - S_1, S_0 - select lines
  - P_0, P_1, P_2, P_3 – input lines
  - F - single output line

Now, the second element we see the digital element which is a multiplexer. First we define a multiplexer normally in short form it is called a MUX is a logic component, that has several inputs. But only 1 output. MUX directs one of the input to it is output line by using a control bit word to it is select lines. So, if I draw a block diagram see say I am taking a 4 to 1 multiplexer; that means, there are 4 input lines, this is a 4 to 1 MUX. And there are select lines like the decoder, so this is a 2 select line and there is only 1 output line.

Now, the function is that if we apply a particular control word to the select lines S 1, S 0 then the one particular input will be directed to the output. So, when we change the control word to the select line, the directed inputs to the output will also be changed. So this is the function of the multiplexer. See, if we take the S 1, S 0 equal to 0 0 then we are selecting the P 0 lines, where the P 0, P 1, P 2, P 3 we have taken as the input lines, then P 0 is directed to output.

That means, whatever value I will put as the P 0 input line that will be that I will get to my output F. Similarly, it can be 0 1 1 0 or 1 1, so if S 1, S 0 is 1 1 then whatever input is applied to P 3 that with be directed to the output F. So, this is the function of multiplexer.

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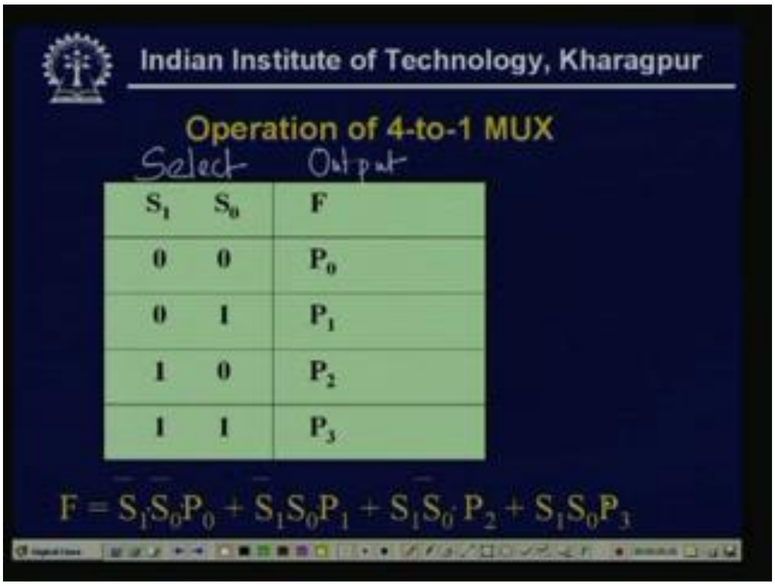

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Operation of 4-to-1 MUX

Select Output

S_1	S_0	F
0	0	P_0
0	1	P_1
1	0	P_2
1	1	P_3

$$F = \bar{S}_1\bar{S}_0P_0 + \bar{S}_1S_0P_1 + S_1\bar{S}_0 \cdot P_2 + S_1S_0P_3$$

Now, if we do this operation explain then again this is my select lines or control bits, this is my output. Now, how the what is the input, output relationship, so when S 1, S 0 is 0 0 output is nothing but, P 0, 0 1 output is P 1, 1 0 output is P 2, 1 1 output is P 3. So, then now if we write see that I am writing the expression for the output F, so F I can write that S 1 bar S 0 bar, the 0 bar this is 1 that time P 0 will be my output. So, S 1 bar dot S 0 bar dot P 0 plus S 1 bar S 0 for the second case means P 1 and dot P 1, S 1 is S 0 bar dot P 2 S 1 is S 0 dot P 3.

See, for the decoder four select lines or the four control words apply to the select lines that are same only on each cases, which input line is directed to the output that has been ended with the each min term, so we got this expression for the output.

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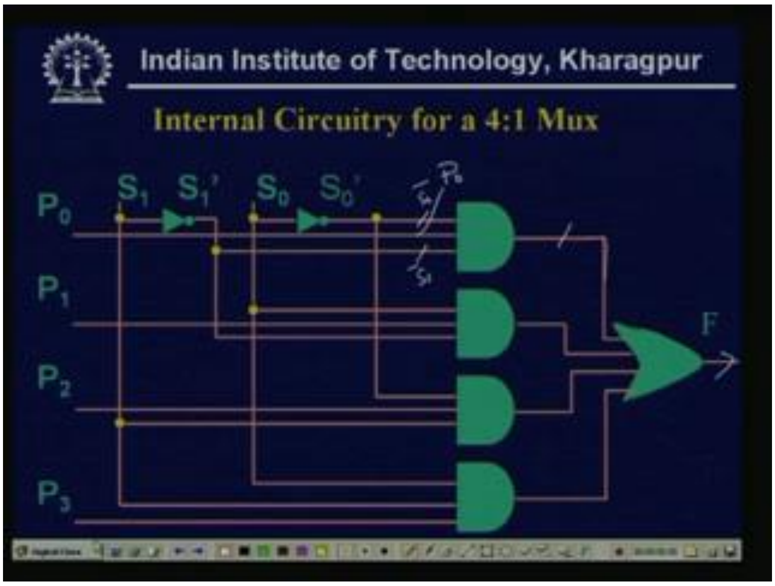
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Internal Circuitry for a 4:1 Mux

So, the circuit will be, so that simple realization of the AND, OR and as there are some complemented input variables, so some inverter is applied to the input. Now, this is the similar circuit for the decoder here that for the first AND gate, this is output our input should be S 0. See that here the input of the AND gate this is S 0 bar, this is S 1 bar and this is my P 0. So, this is for actually that first input directed to the output, similarly that for other 3 inputs or the other AND gates it will happen, so this is a simple circuit which consists of AND gates, OR gates and some inverter.

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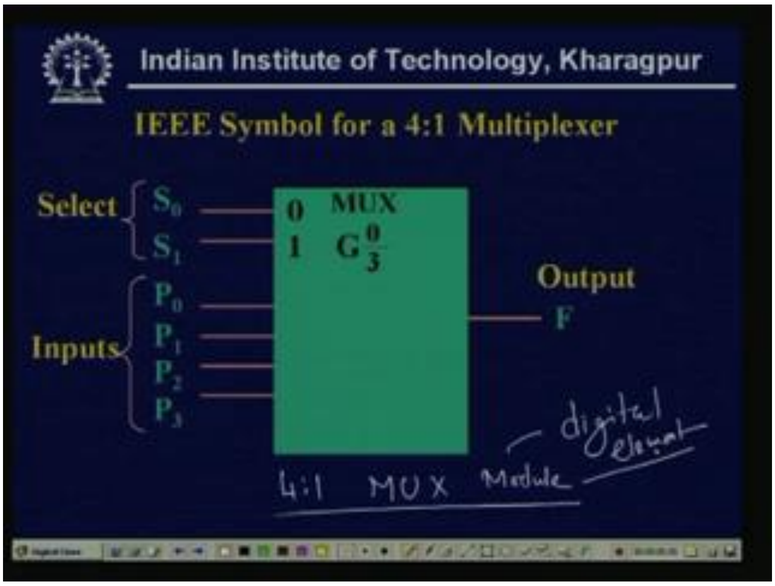
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IEEE Symbol for a 4:1 Multiplexer

Now, these are 4 to 1 multiplexer we can treat this as a module and for my larger design or bigger circuitry design I can use this multiplexer as a smaller module, as if this a basic building block of my design. And this is what, this is very standard, so the IEEE symbol for a 4 by 1 multiplexer is like this thing, so there are this is one box, whereas if there are 6 inputs, the 4 are the basic inputs and these are the select lines, again select lines also I am applying my control signals. So, there are treated as a input and 1 output line.

So, this is my as if this is one module this is one 4 to 1 MUX module, so for larger circuit design I can take this as the digital element, that is why we are calling this is also digital element.

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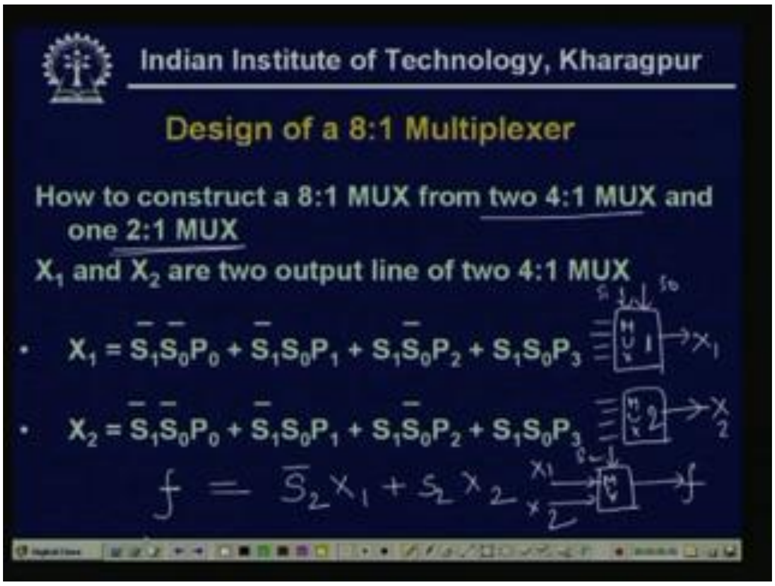

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Design of a 8:1 Multiplexer

How to construct a 8:1 MUX from two 4:1 MUX and one 2:1 MUX

X_1 and X_2 are two output line of two 4:1 MUX

- $X_1 = \bar{S}_1\bar{S}_0P_0 + \bar{S}_1S_0P_1 + S_1\bar{S}_0P_2 + S_1S_0P_3$
- $X_2 = \bar{S}_1\bar{S}_0P_0 + \bar{S}_1S_0P_1 + S_1\bar{S}_0P_2 + S_1S_0P_3$

$f = \bar{S}_2 X_1 + S_2 X_2$

Now, we consider a 8 to 1 multiplexer and we noticed that how these 4 to 1 multiplexer can be used to design a 8 to 1 multiplexer. So, for to design a 8:1 multiplier we need other the two 4 to 1 multiplexer, see the two 4 to 1 multiplexer and one 2 to 1 multiplexer. First, we say as if because it is a 8 to 1 multiplexer how do I know, how do I select that how many multiplexers will module will be needed.

See here 8 to 1 multiplexer means, there are 8 input lines and for 4 to 1 multiplexer there are 4 input lines. So, at least 2 multiplexer I need to apply my inputs, so I have got that two 4 to 1 multiplexer, now for each multiplexer there is 1 output line, so for two I have identified them as the X 1 and X 2 are the 2 output lines of the 2 multiplexers. Then, I can define them, already I know that expression for 4 to 1 multiplexer and what was that that if it is a say if it is number 1 this is a 1 MUX 1 this is my MUX 1.

So, again P 0, P 1, P 2, P 3 and output is X 1, similarly here it is MUX 2 P 0, P 1 and this is X 2. So, I can write X 1 is S 1 bar S 0 this is my S 1, S 0 bar P 0, S 1 bar S 0 P 1, S 1 S 0 bar P 2, S 1 S 0 P 3. Similarly, for the second MUX also the expression will be same only output line is X 2, so X 2 is S 1 bar S 0 bar P 0, S 1 bar S 0 P 1, S 1 S 0 bar P 2 S 1 S 0 P 3. Now, that the final output of the 8 to 1 multiplexer will be that f equal to say I am taking another select line S 2 bar X 1 plus S 2 X 2.

That means, another 2 to 1 multiplexer this is a MUX, where only 2 input lines will be 1 select line and 1 output. This I am calling f and the inputs are X 1, X 2 select line is S 2, then this is my expression.

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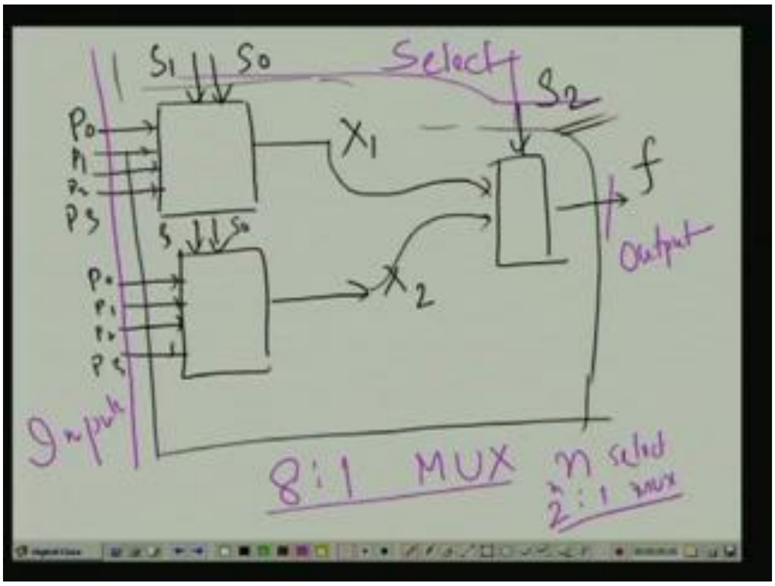

So, if I redraw that thing what will happen that I need 4 to 1, so these are S 1, S 0 and P 0, P 1, P 2, P 3 this is my X 1. Similarly, I need another 4 to 1 same P 0, P 1, P 2, P 3 these are all inputs S 1, S 0, now as if another 2 to 1 and this is f and this a separate select lines. So, this f will be that overall; that means, see there are 8 inputs 3 select lines, so these are my inputs, these are my select lines, this is my output, so this is a 8 to 1 MUX where three select lines are needed.

Normally, that in general that if it is n bit select lines, then input should be 2 to the power n. That means, 2 to the power n is to 1 MUX, for 2 to the power n each to 1 MUX n select lines will be needed.

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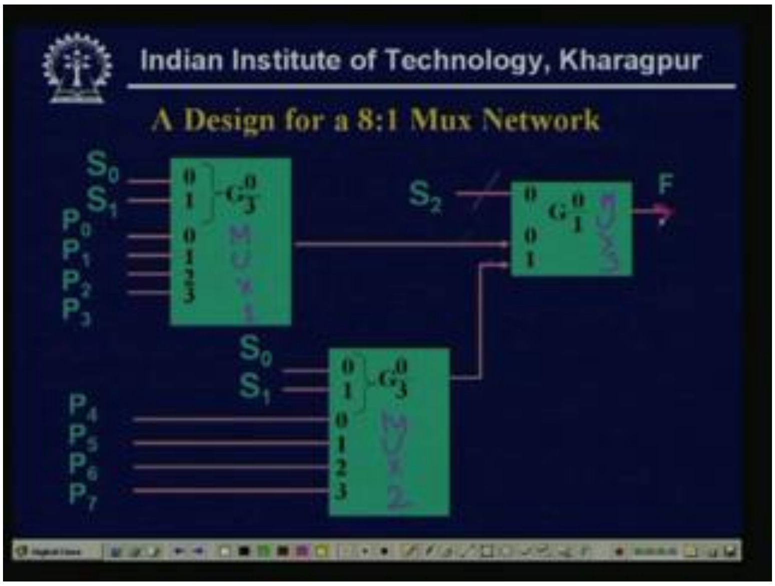

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A Design for a 8:1 Mux Network

Now, this is the just now what we have drawn, that if from that IEEE convention if we maintain, that this is the conventional MUX module that 4 to 1 2 MUX module, where that S 0, S 1, are two select line P 0, P 1, P 2, P 3 are 4 input lines for the first MUX. This is my MUX 1, this is my MUX 2 and this is my MUX 3. That output of the for 2 to 4 to 1 MUX, these are the inputs and another select lines are there and this will be my output F 2.

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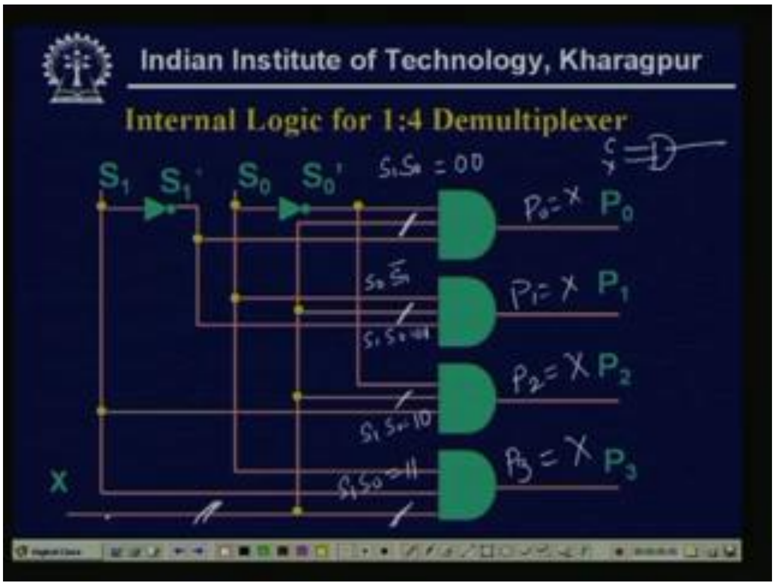

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Internal Logic for 1:4 Demultiplexer

Now, this is internal logic for 1 to 4 de multiplexer, now multiplexer is there are several input lines, but only one output line, now here the total reverse thing is there. So, if we define the operation here the select lines will be if for the n select lines only one input line will be there and there will be several output line. And for application of a specific control bit word to the select line, we will direct the input to a particular output. So, this is the reverse operation of the multiplexer and that is why it is called a de multiplexer.

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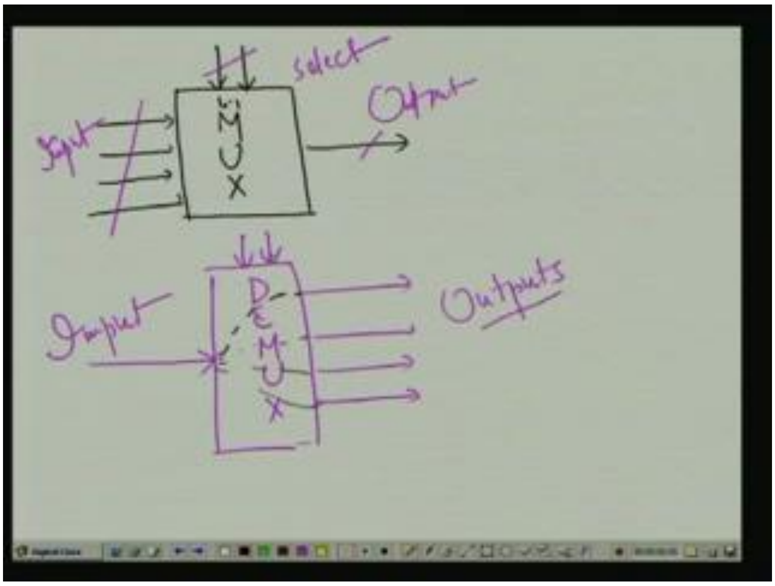

So, if we see that; that means, for multiplexer there are say, if we consider again that 4 to 1 MUX. So, this is a 4 to 1 MUX 4 input lines will be there 1 output line. So, these are my multiple inputs, single output select line will be n, now if it is DEMUX see it will be totally reverse thing, as if I am applying the input here. So, one single input select line will be as it is and the output, several output will be there, so these are my outputs.

That means, in this case the only one single input and depending on the value or the control bit at the select signals of the select lines. That in particular input will be directed to different type of or different output lines depending on the select lines. ((Refer Time: 48:36)) Now, if we see the internal circuitry, see always that 1 input is there, that is my X input.

Now, this X is fed to as the input of all the AND gate and the output of the AND gates are P 0, P 1, P 2, P 3. Now, depending on the other inputs of the AND gate, whether the P 0 will get; that means, here P 0 will be XOR not that will be there, here P 1 equal to X, here P 2 equal to X, here P 3 equal to X.

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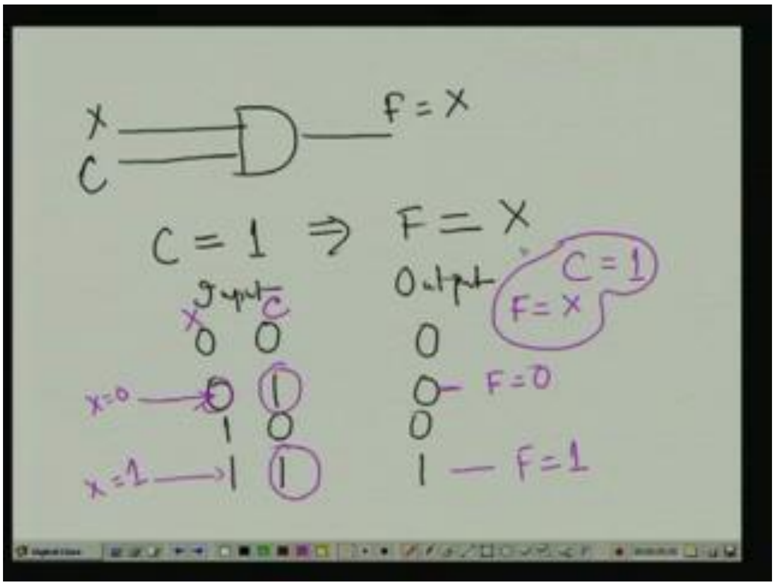

Now, one small circuit we see 1 small AND gate, we take one small AND gate see here I am giving X and here I want my F should be X, when I will be getting that thing. When these input say this is my control input C, when that C equal to 1. That time I will be getting F equal to X why, because if I remember that the truth table for the AND gate then 0 0, if are the 2 inputs this is my output, then this is 0, 0 1 0 1 0 0 1 1 1.

Now, see when that this 2 inputs think that as if this is my X and this is my C, now when C is 1 means C is 1, this is C is 1, C is 1. See, what value I am giving X here X equal to 0 that I am getting as output; that means, here X equal to 0 this situation X equal to 0. I am also getting F equal to 0, this situation when C equal to 1 I am giving and X equal to 1 here also I am getting F equal to 1. So, what I can from here what I can infer that 2 input AND gate, if one of the input is 1. That means in this case if C equal to 1 than whatever value I will give to X, I will get the output as it is; that means, my F equal to x, so this is called the gated output.

That means, I am controlling whether which one I will pass, when C whatever C value C is 1, whatever value I will be giving to X that will pass. See, here in my de multiplexer actually I want that thing ((Refer Time: 52:20)) whatever value I want to give here X that X I want that to be passes as P 3 or P 2 or P 1 or P 0. So, that means, when P 0 equal to X my here there is instead of that an example I have given that gated AND C and X that only 1 input here it is 2 input, but the 2 input should be 1.

So; that means, together the combination of this is 0 S 1 together it will be 1. So, if it is S 0 bar S 1 bar and when S 0 S 1 equal to 0; that means, for the first P 0 case that when S 0, S 1, S 1 S 0 is 0 0 then S 1 bar is 0 bar is 1 and I will get P 0 equal to X. Now, here the inputs are in this case the inputs are S 0, S 1 bar, so if I put S 1, S 0 if for these I put S 1, S 0 as 0 1 then it will be P 1 will equal to X because, these are one. Similarly, here it will be S 1, S 0 equal to 1 0 and here S 1, S 0 equal to 1 1, then this is P 2 equal to X here P 3 equal to X.

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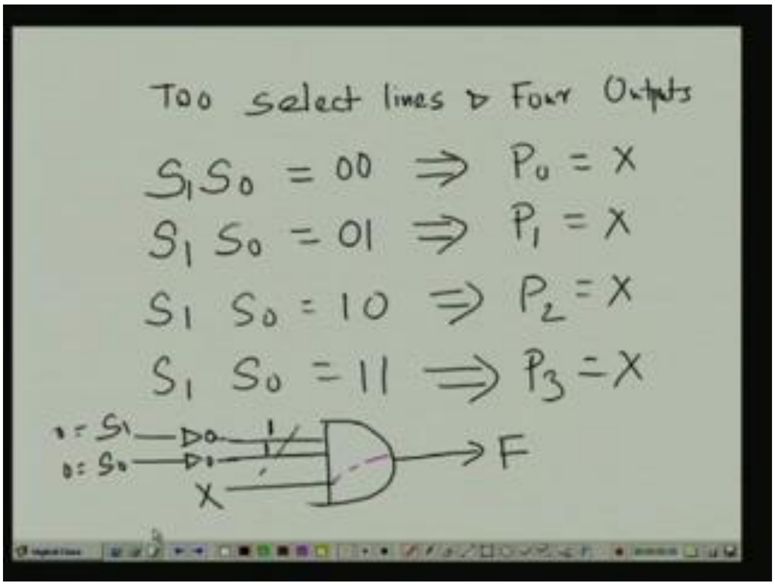

Too select lines ⊳ Four Outputs

$S_1 S_0 = 00 \Rightarrow P_0 = X$

$S_1 S_0 = 01 \Rightarrow P_1 = X$

$S_1 S_0 = 10 \Rightarrow P_2 = X$

$S_1 S_0 = 11 \Rightarrow P_3 = X$

That means, if we summarize that if I have two select lines and 4 output lines. Then S 1 S 0 equal to 0 0 will make P 0 equal to X, S 1 S 0 equal to 0 1 will make P 1 equal to X, S 1 S 0 equal to 1 0 will make P 2 equal to X, S 1 S 0 equal to 1 1 will make P 3 equal to X. And that time that to make S 1 I am putting S 1, S 0 0 0, but I want the AND gate these are the 2 input say this is my X, I want my X to be gated.

So, I want this thing, so together this should be one, so here it will be as it is 0 0; that means, it should be 1 because it is AND gate. So, this should be 1 this should be 1, so if it is 0; that means, my S 1 is S 0 if it is 0 0, then 0 bar 1 0 bar 1. So, it will be 1 and then as it is the 1 input is as it this 2 together S 1 is 0 together will be treated as 1 input of the AND gate that is 1. And so whatever value I will give to X that will be as it is passed to the output F.

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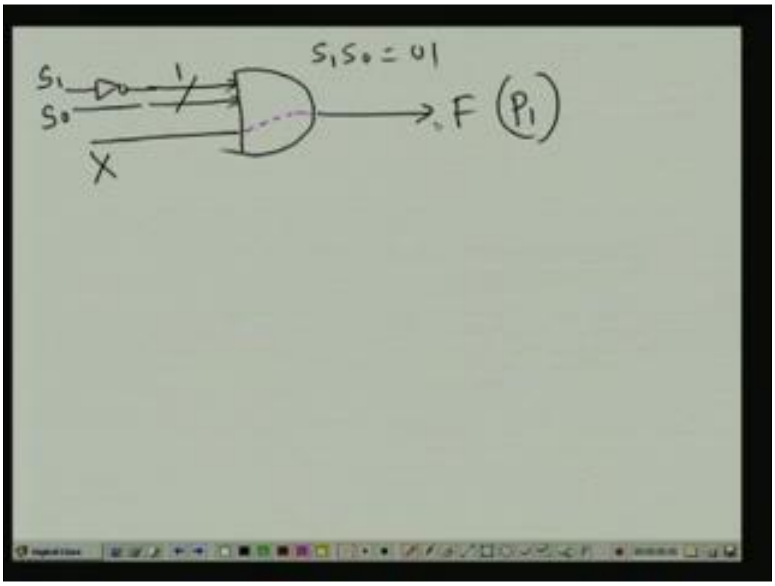

And similar thing will happen for three other situations that for the P 1 again this is my X F means my P 1. And here again I want the 2 input together as 1, so is I have given the situation select control bits to the select lines as 0 1. So, S 1 bar, so this is my S 1 bar, this is my S 0. Because, here S 1 is 0 is 0 1, then that X will be passed as ((Refer Time: 58:53)) similarly passed to P 2 or P 3 and in this way we can design the circuits. So, I want to end this class here.

Thank you.