Digital System Design
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Lecture - 11
Hazard Covers by K-Map

Let us first… I want to discuss the previous days quiz.

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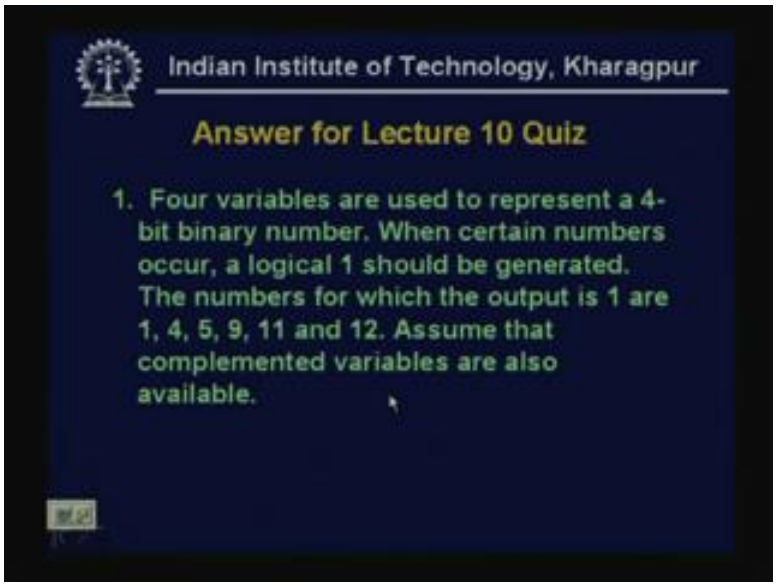

There was only one question for the last lecture and the question was that one, 4 variables are used to represent a 4 bit binary number when a certain numbers occur a logical 1 should be generated. And the numbers are 1, 4, 5, 9, 11 and 12, assume that complemented variables are also available, then reduce the expression.

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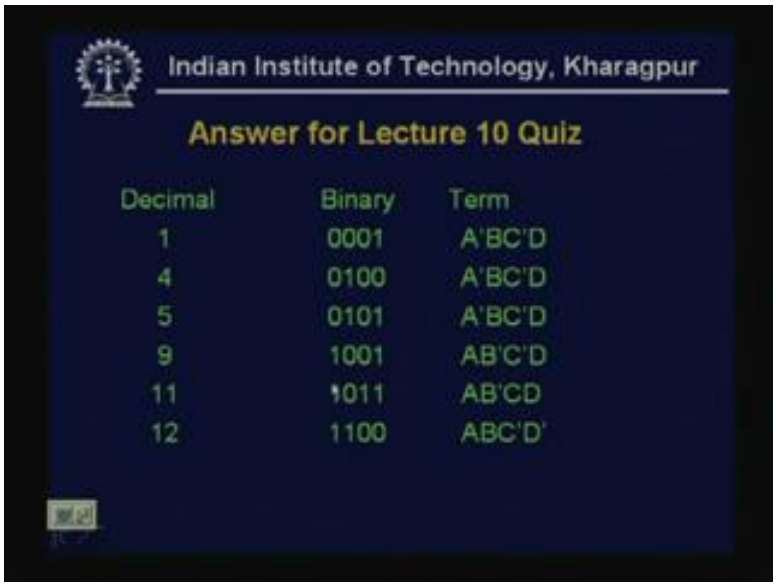

So, the numbers are for which the output should be one, the decimal values are 1, 4, 5, 9, 11 and 12. So, first we convert the decimal to numbers to binary, so 1 means 0 0 0 1 as already it is mentioned it is a 4 variable function. Similarly, 4 is 0 1 0 0, 5 is 0 1 0 1, 9 is 1 0 0 1, 11 is 1 0 1 1 and 12 is 1 1 0 0. Now, the terms will be or the means terms will be 0 means complemented variable 1 means uncomplemented. So, 0 0 0 1 that means, for decimal value 1 it will be A dash B dash it will be B dash then C dash D, so it will be B dash C dash D.

Similarly, for 4 it will be A dash B C dash D dash, for 5 it is A dash B C dash D 1 0 1 0 1, for 9 it will be A B dash C dash D, 11 1 01 1, so A B dash C D. One means that as for A C D that particular minterm and the binary values it is 1 1 1, so they are the 3 variables are uncomplemented 1. And as only the 1 it is for B, so it will be B dash in the minterm, similarly, 12 will be1 1 0 0 means, A B C dash D dash. So, these are terms, so that means, in the expression that the sum of these means terms will be there.

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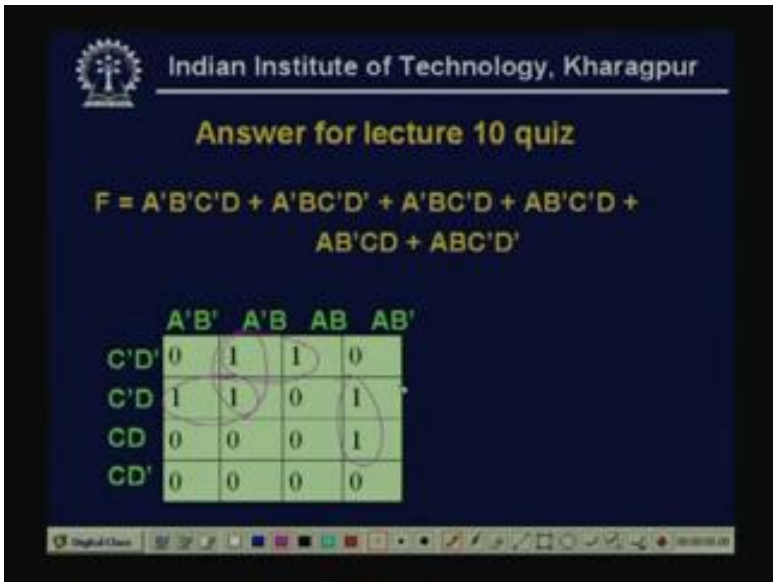

So, F will be that if first this will be the expression that means, that previous terms all the previous terms will be there and these are the five terms. Now, if we draw the Karnaugh map then that there are for this 5 minterms there will be 5 such there are 6 means terms there are 6 minterms, their will 6 1's and these are the positions. Now, if we do the couple or quart or the opted whatever be the things. So, here it will be only the it will be only couple say, if we see that this will be it will be one couple, this will be one couple this will be another couple and this will be couple. So, there are four couples exist, now if we put that thing then the sum will be.

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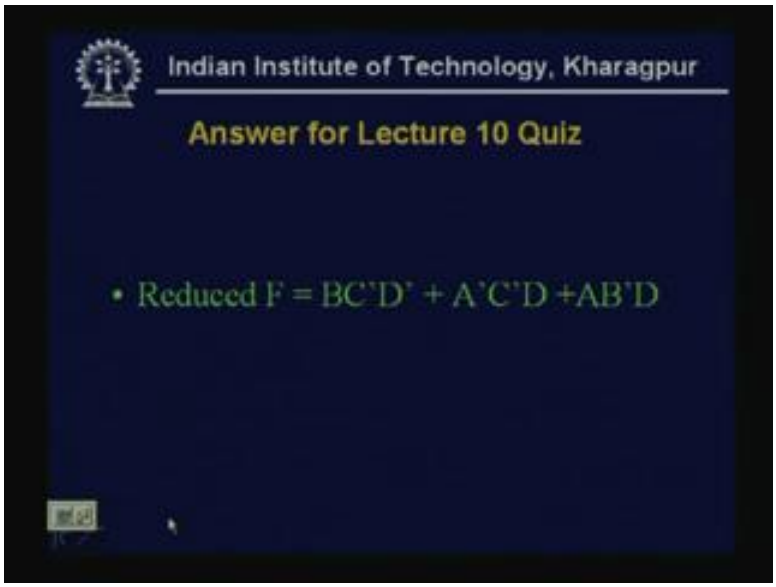

That B C dash D dash plus A dash C dash D plus A B dash D why these are 3, because see here one is already covered. That means, say when we have for the we have considered one couple. Here, we have considered one couple here, then already this 1 is covered in the C A dash C dash D. And here, this 1 is covered in the B C dash D dash. So, this is actually a redundant 1, so this is the this easily we can reduce and that is why there are only three terms and this is for the A B dash D this term is for the A B dash D.

So, we got the expression that A B dash D and for the previous two couples B C dash D dash plus A dash C dash D. Now, we start the today's thing that how we can cover the hazards by Karnaugh map method.

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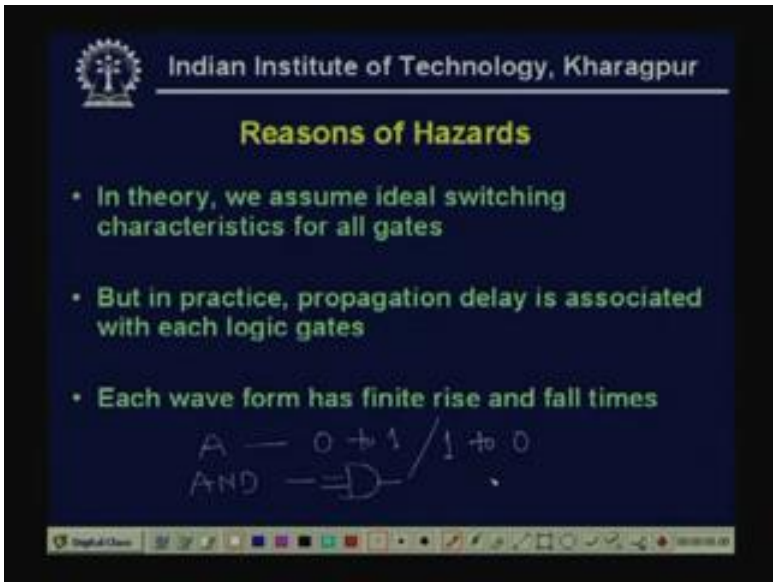

Now, first thing is that what do we mean by hazards and what is the reason for hazards. Now in theory or, so far the we have discussed in the previous classes we assume that, ideal switching characteristics for all gates. Or the operator that we have consider that AND OR and the inverter there we have assume that, it is a ideal switching that mean when it is what do we means by switching, switching is that when it is changing from 0 to 1, say it is that some value1 variable A it is changing 0 to1 or 1 to 0.

Then it is taking almost no time, so this is a switching and we call this is a ideal switching. But in practice the propagation delay is associated with each logic gates means, when say this is a AND mean if it is it can be AND gate. This can be say, simple case to input AND gate or this can be a dot operation.

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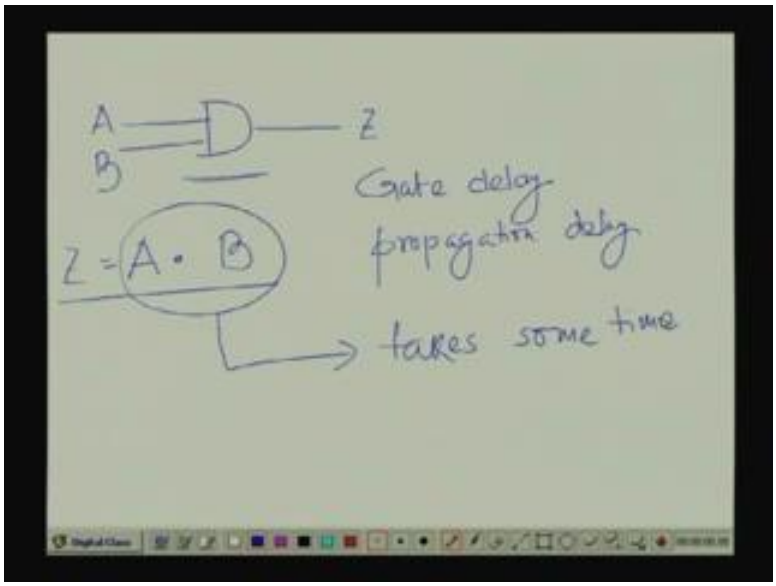

Now, whatever be the thing say, say I am taking this is a two input AND gate or this is a A dot B, this is a A dot B operation, so Z equal to A dot B operation. Now, in practice or in real life it will take some time, now this we are calling for gate we are calling this time is the gate delay or the propagation delay. Now similarly, if we consider this operation just to execute this A dot B it will also take some time and that is also the delay of this takes some time that is called the delay. So, that we are calling that logic gate is associated with some delay, now each wave form has finite rise and fall times what do we mean.

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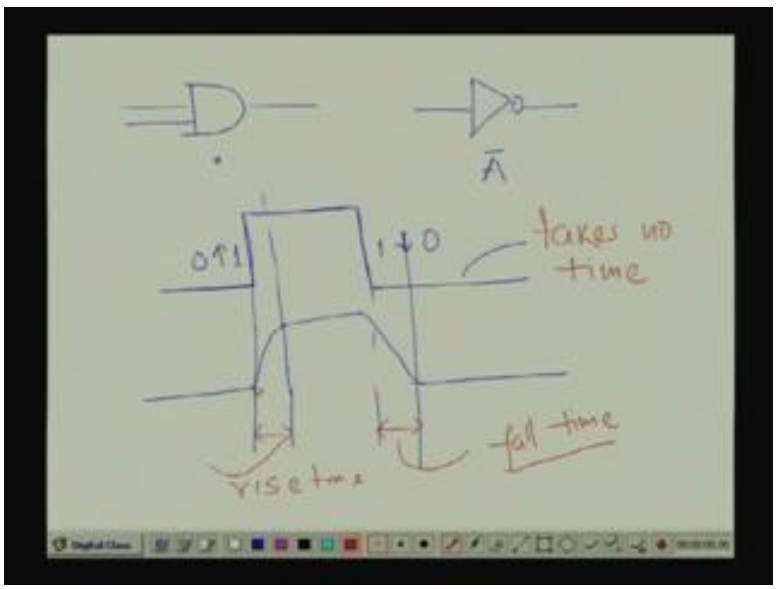

See, so just now what we have drawn see whether it is AND gate or whether, it is a inverter, it is taking some time to do this operation to this AND or to do this inversions. Now, say ideal switching means say, if I take that this is a say here it is a 0 to1 switch, here it is a1 to 0 switch, now this is the ideal situation as if this 0 to1 or 1 to 0 it is not almost it takes no time. So, I can tell that takes no time for this switching, but in real life situation this take actually, it is it takes some time then again here it will be like this that mean, here its starts, but at least it takes this amount of time.

So, here this is the time it needs for this rise and this is time it needs a fall, so these we are calling the rise time this we are calling the fall time. Now, in real life it the some if this is x axis is the time axis, then it takes some finite time for the this switching from 0 to1 or it is from1 to 0. Now, for this reason that as the each gate is taking some time for the its execution or it we what we have defined as a delay, and sometimes this creates a problem in real life circuit.

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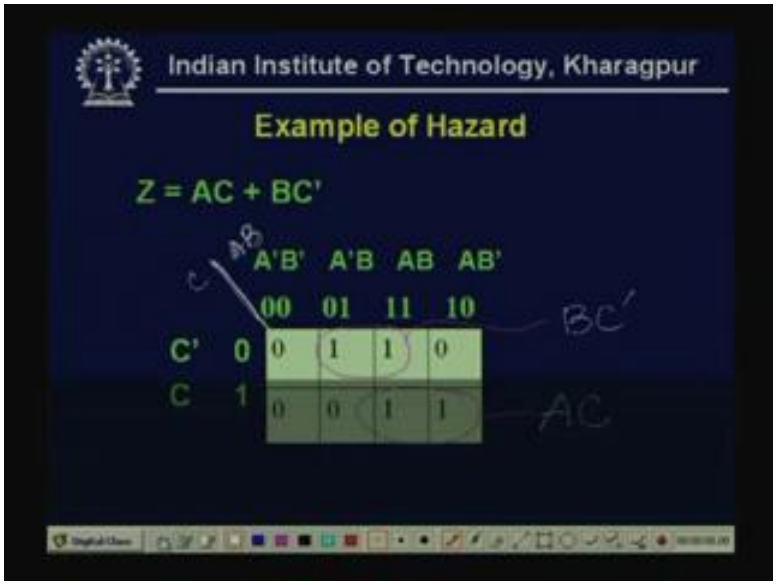

Let us take an example and of hazards, so this problem we are defining as a hazard and that.

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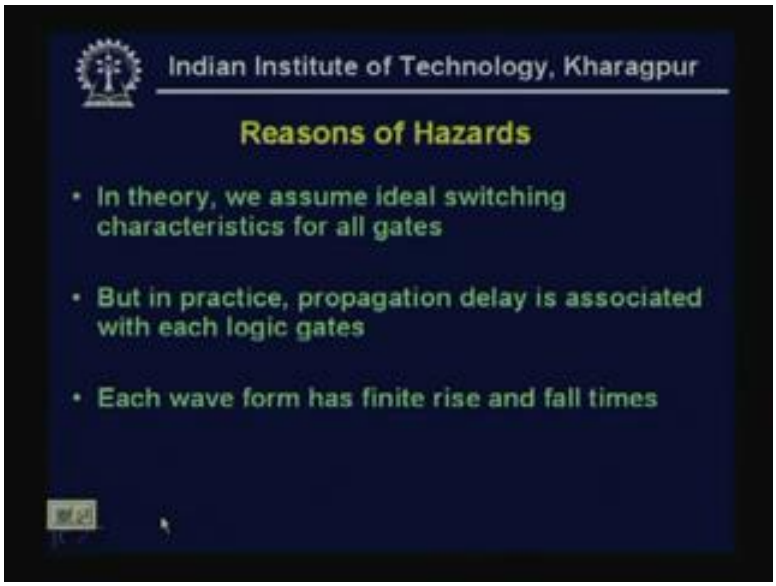

This is the reason for the hazard that the time or the delay it is taken ((Refer Time: 12:12)). So, let us take an example, say Z equal to A C plus B C bar, these are three variable expression. Now, if we draw the Karnaugh map, for this expression Z, then how we see, say our thing is that, here. I am taking that, the upper portion I am taking, the A B variable and this is my C variable, so here the, four terms will be A dash B dash, A dash B, A B, A B dash and C dash, C.

So for A C term, A C plus B C dash, so this can be a, say here, for A C dash, this can be a realization. See here, this is, this for B C dash means, for this couple, this is a, this represents a, this represents B C dash and these represents A C. So, this is my BC dash and this is my AC.

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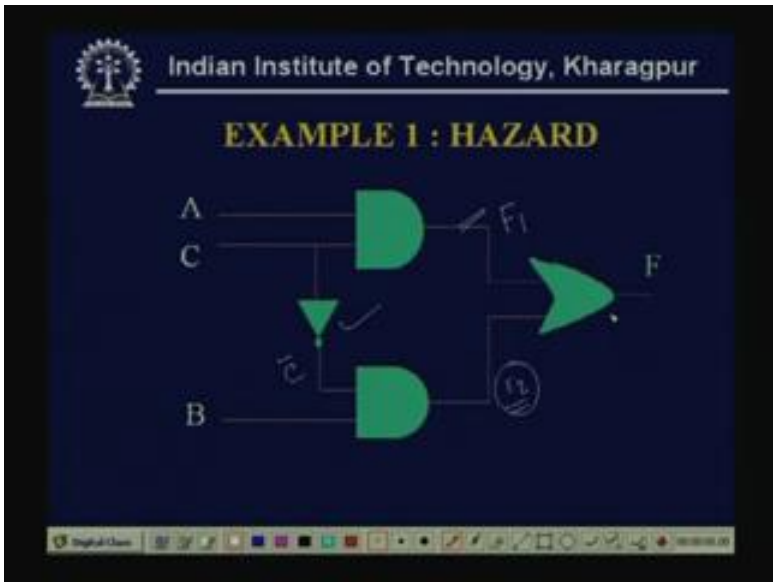

Now, if we draw that logic circuits, see this is an second AND gate, whose inputs are A and C and B and C dash. So, C dash I am taking the, as if the input is coming from C and by introducing a inverter in between. So, this input is actually, this is C, this C, this is C bar. So, this is my C bar and this is OR, that means, this is my F equal to A C plus D C bar. Now, see, here when that A C is, for the first gate or the top AND gate, the, when it is executing A C then, say just to compute C bar, because for that gate delay associated with the inverter, it will take some time to compute this thing.

So, when this input of the OR gate is available, say this is my F 1, this is available, that time F 2 is not available, because these inverter is taking some time to compute C bar and then DC bar is computed after sometime for this delay and again some delay is associated with the bottom AND gate also. So, F 2 will be there, but think that when F1 is available, that times some signal value is available here in this line. That means, the second input of the OR gate, whether it is a correct F 2 or not, that we will see. And if it is not a correct F 2, then it will give a problem and that we are telling as a, this a hazard of the circuit.

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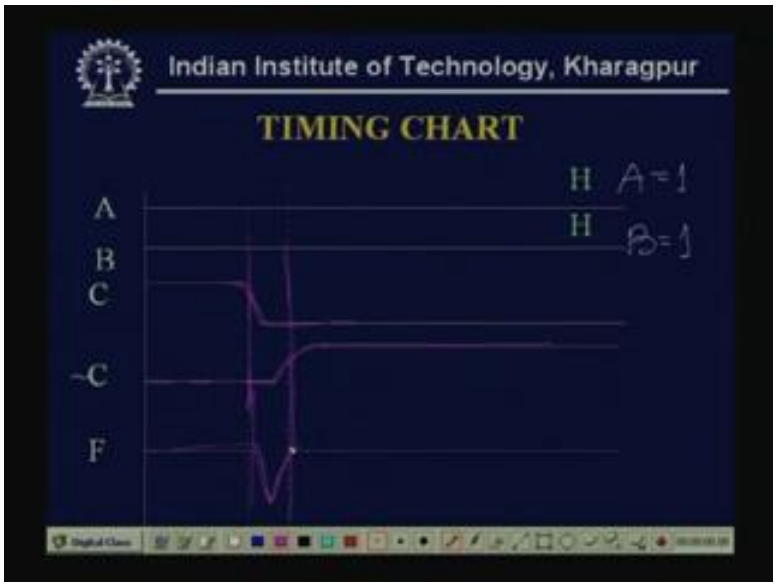

Now, if we see the timing diagram of the timing chart of this particular circuit, say I am taking A and B both are high. So, this is, that means, A equal to1, this is A equal to1, here B equal to 1. Now, C is switched, because C is the input of both the AND gate, now initially C is high, now here C is taking some value, say C is here, C is falling. Now, S for the delay of the inverter, immediately C dash will not be available or C dash will not be computed, C dash will be available after sometime, see it takes this time.

So, actually, C is fed here and C dash is available, say this is my C dash, so in between this time, that means when C switches or C becomes 1 to C, if C is1, C dash become 0 or when C switches to1 to 0 and for C dash becomes 0 to1. In between these, that output of the F, there will be a glitch in the output of the F and this we are defining as a hazard. So, if we consider the timing chart, this is a reason why we are getting a undefined output or not the correct output at this stage, when the C is switched.

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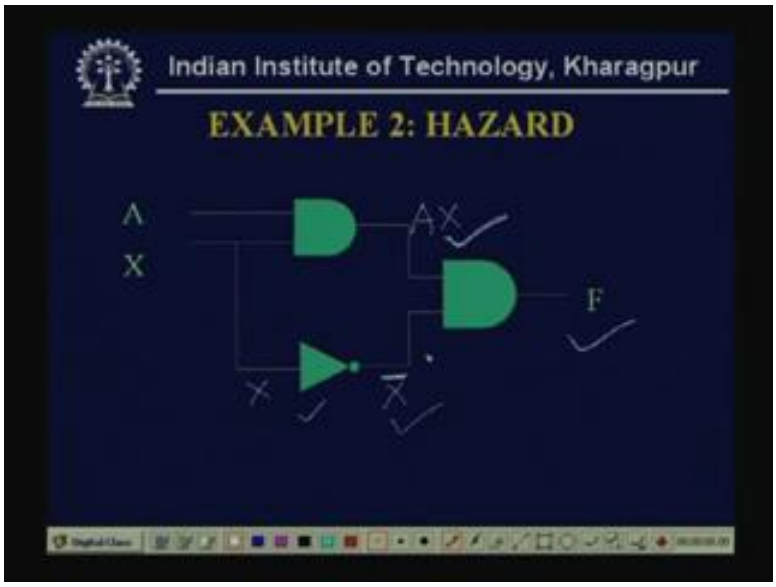

Now, again if we take another small example, say one AND gate, this is one AND gate, where whose inputs are A and X and another inverter, was simply, X is being inverted. So, this is my in output, X complement, here this is my X and this is again A X, this is A X, now what will happen? See that, if the delays are different or if the delays are same, the delays of the this AND gate and the delays of this inverter, because the output of the first AND gate and the output of the inverter or the two simultaneous inputs of the next AND gate.

So, if the two delays are same, initially, first we think that these two any delays are same, then same time, this A X and the X complement are available and we will get a current output F, so there will be no hazard in the circuit. Now, if the inverter, this inverter has the delay which is greater than this AND gate, then, first this AX will be available first. But this X complement is not, it is delayed, so it will, it is not or the reverse thing can happen, that AND gate has more delayed than the inverter, then what will be the timing chart or if we draw the timing diagram of this particular example.

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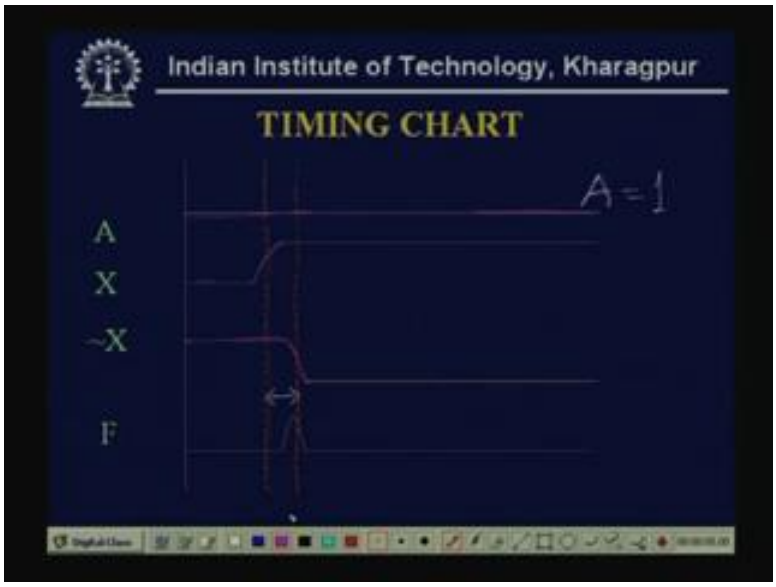

Then, see, first again I am taking that my A is high, this is my A equal to 1, now, say this X, initially the X is 0 and now, it is being 1, so it is switching X equal to 0 to 1. Now, what the X complement, the initially, the X complement will be, this is 0 to 1. So, this becomes X complement, it was high and ideal situation it should be, here it should be 0, but it should take some time for the inverter given. So, it will take this time, it will take, it will take this time.

So, this is the time, it will be taking for this transition or to make the X inverted or the output of the inverter to be steady. Then, in this case, in this particular example, the, at the output F, there will be a glitch, when for this transition or in this period. That means, if I consider that, this is my output F, then I will get a glitch at this position, so this is a static hazard, this a ((Refer Time: 22:58)).

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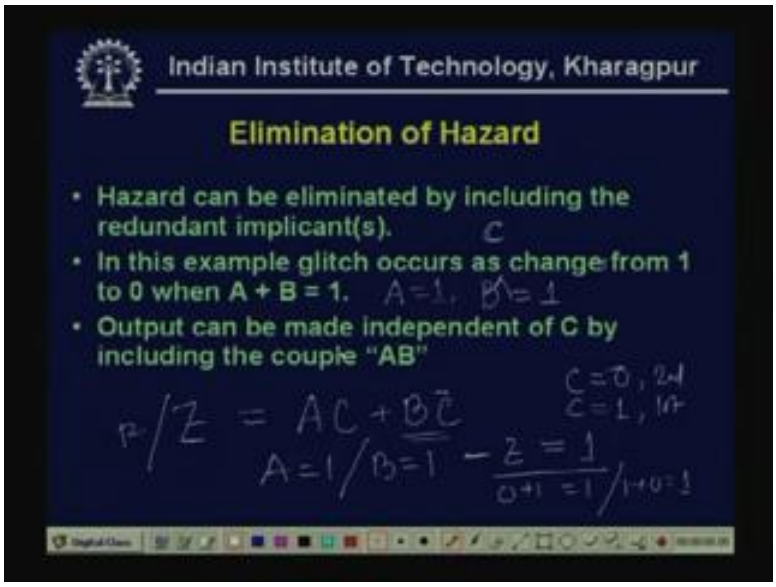

Now, what we are discussing, that how we can eliminate the hazards, the elimination of hazards by K map. See, the hazards can be eliminated by including the redundant implicants. So, in this particular example, glitch occurs as, the C changes from1 to 0. So, already we have seen that, if C changes from1 to 0 and when, A plus B equal to 1. So, or what we can tell that, A equal to, or instead we can tell that, A equal to1, B equal to1 and then, if C changes, there will be a glitch occurs or the hazard comes.

Now, see that, our example is that Z equal to A C plus B C bar, now this is nothing but a multiplexer type of example. That means, whenever A equal to 1 or B equal to 1, my output Z or F should be, Z should be, this should be 1. So, it should be independent of C or C bar, that means, if C equal to 0, see the type of function, if C equal to 0, then the second term is 1. If C equal to1, then the first term is 1 and as it is a odd function. So, 0 plus1 is1 or1 plus 0 is 1, that mean, if it is a, 0 plus1 is1 or1 plus 0 is 1.

So, whatever be the value, C takes 0 or 1, that Z should be 1, that means, it is independent of C. Now, this particular property, we can utilize to reduce the, or to make the circuit hazard free and how we can do that thing, we can include, an another input A B or this is actually a redundant implicants.

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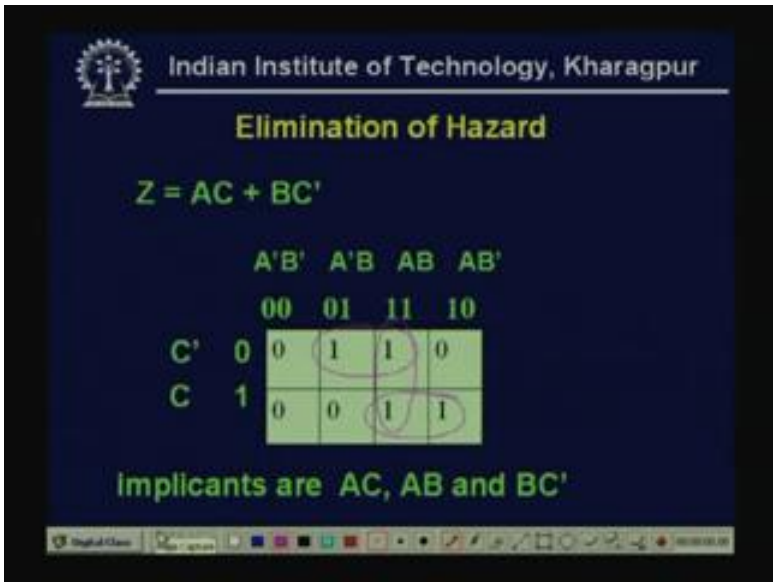

Now see, again we are, we consider the Karnaugh map, now, earlier we have seen, this is A C plus B C, so this is one couple, which represents the B C dash, this is one couple which represents the A C. Now, there is another redundant implicant, that is my A B and what earlier we discussed. Particularly by K map or that Quine-McCluskey, that this redundant implicant can be ignored, so that, it can be further reduced. So, now, what we are, again we consider, what we are doing, again we consider that, this implicant A B. So, now, the implicants are A C, A B and B C dash, so what will the circuit.

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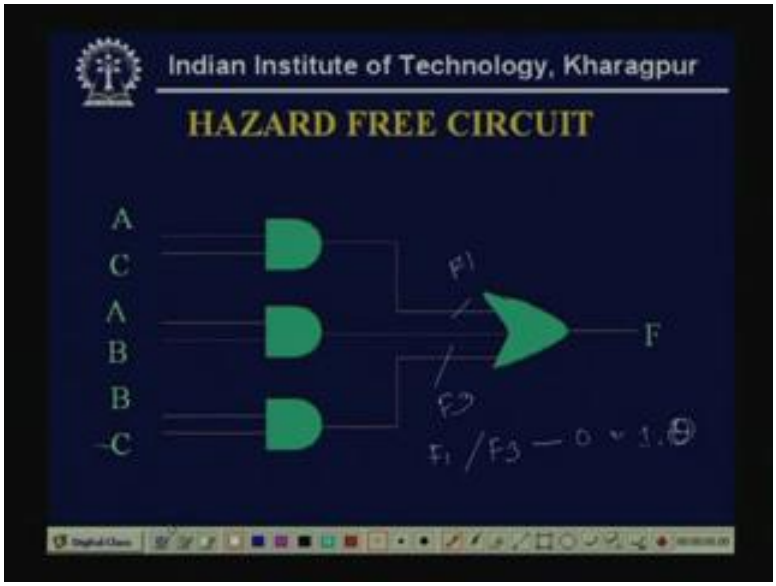

See that, this is A C, A B, B C dash, there are three minterms and this is a sum of product forms, so A C, A B, B C dash. So, whatever be the, value of C or C dash, see or even the

C switches from 0 to1 or 1 to 0, actually it is immaterial, because if the OR gate property is, or the truth table of OR gate is that, if any one the input of the OR gate is1, then it will, the output will be 1. So, that means, if A equal to1, B equal to 1, that means AB high, then1 input is high, so it is immaterial for the, the first input.

For this first input of the OR gate, or the, say, or the third input of the OR gate.((Refer Time: 27:56)) , this first input of the OR gate, say it is F1 or the F 3, whatever will be the situation. That means F1 or F 3 whether they are 0 or 1, that means, I am telling, this is A do not care theta, theta can be 0 or1 anything. So, it only depends on A B, so by including the implicant A B, I can easily reduce a hazards. So, by doing this thing, we can, this is normally called the static hazards.

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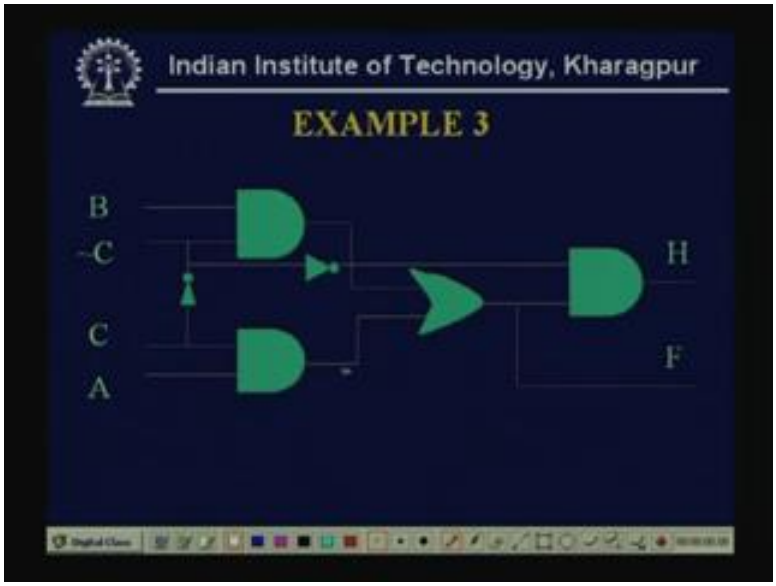

Now, we take another example, see here the, the previous example is already included here. So, this is B C bar, this is actually C compliment, so B C bar, the first AND gate is completing. The bottom AND gate is completely A C, that means B C bar plus A C and here, C is inverted, B inverted as C bar. So, these OR gate, so this is nothing but, our previous example that F, it is given the F. Now, I have included another sub component, say another inverter, this is one inverter, whose input is C bar. So, this is actually, input is C and another AND gate is included, so this is F C, so it is nothing but F C. Now, if we consider the timing diagram.

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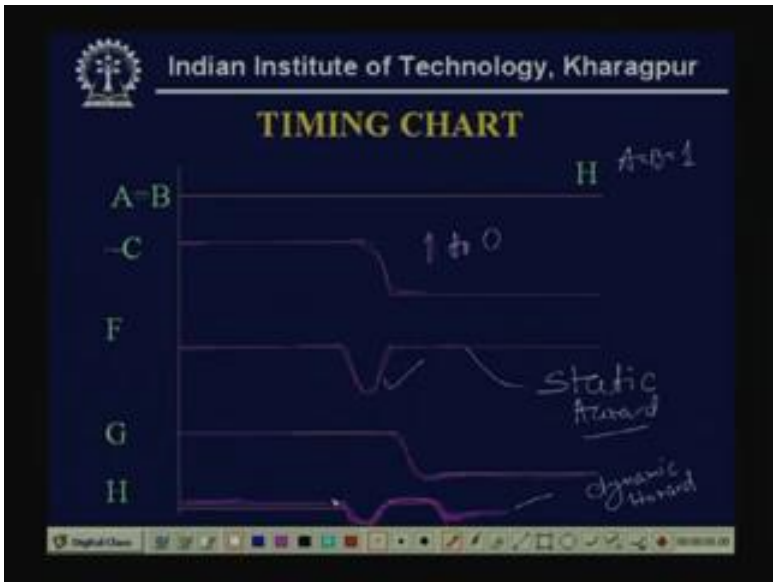

See, that, first again I am considering that A and B are high, that means, my A equal to, B equal to 1. Now, the compliment of C, so initially the C is1, now it is switching 1 to 0, this is1 to 0, now, what will be the F, already we have seen, that it is a static hazard. That means, I will get a glitch during this transition, so this is a glitch I will get. Now, what will be the G, see that G value is, that during this transition again it will be a some delay and H, again that, where the F was there, that time it is a, some glitch will be.

That means, for this particular circuit, with the static hazard also, some more hazards we are getting. See, here F we are calling, F we are calling, this is a static hazard. Now, with this hazard also, for this particular circuit, when we have incorporated or we have included another inverter and the AND gate, then we are getting some more added glitch. See, this 1 for the H, this is a some more1 for this, this is called the dynamic hazards. Now, what is the reason for dynamic hazards, unless in the circuit, that static hazard exist or if say, we would not get the glitch in this F line, then we will not get the, glitch in the H line. So, mainly, this is that, as the static hazards exists in the circuit and that is why, that some dynamic hazards. That means, some more added hazards with the static hazards, we are getting and this we are defining at the dynamic hazards.

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So, dynamic hazards can only exist as a result of static hazards and we need not be concerned with dynamic hazard, if static hazards are eliminated. So, that means, in the previous cases ((Refer Time: 33:01)) that if, if this glitch are not there, then, there will be no glitch in the H also, so in the H also, there will be no glitch. Now, if we summarize that, the hazards covers by K map, then what we get that, the minimum circuits may not be hazard free.

As the example we have taken, under minimization have to be sacrificed, if we want hazard-free circuits. That means, in real life, if we want a reliable circuits, that means, which is not giving any hazards or it is not producing any glitch at it is output. Then, sometimes we introduced, intentionally we introduced, some redundant implicant to reduce or to overcome the hazards or to get a more reliable circuit and by using this Karnaugh map, we can easily include this redundant implicant.

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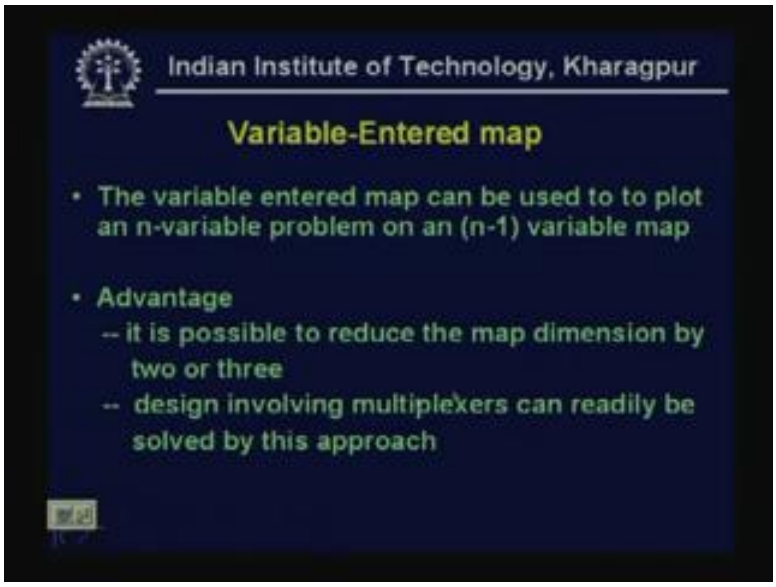

Now, today we read another thing, that is called the variable entered map, so far, we have discuss that normal K map, then the, how we can reduce that extra implicant or the Quine-McCluskey. Now, today we read that, one is variable-entered map, see, why another variable VE map is, or variable entered map or normally it is called VE map. Why VE map is needed. Normally, that Karnaugh map we have read, that is very good for a very suitable, well suitable for the, for six variable function.

If it is more than six variable, then to draw that thing is a cumbersome one, so we need to automate the program. Now for larger, for n variables, say when n is a very big number, for larger numbers, this is not a good choice to reduce the function by a K map. Then, the variable entered map can be used to plot an n-variable problem on an n minus1 variable map. So, if we write program, then always, for a large value of n, we can reduce the K map for it is lowest values or that, some reduced variable map and this is a very big advantage.

So, it is possible to reduce the map dimension by two or three, so that means, if n is 8, then I can reduced by is, reduce it by 8 to 7, then from 7 to 6, 6 to 5 like that. So, it will be very good for writing a program and for large variables and the design involving multiplexers, can readily be solved by this approach. So, this is another big advantage, that means, if my design problem involves a multiplexers means, just now the examples we have discussed that type of A C bar A C, plus B C bar.

That type of equation or function, then it will be very good to select or to choose the variable entered map. So, with now we see, that what we mean by or how it differs from the normal K map.

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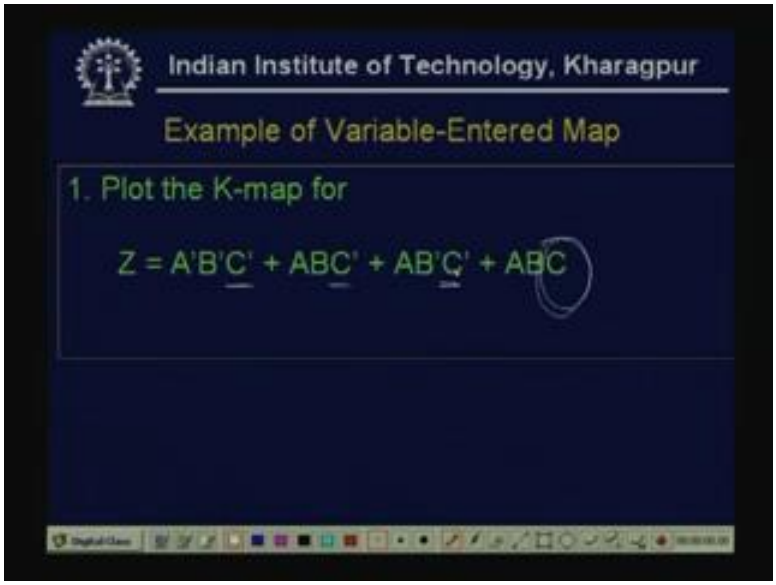

We take one example, so plot the K map for Z equal to A dash B dash C dash, plus A B C dash, plus A B dash C dash plus A B C.

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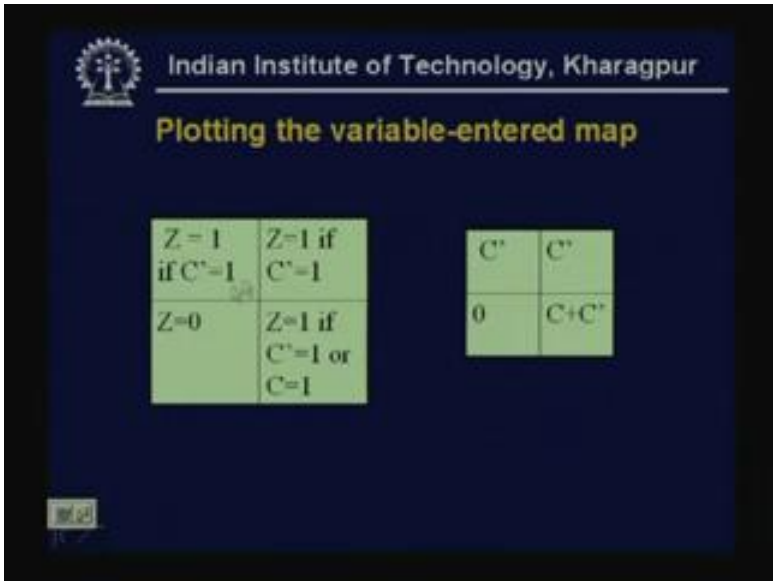

Now, see that, again if we or see here, if we draw the normal Karnaugh map, see first thing is, that, see this is that variable the or the Karnaugh map for that ABC. So, ((Refer Time: 38:07)) see this is a three variable function, where ABCs are there and for the first

three terms, see for the first three terms, that C dash is there means, these are complemented form and only in the fourth term, this is a uncomplemented variable for C.

Now see if we, now if we draw. See, this is for my A B, now see, Z equal to 1, so this will be my A dash and A, this is my B dash and B, so this is my A dash B dash. Now see, this, if C dash equal to1, that mean if C dash exist in the term, then this will be Z equal to 1.

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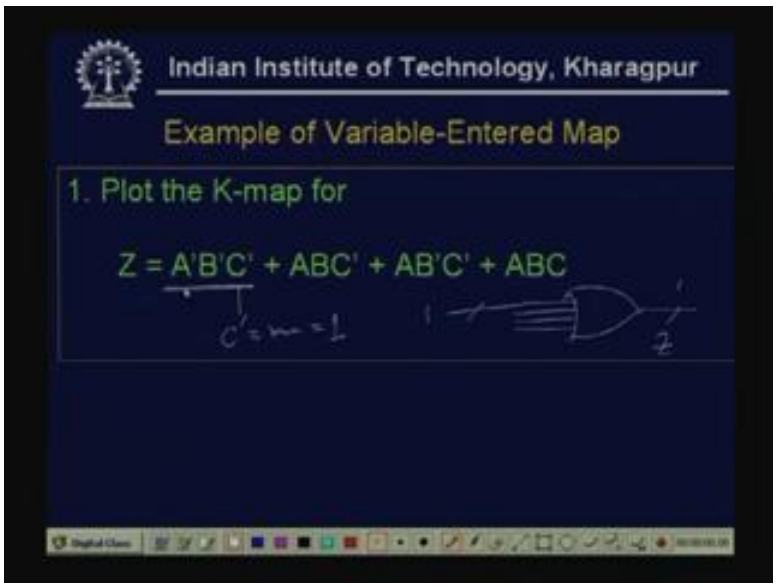

See, the previous example A dash B dash C dash exist, see here A dash B dash C dash is one of the minterm. So, that means, if A dash B dash is true and C dash is also true, means C dash equal to 1. Then the output will be 1, because this is a sum of minterms, that means, again if we realize, this is nothing but a four input OR gate and if anyone of the OR gate is 1, anyone of the input of the OR gate is1, then it will be, output will be 1, so this Z will be 1.

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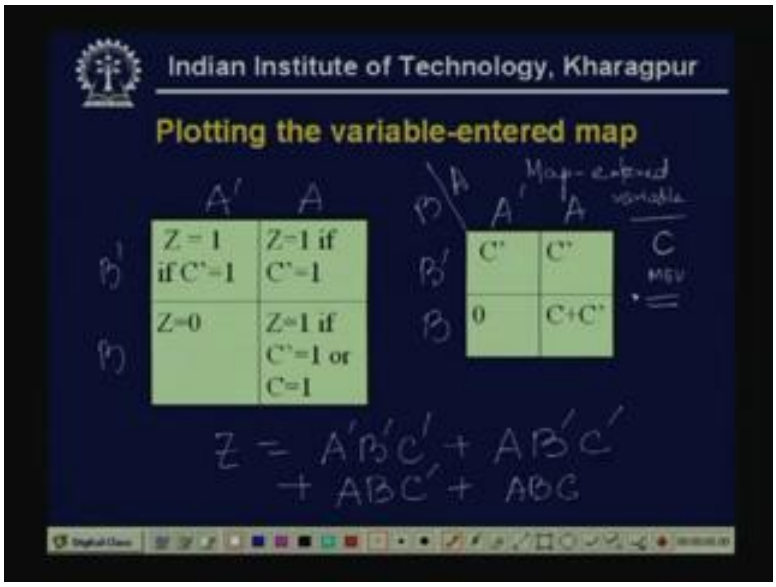

So, in this way, what we have, we can tell that this is actually my A dash B dash C dash, so if I, see this is a three variable function, but I am drawing it for, as if two variable A B and I am taking C as my variable or map, I am telling this is map entered variable, M E V. So, this is the position that, A or this element that Z equal to1 or output will be1, if A dash B dash C dash, that is the first term, now, this is my A term, so this is my A B dash, now, Z equal to1 if C dash equal to1.

That means, some A, B dash, C dash, that minterm is there, we check, whether it is there or not, ((Refer Time: 41:57)) see A B dash, A B dash C dash, A B dash C dash, so that minterm is there. So, this is, Z equal to1 if A B dash C dash, that term is there, similarly, there must be one term, that will Z equal to 0 , that means, this is A dash B, there will be no term and Z equal to1, if C dash equal to1 or C equal 1. So, that means, this is the minterm for this element is the A B.

That means, A B C dash and A B C, both exist in the expression, so from here, what we can tell, that my expression must be some Z is, for the first element, this is A dash B dash C dash, because my C dash is map variable or map entered variable. Then, for the second one, this is A B dash C dash plus see, for the third element it is, it does not exist because output will be 0. That means, the minterm does not exist and then for the fifth one.

Actually this is, the term is from the K map this is A B, A B term and as both C dash and again C, both exit, so that means, AB C dash plus ABC, so this will be the thing. Now, we can reduce this thing by this, say this is a map and A dash A, B dash B. Now, I can reduce as if, this is, the first one is C dash means, the output will be1, if this is A dash B dash C. Again there, this is, the output will be1, if the C dash is true and here output will be1, if C or C dash is true, that is why C plus C dash,1 is plus, so C plus C dash.

So, as if, the, in the normal K map, this were actually either 0 or 1, if the minterm exist, then that particular element, we put as a1, otherwise it is 0. Now, that 1 is replaced by either the third variable, which I have not considered in my map, say the, actually there are three variables A B C. I have consider only A and B are the map variables and C, as if the C or C compliment or some combination of C. That means, C or C dash, just now I we have seen, because both the term exist A B C dash or A B C.

That means, it will be true, the output will be true, if A B C exist or even A B C dash exist, so that C plus C dash. So, the 1 will be replaced by the third variable, in this particular example or the complimented variable or the, or of the variable and it is complemented 1. So, this third variable, which we have not considered in the variable of the K map and the1 is replaced by this variable, this is called the map entered variable or MEV, so this is called the map entered variable or C, in this particular example. This is map entered variable, in this particular example, it is C and it is called the MEV.

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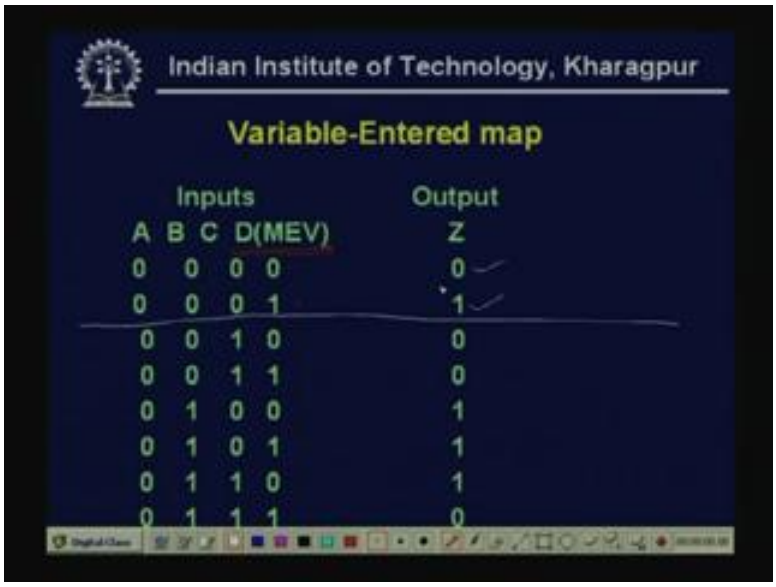

Now, we take one four variable example, say A, B, C, D are the four inputs and output is Z, we take, first we consider the truth table of this four variable function. So, truth table means, that all possible combinations, all 0 0 0, 0 0 0 1 to all 111, I have to take the, what will be the output. That means that, all possible input output combinations, I have get, that is the truth table, the tabular representation. Now see, this is the, for this particular function, that if, say I have kept A B C are the K maps.

And that means, I have taken my D as the map entered variable, so this my D, it is the map entered variable. Now, when A B C is, actually we should draw a line here, say A B Cs are 0 0 0, then D can be 0 or1, Z is, if D is 0, Z is 0, if D is 1, Z is 1 then, how I can represent this.

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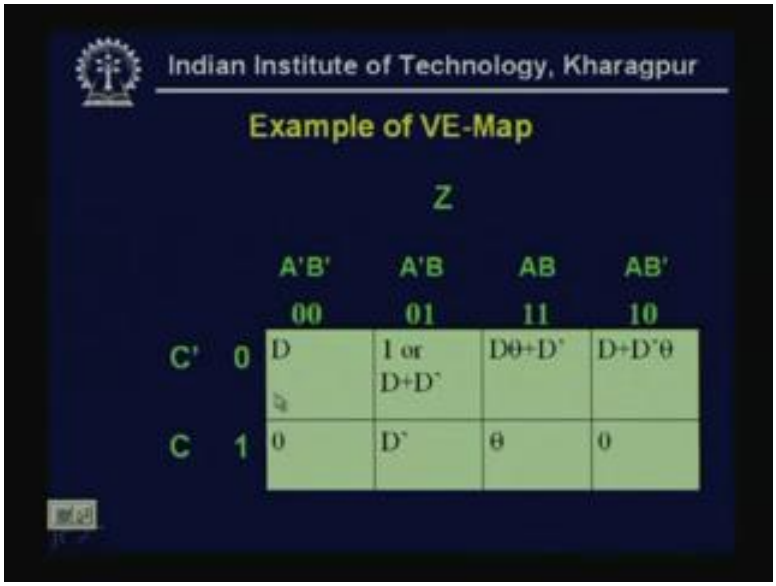

See, A B C 0 0 0 means, A dash B dash C dash, this is my term 0 0 0 and, see if D is 0, output is 0, Z is 0, if D is1, Z is 1. That means, my output is nothing but the D, so for this, that A dash B dash C dash, this is D.

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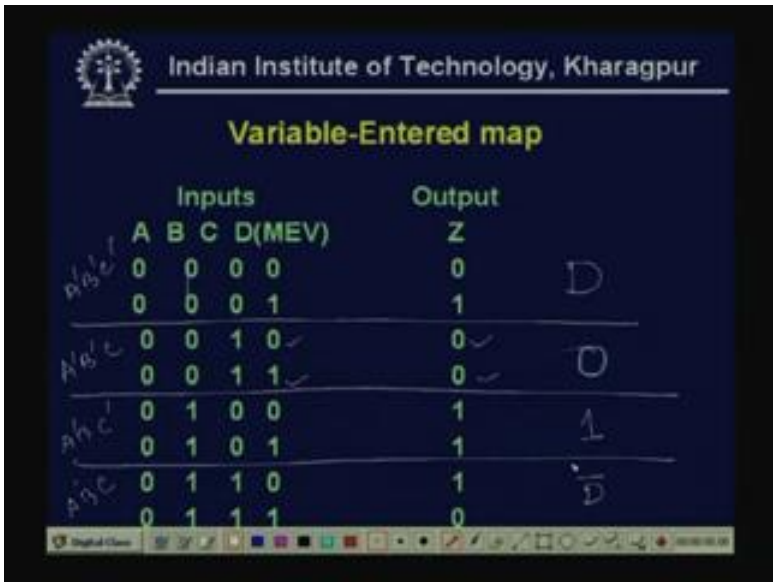

Now, so actually, this is my four variable function, if we draw the normal Karnaugh map, it should be a that 16, that means 4 by 4 table, 4 by 4 map. Instead of that, we have reduced it into three variable, I have taken A B C as the variable, normal variables and D as the map entered variable. So, now for that, so this is for the first one, so this output is Z is nothing but D Z. Now for the second pair, see for 0 0 1, means A B, A bar B bar C, then this is, if D is 0, Z is 0, D is1, output is 1, Z is 0.

That means, it does not depend on the D or it is independent of D, that means my output is 0. Similarly, here my output is1 for this combination, so this is the combination, that A bar, B, C bar. Earlier previous one it was A bar B bar C, this is A bar B bar C bar, this is A bar B C and this is 0110 means, it is actually complemented of D.

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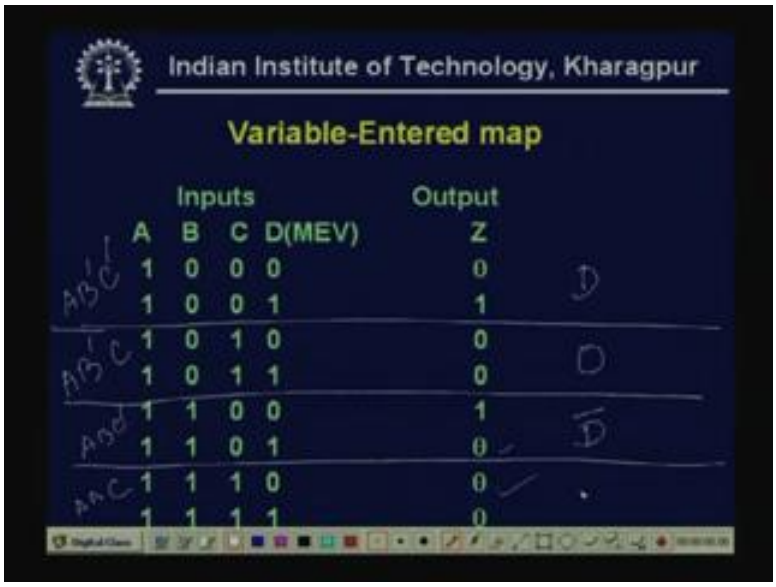

Now, again for the next, next pair if we draw, see for the next pair, actually this is for the term A B dash, because this is1 A, B is 0 means B dash and C is 0 means C dash, see D is 0 1, Z is also 0 1, that means, my output is D. Then, for this term, it is A B dash C and my output is 0, similarly this is for A B C dash, this is 0 1, D is 01. Then output Z is1 0, so this is compliment and for A BC, this is 0 1 and this is C. Here, I have written theta, means this is actually do not care, it does not.

Here, also actually I have taken theta, theta means it, this term will not appear, so whatever be the case, it will not be the ((Refer Time: 52:38)) D. Now, if we summarize or if we put this truth table, from this truth table what we have studied. That means for each pair or for each minterm consisting of A B Cs, how the output Z depends on D. That means, what we can tell that, variable entered map is for some for the combination, for each combination of it is reduced variables. How the output depends on it is map variable or map entered variable, hat we are summarizing or we are putting in the map.

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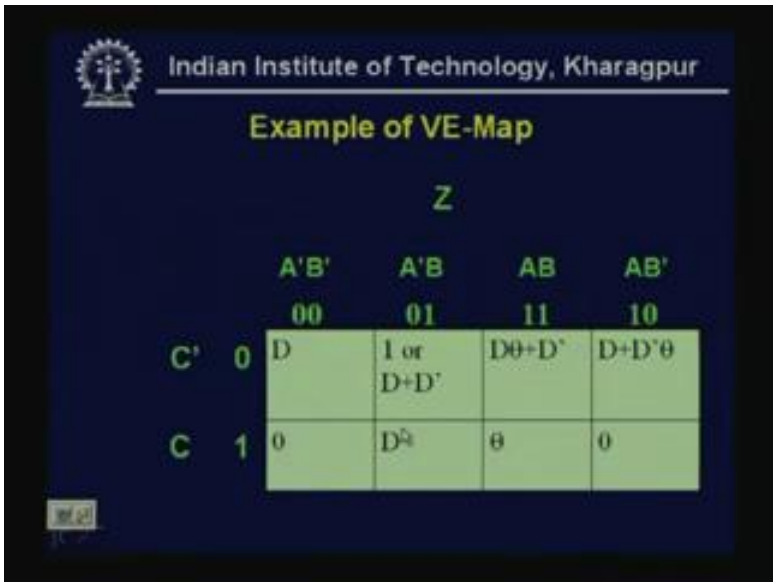

So, just now what we have discussed, this is the summary, see for that A dash B dash C dash, already we have seen, this is D, for the next, this is A dash B C dash, A dash B C dash it is1 or D plus D dash. Similarly, for A B C dash, this is that last cases, that A B C dash, that it depends on D theta plus D dash, theta is the do not care. Similarly, here A B dash C dash, it is D plus D dash theta and we have seen that A dash B dash C, for this minterm actually whatever be the D value, the output will be 0.

Similarly, for A B dash C, the output will be 0, for A dash B C, the output will be D dash and for A B C it does not, it do not care whatever be the combination of A B C. So, that is why we have kept theta, so this is the summary. That means for the 4 by 4 map, see it reduced to 2 by 4, that means from four variable to three variable and as if this 1 0 are reduced by some combination of the other variable. That is which is left, which we have not consider in the Karnaugh map, so this is the concept of the map entered variable.

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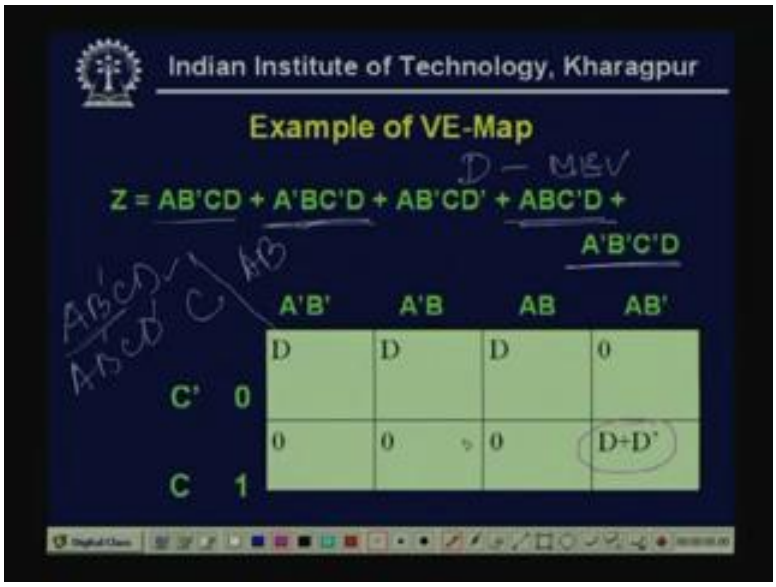

So, this is another example and of the four variable and see here, simply that say D we have consider as the map entered variable. So, D is M E V, then again that, if we take A B and C, then see for A dash B dash C dash, it is D, see for this term A dash B dash C dash, it is D. Similarly, if I take, say A dash B C dash, so it is D, this is A B C dash D, so A B C dash, A B C dash D. So, A B C dash, if D is true, that means for this, it is D is true, if D is true.

Now, see A B dash C dash the first term, the A B dash C D and A dash C D dash, so these two term exist A B, if, for a A B dash C term, it is true whether it is D or D plus D compliment. So, that means for A B dash C, the term will be D plus D dash, say this will be D plus D dash, so in this way we can summarize our, this VE map.

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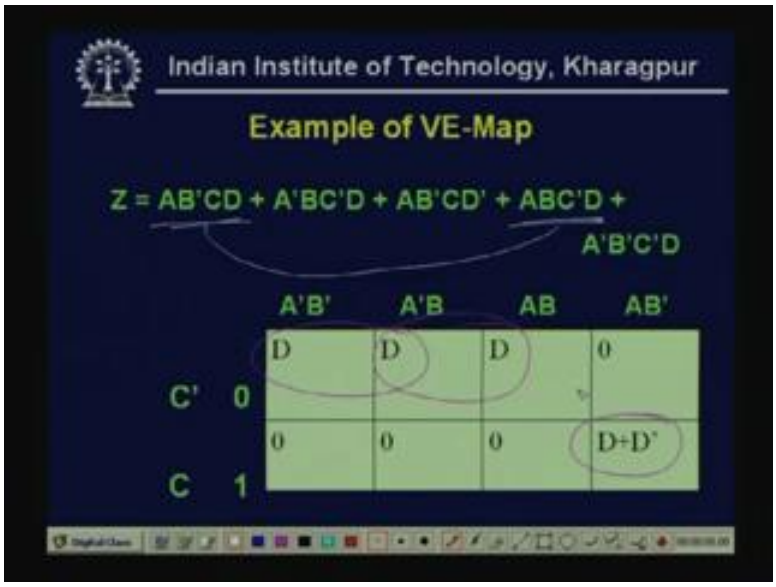

So, now what we can do that, now we can reduce in the same fashion, now we can take the couple, we can identify some couple. See here, I can, this one be a couple, this can be a couple and this is, this itself is a couple because D plus D dash is there. See for the first one and the fourth one, this two, this two, so we can easily reduce this expression by again considering the couple. So, what we have seen by introducing or by selection the VE map method, that we can easily reduce the n variable to n minus 1 variable. And recursively we can do that, n minus1 to n minus 2 and so, it will be very easy for reducing some expression and some higher variables a large number of variables are there.

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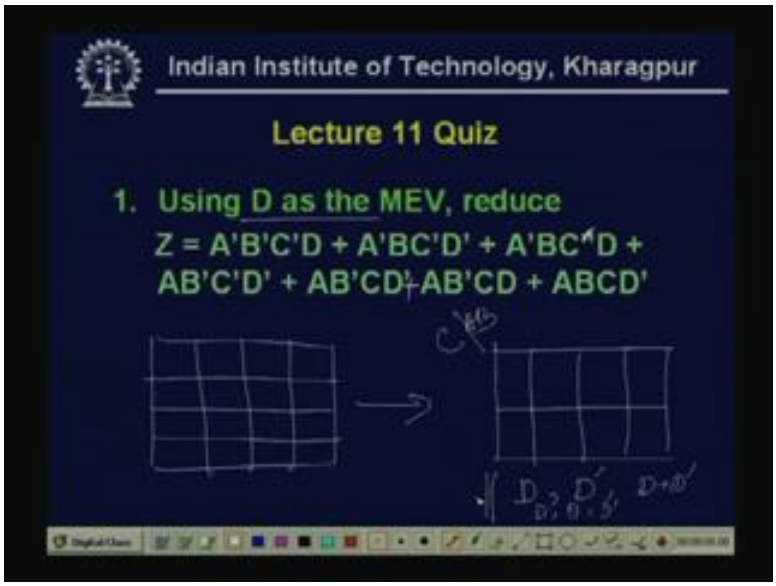

So we will, now today's quiz problem, that using D as the M E V, reduce Z equal to A dash B dash C dash D, plus A dash B C dash D dash, plus A dash B C dash D, plus A B dash C dash D, A B dash C D dash, plus A B dash C D. So, actually this is a four variable function and as this is a four variable, so normal K map should be, this type of 4 by 4, now it will be reduced to the 2 by 4 and the way and this as, D as the MEV. So, here it will be the, content will be, it will be A B C.

And the content will be some D, D complement or some D plus D dash or the combinations of D theta, D theta D dash. So, this is the today's quiz problem that we have to reduce using the MEV method.

Thank you.