Indian Institute of Technology Kanpur

National Programme on Technology Enhanced Learning (NPTEL)

Course Title
Digital Switching

Lecture – 33

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Okay so let us continue from where we left in the previous video so in the previous video you are actually analyzing you are actually go through step by step process for the analyze of buffer delta network so I also discussed about the patter net model I think in the previous video and then of course we also talked about t select is = 0 or t pass = 0 so one of the two things and then how we are going to do the modeling with that I had also explain that what is a consequence of when t passes 0 or when t select is 0.

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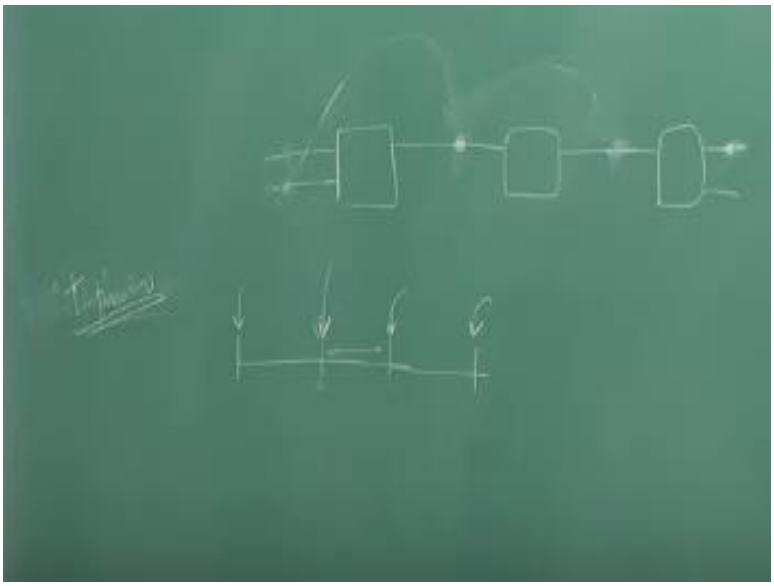

So if we look at a cascade of the switch I am just repeating that if we look at the cascade of a switch they are two packets at the input this ahs to be go this ahs to go to another switch and so on I am only taking three stage system so when t passes 0 that actually means that packet transferred as is happens almost instantaneously while selecting a packet takes one full slot okay so what will happen is this situation of what will happen to the buffers is being propagated almost instantaneously that is what I am assuming and then the selection can be done at all the stages simultaneously.

And then packets can be transferred almost in 0 time so in the first time slot these two packets which are containing so what is the time slot is going to be over that time we know which packet has to be transferred and it will be transferred almost instantaneously so at the beginning of the slot next slot you will have a situation that this packet is already moved here because this has one the contention now again the in the full slot in this particular duration they will be now doing the decision process and the selection will be happening and at the end of this almost instantaneously this packet will move here and this packet can also be moved here okay so you will have situation we had this packet.

We will have a situation when the packet here will move here and there is another packet on this side and at then again in the next slot the selection process will happen and then almost since instantaneously the packets will be transferred so one will go on the outgoing port and then this will be immediately remove okay that is what will happen with t passes is = 0 instead of the t select is = 0 we are going to take so in that case when initial the two packets will be there and it would not take much time to select which one of them has to go to that but only one packet can be going.

And it will take one full slot period okay so instantaneously decision is made which one will go out by that time you reach here this packet would have been completely transferred at this position okay now at this position unless this slot is empty you cannot write this packet here because in the earlier case when t pass was o this packet was instantaneously empty in next packet could have been pushed in so all packets actually do the jump and there is a cascade effect

which cannot happen here in this case so it will take one full slot for the packet to transmit here by the end of this, this is a situation.

In the time slot again decisions will be made but this slot is not free this will take one full slot to get empty and this packet will reach here at the end of the slot but this has to be hold up because you do not have the buffer empty here okay this buffer get empty only at this position so now in the at this position again these packets will move and I will have a situation where the packet one packet is here and it will take one full slot to read out on to the outgoing line so that is a difference between t pass is = 0 and t select = 0 now of course everything is going to happen in now three steps when t pass is 0.

So let me see what are the those steps so we will be first fall analyzing t pass = 0 case so this is then case which were analyzing.

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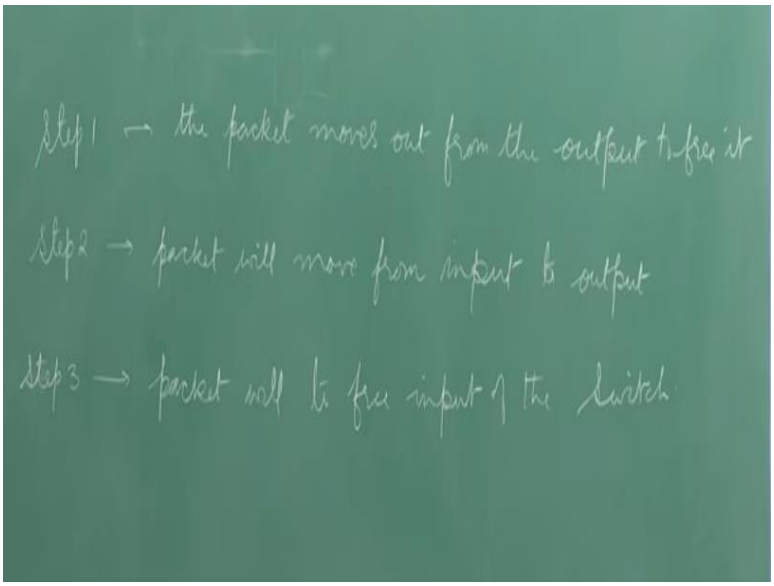

So a step one will be when the packet moves out from the output to free okay so if I am talking about switch it might be having a packet on the outgoing buffer so this has to go out first so within one slot I am actually defining these three stages steps which are happening and this is

basically kind of an assumption which have made this will simplify my computational process after step one this step two will be happening step two will be happening where the packet will move from input to output.

And then there will be a step three were packet will move from the previous switch to the input actually so packet will move to free input of the switch so these three things these are the factious steps which we are going to have and at a stage n – 2 in fact if you look at the last stage, last will be n- 1 so stage n- 1 will be connected to that now remember the case which we are constraining the t passes 0 okay.

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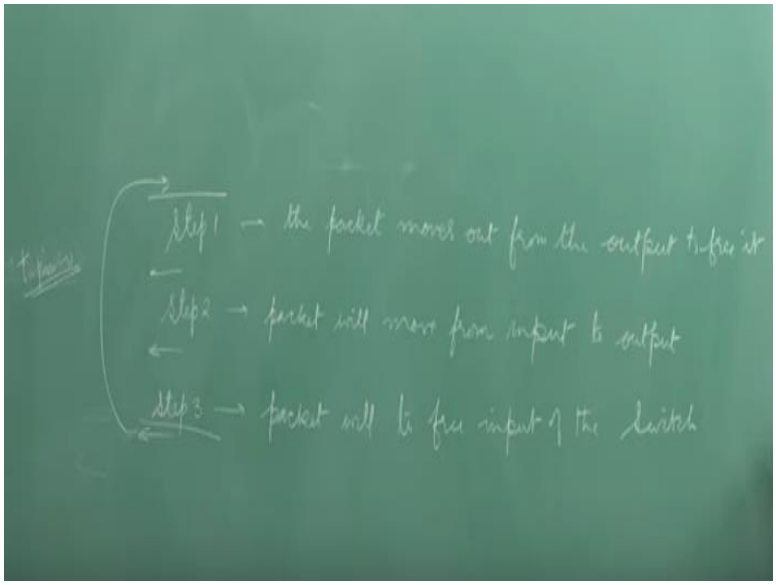

So when t passes 0 so the packet will instantaneously removed out so which actually implies that any packet which is here will always be removed because there will not be any packet here this will be always become free these outputs so any packet at this point will always removed out so they will always be empty actually and state probabilities so every switch now every switch I will identify as what are the possible states in this case and this state probability is these states can transit can do a transition from one stage to another state so we will find out the state probabilities after step one okay we will find out the state probability after step two.

A state probability after a step three this will become the probability which will be used here in the next time slot so this one full time slot actually so is the state probability after step three will become the initial state probability before step one in the next time slot so we can now formally define what will be these state probabilities so let me define these and then we will actually consider the transition probabilities we will estimate so p(0) this is basically in the current time step what is a probability of being in a state here this basically after step three of the previous time step okay so p is o.

1j, j actually implies here so this is n times step talk okay so this case signifies this particular time step and I define this as I, I means it is a state I j means the stage j the switches in stage j all switch in a stage j will actually will have the same probability distribution so this we have already done has one of the Lema's and 0 means the step 0 which is basically after the step three of the previous time is step okay this will be written as probability that switch in a stage j is in state i at time is = tk so remember τk this step so when I draw a time line the tk is just time and this particular time interval is talkie okay.

So tk is that particular time instant, so we will also define once the first step has taken place then the state probability will be different so this is the probability that after a step 1 you are in a step I in stage J in this time internal Tk so this will written as probability that switch in stage J is ins state I after a time step after step 1 in interval τk, okay. So similarly we can go for the next one this is after step two so I can write this as probability of switch in stage J is in state I after a step two in interval τk, so we can define further P3 so let me write down the P3 on this side.

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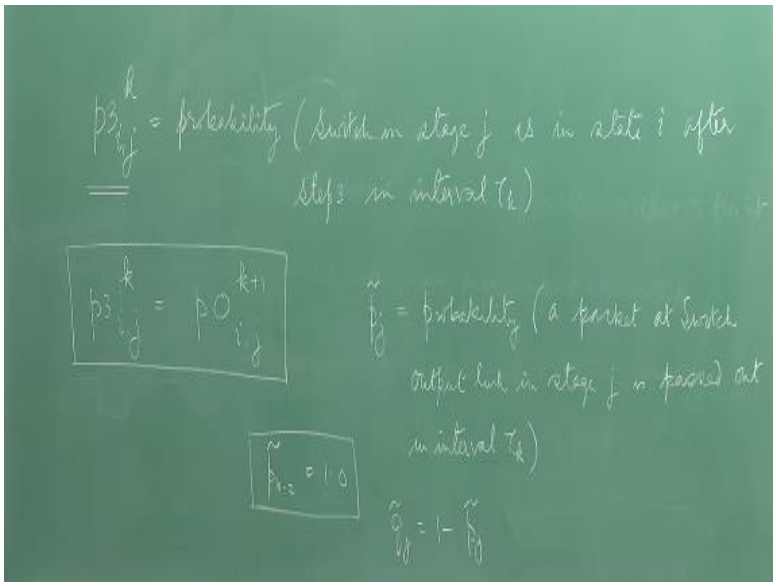

So this will be probability of switch in a stage J is in state I after step 3 in interval τk now interestingly this P3 ij should be equal to P0ij in k+1 so this is important this is what I have empathized earlier we also now define certain other probabilities so we can define PJ ~ so this will be probability get a packet at switch output link in a stage A is passed out basically moved to the next stage buffer in interval τk.

So we can actually now we need to figure out what are the states before we actually start estimating this PJ ~ and there is another probability will define PJ bar and based on that we will make the comp0letre estimate so ultimately what we want is we want to find out what is going to be the throughput which will be the P and -1~ the probability that packet will be going out of a tis of course is a conditional probability.

So we have to find out what is going to be the throughput using this particular procedure, so in fact if you look at as I define that in the n- second stage if there is a packet till certainly go out this is a conditional probability if a packet is present it will be going out condition on that, so boundary condition for this one will be the TN-2 ~ will be 1.0, okay. And then of course you also define if there is a PJ that packet may go out that is also probability packet will not go out.

This has to be complementary of this so I will define QJ ~ = 1- PJ ~ so this is a boundary condition which we can actually use, so we need to look into now the states so let me list down all the states which are there so I can write down the state, so we essentially derive all possible states which can exists in a 2/2 switch, so switch is like this it is two outgoing ports and two incoming ports and packets can be stored at input as well as output buffers, okay. So basically the output buffers are nothing they are the input buffers of the next stage switches.

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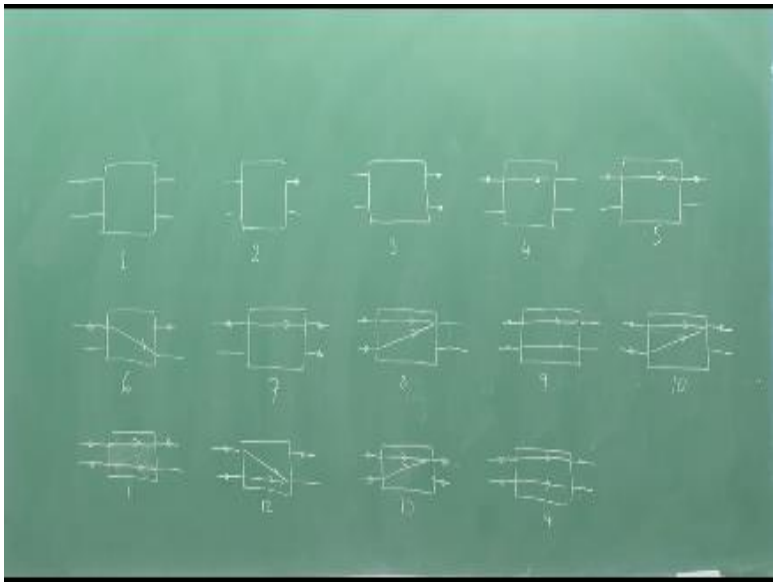

So first possible state is when there is no packet being buffered I call this state as 1, okay. So next possibility I will now look into 1 packet being put on the outgoing side so if this is buffer there is no packet on the input side this we call the state two of a switch, third possibility is that we will have two packets on the outgoing side so this is the third state there is no packet at the input.

Now I have exhausted all the possibilities for the no inputs at the input buffers I am only considering the output side now let us consider one packet at the input buffer so if I have one packet at the input buffer there is no packet at the output buffer is one possibilities I have to also

give a direction so this packet can go here this is actually state is equivalent to this state these two are same state actually.

So I can always swap these two outputs okay I can always twits them around and this will turn n out to be the same thing, so there will be only this state which is possible, so I define this as state 4 then it is possible to have it still one input and I can have one output so the packet can be directed to this particular thing so or there is a possibility that packet can be directed to free out going port.

Now all other combinations for example I can always say a switch might have a situation like this there is a packet here and this is going here now these two are actually same conditions, so this essentially merges into this particular state, okay. So there is a possibility of similarly for example having a switch here and doing it this is also the same, okay. This is the other one so we can have similarly all possible combinations you take.

So this is nothing but the same condition which is there on the other side the 6^{th} one so this is the 5^{th} stage 5ths state and this I define as a 6^{th} one, so if I can by twisting the inputs around there if I can map onto something then that is being merge in that state, so this is the 5^{th} one then I can define 4 this is the 5^{th} and this is the 6^{th} state I can now define the state with one single input.

And two outputs so this is going to be directed here so if it is not directed here this is actually means the same thing, okay. So there is only one possibility here we define this as state 7, now I can I have to start with two input thing occupied when there is no output and two inputs they are two possibilities okay both of them are being directed to the same output so if both of them are directed here or here which is the same thing it will essentially degenerates into the same state so I call this a state 8 and then we will have two free things and they are being parallely going out this is state 9, okay. Then of course I can have situation when there is one input two inputs and one output, so both of them can be directed to the port way already the packet is there I call this is state 10.

It is possible that both of them get directed to the bottom side, so in this case so one of them going to this occupied one other one into this, in fact this is state same as if I draw it the other way around also the same actually, so both of them are same so I am going to just use this, this we call state number 11, and then of course when both the inputs are being directed or are being containing for the free output port this is the state number 12, okay.

Now I have actually exhorted all once two inputs and one output, now I have to put with two outputs and two inputs and there only two possibilities so one is these two are trying to go to the same outgoing port, this is the state number 13, and then we have this as the state number 14, so even whether even this being cross the top one top input is trying to go to the bottom output bottom one trying to go to top one is same as the state which is already shown. There are only 14 possible states which are distinct all other possible state which can be there for a 2/2 switch can actually will be represented by these itself equivalently so these are a non-equivalent states which are possible, so we can now write down in terms of these by $Pj^{\sim}$, okay. so let me explain how we get that.

$P_j^{\sim}$ will be essentially this is the packet, this is the conditional probability that a packet is there in the outgoing port and in the next time step after step 1 or this packet is being moved out that will be happening after step 1, because in j^{th} stage the packet actually goes out of the outgoing port only after step 1, okay. So this $Pj^{\sim}$ will lead to transition after a step 1 the states will change for the j^{th} stage switches, okay so this will be essentially responsible for that, so I need to find out the probability first of all because the conditional probability, probability that a packet is there in the output buffer, okay.

And then of course we will have so this should be after step that a packet is there in the output buffer of switch in stage a this equivalently implies the input buffer or switch when stage a+1, okay so these two are equivalent actually. And this is the probability that in step 1, sorry I will rewrite it in slightly different way, okay so that it can be clearly communicated.

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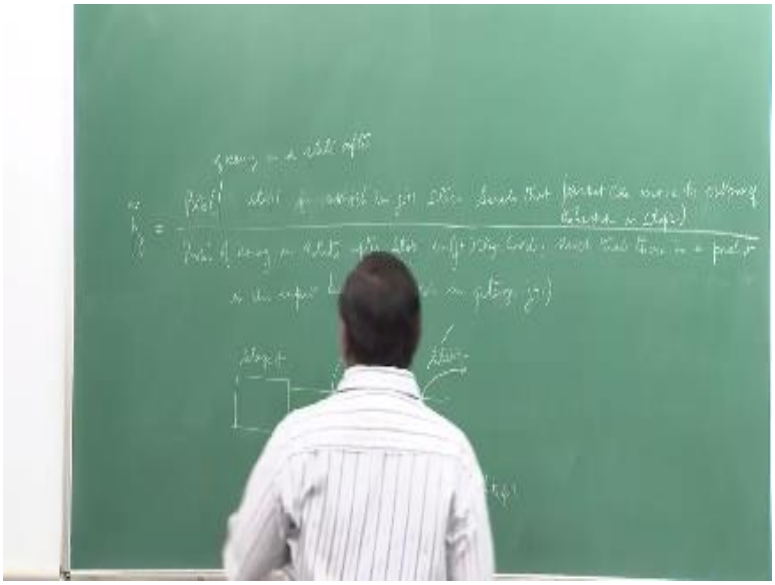

So what is happening is in stage j this connected to stage j+1, okay so j+1 already the packet has moved out that is the step 1 which is happen, so now the what is happening is after the step 1 when step1 is already over so step 2 is this packet will be transitioning from input to output actually, so I am trying to estimate what are the states after step 1 where there is a packet which is present here, okay so that I will be using numerator that is the probability that the packet will be present there and then I will find out that after step 1 what is the probability that switches in that in the state in such states where a packet actually can transition.

In the step 2 of this one which corresponds to the step 1 for stage j, so remember when the step 2 is happening here, step 1 will be happening here, okay and then of course step 3 will be happening in the next one because the packet will be arising there in their input buffer. So I need to find out in j+1 first stage what are the step probabilities where you will actually have a packet at the input of j+ first stage switch which also implies the output buffer of the stage j switch.

So I should write it as probability of being in state after step 1 in j+ first stage switch, such that there is a packet in the input buffer of switch in stage j+1, okay and of course this probability will be of being in a state after step 1 in switch in j+ first stage such that packet can move to output of the switch in step 2, okay. So let us look into we actually have to maintain these states

and based on that we will decide we will actually write down the expression for this. So this expression I have to write down all the numerator and denominator terms, so for Pj˜.

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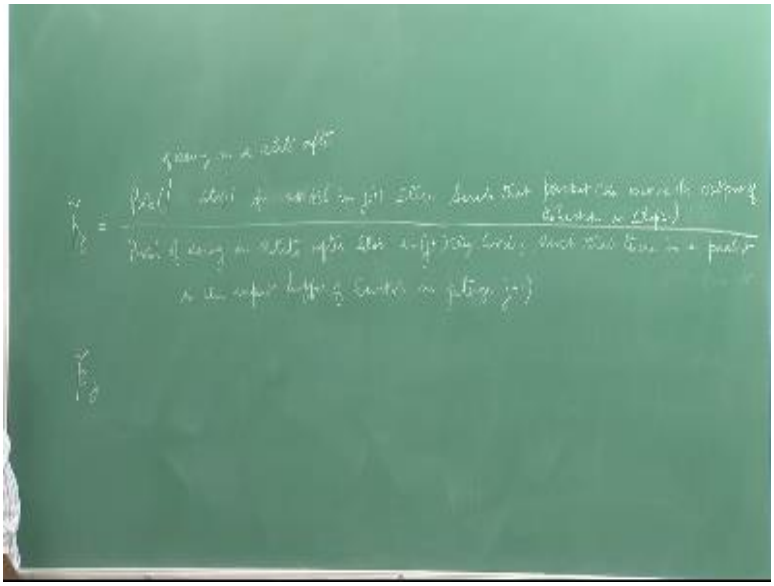

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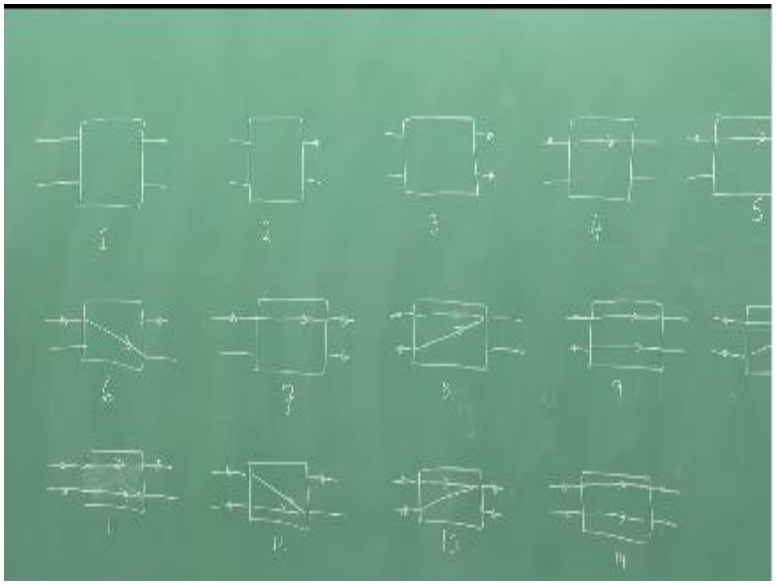

I will have to find out the states.

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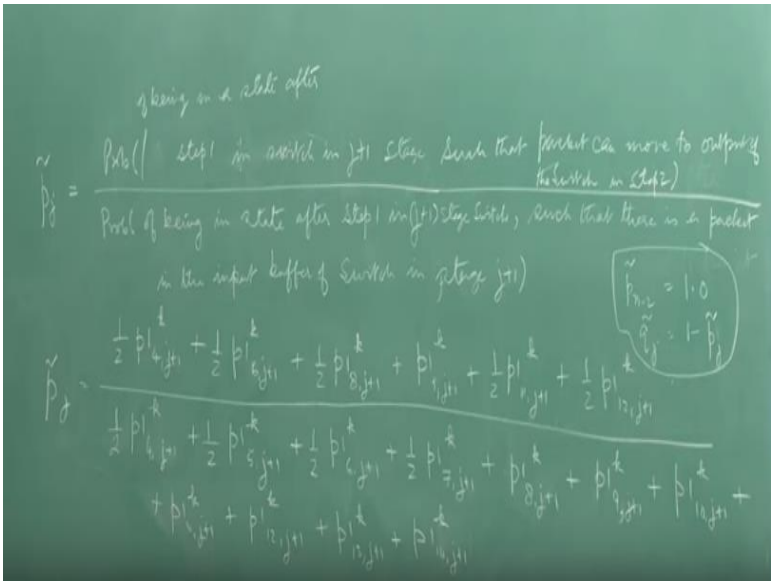

Now remember I am talking about the j+ first stage switch and step 1 is already over, okay.

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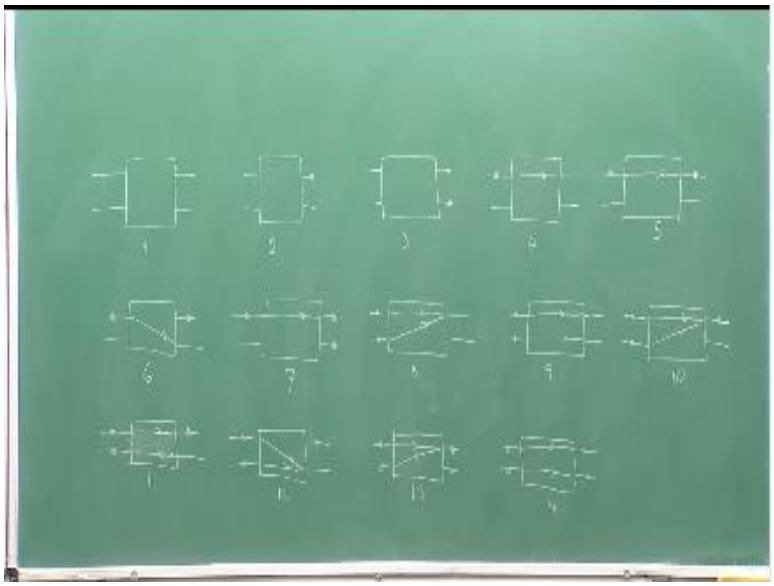

So do I have a packet at the input after step 1 in j+ first, so you cannot being this state there is no packet at the input, there is no packet at the input, there is no packet in the input. If by chance the switch is in the fourth state in j+ first stage switch then there is a packet but with half probability the output which you are considering can be this one and reminder at the remaining half it can be here, so I need to write down that it will be.

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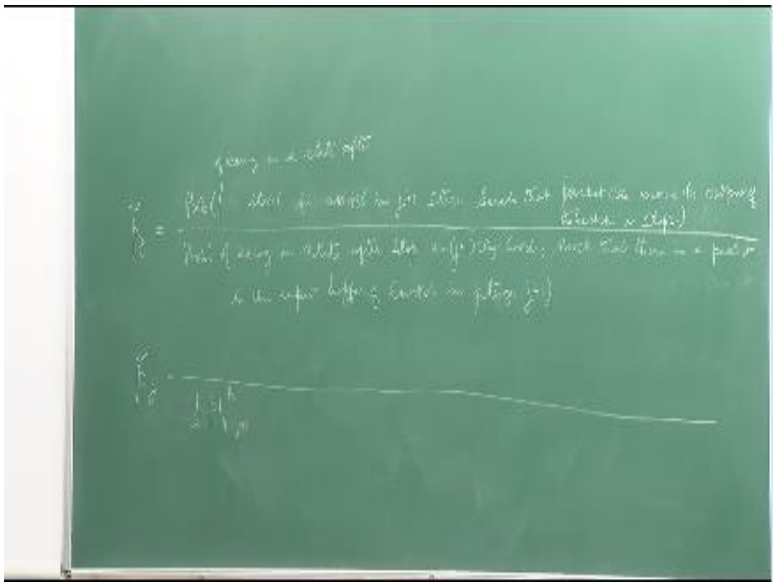

1/2 p1 this after step, you are going to be in state 4 stage j+1 in time step k okay so with that probability you will have a packet at your at the output buffer of the switch in j^{th} stage okay now let us look at the next one this one also contains only one packet so with half probability this also I need to put in so I will put ½ p of 1 5j+1k we can keep on looking so similarly I need to do it for 6 so wherever there is only one input port having the packet I will do that p1 6 j+1k 7 also in the same fashion.

8 actually both the inputs have the packets so with equal probability you can have this or this connected to you so which actually means this time there is no ½ I have to have 1 so I will be putting p1 8 j+1k so p9 similarly p1 9 j+1k p10you can be in p11 p12 and p13 and p 14 so all of them will come okay so this is what will be the denominator this is this probability. Now I have to look at the cases were packet actually will be transferred when the step 2 is going to be happen in j+ first stage switch.

So one there is no moment so one cannot come in the enumerator to again there is nothing is going to happen so packet cannot move there is no packet at the input of the j+ first stage switch 3 again the same case in fourth here is the packet will actually going but this will be only

happening with the half of the probability, so ½ p1 4j+1 k so next in the fifth there is no possibility.

Because there is a blocking so output buffer is not empty in sixth it will be happening but that will be again with the ½ probability, you have to note this I am actually talking about j^{th} stage so I am using j+ first stage a state probabilities. And similarly look at 7 nothing will happen in eight though you actually there two packets are the in the input but do only one of the packet will going out okay so with only half it will be happening.

So we will be putting half p1 because you might be actually talking about the packet which is this one it cannot go through with only 50% it can go through so p18j+1k then similarly when you look at the 9 both of them will go out so I have to put full in 10 they cannot move out so it would not coming in 11 only one of them will actually go out 12 only one of them will going and of course 13 and 14 no packet will go to the outgoing port.

So this is what will be your expression for pj~ okay and boundary condition for this as I mention will be I need it to write it here itself, pn-2 will be always 1.0 okay that happens and of course qj~ will be = 1- pj~ okay so these are the conditions we can now we also need to defines something call pj bar okay so let us define pj bar okay I need to still maintain those state table so I have to write on this side of the board itself.

So I will just make a change is the probability I will just re define it is pj bar so probability of being in a state after a step one in j-1 state it is probability of arrival. Okay so this is the probability that a packet from a input link at j-1 is placed in a buffer at the output links in the previous stage the packet is going the step one happening the previous stage in your stage step two is happening.

Okay so I am talking about j-1 and in terms after step one in j-1 you are actually going through the step two now okay so probability of being in a state after step one there is step one is already executed and your step two is already finished that is what it means so after step one j-1 is stay

switch search that input buffer search that the input buffer of switch in a stage j is free, now this input buffer in stage j is free actually technically also equals.

Output buffer in switch in a stage j-1 okay this we will again de compute this boundary condition will also, so denominator have corrected so for pj bar probability of being in a state after step one in switch in j-1 here stage such that the packet can move to the output of this switch in a step 2, okay so we have already finish a step 2 in j- first stage is step one is finish and this is what is going to be happen.

So when step 2 going to be executed in j-1 first stage the packet has to move to the input buffer so we are now looking into condition probability of arrival so condition down that the input buffer of j^{th} stage switches empty. So let us look how will find out so I need to look in to these states I am looking in to j- first so the switch is something like this so this is your switch okay so you have to find out whether this is free or not free and then the packet will be moving.

So this is the step 2 will be executing here for the moment so after a step one which is happened here they should not be any packet that is the first thing and there is no packet what are the chances that the packet will come so you have find out what is the state of this switch after step one, so that will be governing. So let me actually list down in the denominator all the states such that this input of this particular switch or the output of this switch j- first stage switch is actually free.

So let us look at those and then write down the expressions so if j- first remember I am looking at j- first stage switch outputs have to be free so when you look at the state one both the outputs are free so with the equal probability both the any one of them can be connected to my switch in a stage j so I can write down here p1 you have to be in state 1 j-1 okay after in time a step k, so this will go in the denominator look at the state 2 with half probability I may have a packet, and with another half i will be i will not be having the packet ,so I will put ½ here 1/2p1k U in the state j- first stage switch, then similarly I will have the third one ,third one there is no output buffer ,which will be empty ,or the input buffer for my switch in j^{th} stage, because I am talking about that and sorry this pj bar.

So third one will not come the 4thoone a both of them will come, to this will be 1/2p(1)+4j-1k,then we will have the 5th that is with ½ only this will be happening, and then we will have 6th with ½ only it will be happening, the seventh cannot be there because the output buffers are not free ,eighth both are free so without ½ ,9th both are free so it is again without ½ ,and then we look at 10th only one of the port is free so 10th 11th and 12th will be with ½ actually. 10th,11th and 12th so this completes my denominator.

So then the numerator part is I have to look all those states where they actually packets will be coming in, so when you look at the state 1 there is no packet which will be coming in the next step, so there is no arrival which is going to happen so this will not be listed in the top, so condition on when the input buffer is free I will not be having any arrival.

When considered to nothing will be arriving consider 3 nothing will be arriving, in 4th yes the packet will be arriving with ½ probability ,okay so I will write ½ p14j-1k,then you look at 5th no packet will be arriving ,you have to look at the arrow direction also ,in 6thyes packet will be arriving with ½ probability ,okay, so I will write + ½ p1 5j-1k,look at now the 6th one, sorry this one was should be 6thnot 5th actually ,the 7thnothing will be happen 8thonly one of them will be coming so I will put ½ ,9th both the packets will be arriving .

So i will write p9 there is no ½ here now the 10ththere is no arrival 11ththere is only one which will be arriving, so I will put ½ and 12th only one will be coming so I will put ½ ,13 and 14 will not be there ,so this what actually completes the expression for Pj bar, now boundary condition for this will be P0 bar will always be equal to 1.0 ,this is a complete maximum loading condition which we are looking into. And then of course Qj bar will be equal to 1-Pj bar so these are the two boundary conditions which will be there.

So arrival probabilities will be now being controlled from the input side because in input T0 bar is fixed similarly for the departure probability is Pj ~ the Pn-2 ~ will be equal to 1.0,okay so now once we have these we can build up the state transition table .

So for the j^{th} 1 so I will still keep that state diagram here and show you how you build up state transition table, so remember with this state probabilities I have build up the transition prove I will now generate a transition probabilities Pj bar and Pj ~, which are function of the state probability, so we will do actually iterative computation essentially.

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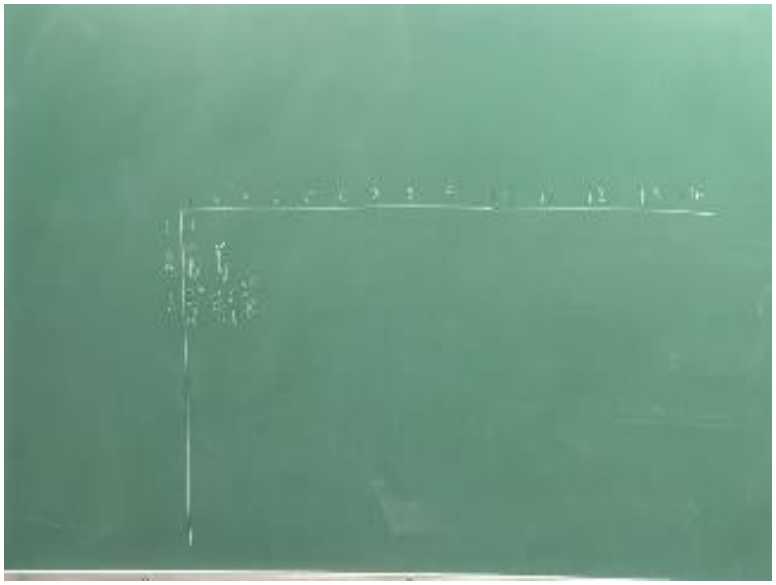

So for the state transition after step 1 so we will have states going from 1, 2, 3,4,5,6, so if you are in state 1 what will be your next state? After step 1, okay, so look in to state 1 after step 1 there is no departure thing here.

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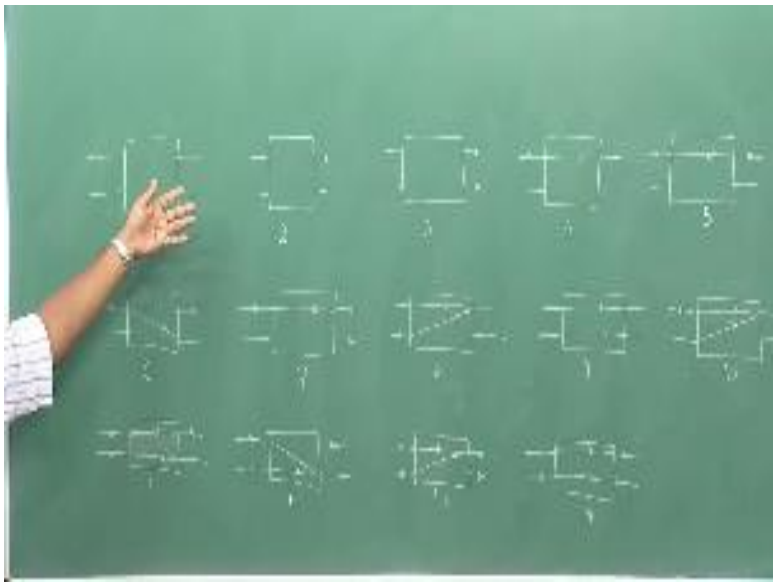

Okay so step 1 is when the packet will be departing so you will still remain in a state1 if you are in currently in state 1 ,so with probability 1 you will remain state 1 ,so rest all elements will become 0 I am only putting non 0 elements here, if you are in the state2. Now this can go out with probability Pj ~ and with Qj ~ this may not go out.

So with probability Pj ~ you will come back to the state 1, so I can write Pj ~ with probability Qj ~ will remain in a state 2 , so now interestingly because by using j-j+ first stage state probabilities you can compute the transition probability is for this stage J and then if you know the current state probability you can actually estimate that the new probability using this algorithm.

So the third one if you in the state 3 so you can remain in the state 3 if none of the packets goes out so you will remain in a state 3 with Qj ~ s^2 if only one packet goes out other one does not go out which will happen with 2 Pj ~,Qj ~, you will come to state 2 so I can write here 2 Pj ~ Qj ~ ,and of course ,both packets goes out you will some to state 1.
Okay, so we can keep on doing it so let me just put in all the valid entries which are there for this, once you know the procedure you can actually compute.

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Ram Chandra

Dilip Tripathi

Manoj Shrivastava

Padam Shukla

Sanjay Mishra

Shubham Rawat

Shikha Gupta

K. K. Mishra

Aradhana Singh

Sweta

Ashutosh Gairola

Dilip Katiyar

Sharwan

Hari Ram

Bhadra Rao

Puneet Kumar Bajpai

Lalty Dutta

Ajay Kanaujia

Shivendra Kumar Tiwari

an IIT Kanpur Production