Indian Institute of Technology Kanpur

National Programme on Technology Enhanced Learning (NPTEL)

Course Title
Digital Switching

Lecture-12

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Okay, so in the last lecture we talked about a time switch and I have also drawn a random access memory based time switch structure.

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And that switch we were doing right operation cyclically and read operation was a cyclic operation. So I was writing in the RAM in order and the slots were coming, so when slots were coming 1, 2, 3, 4, 5, 6, 7, and 8 I was writing them in order actually. And while reading out I was reading in out of order depending as decide by the control memory okay.

So that was a structure which I had discussed in the previous class. So now let us actually do another variation of this, this we call as write acyclic and read cyclic. So if I have to implement this, how this will be done. So I call this particular switch as WCRA and I call this one as WARC, so this what we have done in the earlier lecture, let us do the WARC configuration.

This is almost the same configuration except there will be some manner modifications by which I can implement this scenario. So we will have a speech memory as usual and there is a input line which is coming.

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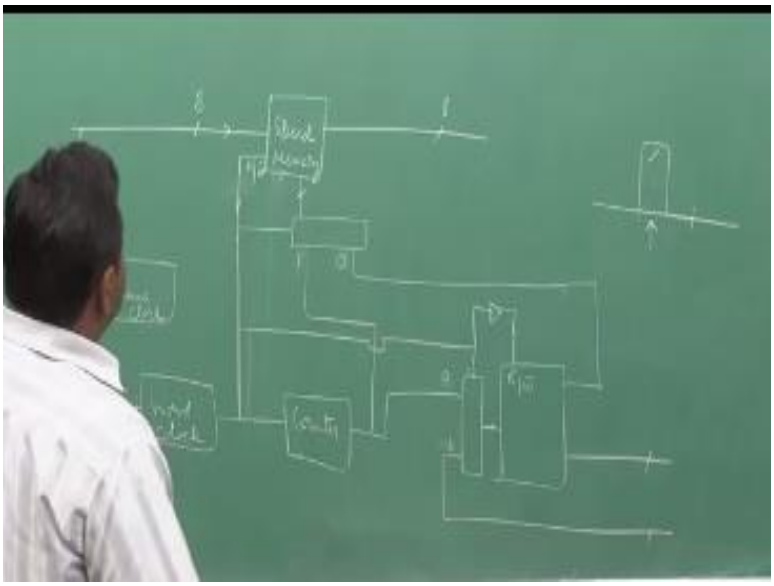

8 bits parallely will be coming through 8 bit toward bus okay, and you will take this same signal and derive a frame clock which is important, I will also drive a word clock this same thing as we did in the previous configuration. We will use this clock to run a counter, so which will be used as an address. But remember this time we are actually doing read which is cyclic which is happening. So I will be using this counters output for read operation. Earlier we actually had used it for write operation okay.

So that will be the variation, and I will be having a mugs RW/ the flag and this of course has to be drive a clock has to go, so clock will also be actually driving this, this word clock will be putting, will be actually driving the memory okay. So this is not an as driven, this is a level driven thing okay, this is not actually required, this is not required here.

So this read, write flag itself will toggle within a clock there, so this will act itself as a clock. So counter I can actually put one counter value, now this time, this same clock will be used to choose one of the inputs either the counter or one which is going to come from a control memory. This you can actually observe this is exactly what we had last time, but only variation which will come is we are actually again assuming that during the one part, the clock actually consist of 1 as 0.

So during the first half the clock you will be doing right operation and second we will be doing a read operation so this actually when it will be 0 I will be connecting the counter value for the read operation and we will be reading out at that time and when it is 1 then I will be right operation which will be decided by this control memory so this same control memory will now be used for so when this is 1 that time just control memory should connect here I can actually do it this way and this is the same clock can be used to select this okay.

And when this clock is one I am actually writing okay so I have to put a not get her so in fact I do not want to put it I have to just simply swipe this and that will ensure things are happening this way so when it is 0 you are writing that time when it is 1 then you are reading it out this one is going to come from the controller this is the address bus this is the data bus and of course there will be a read write flex so when you are to do a write operation here you will be doing a read operation here.

So therefore this clock then inverted thing as to be fit here I think I had not forgotten this particular stuff in the previous lecture so you can add this correspondingly so RW bar for the control memory was not drawn that time so this one gives you a complete write a cyclic and read cyclic configuration, so whenever when you are writing is.

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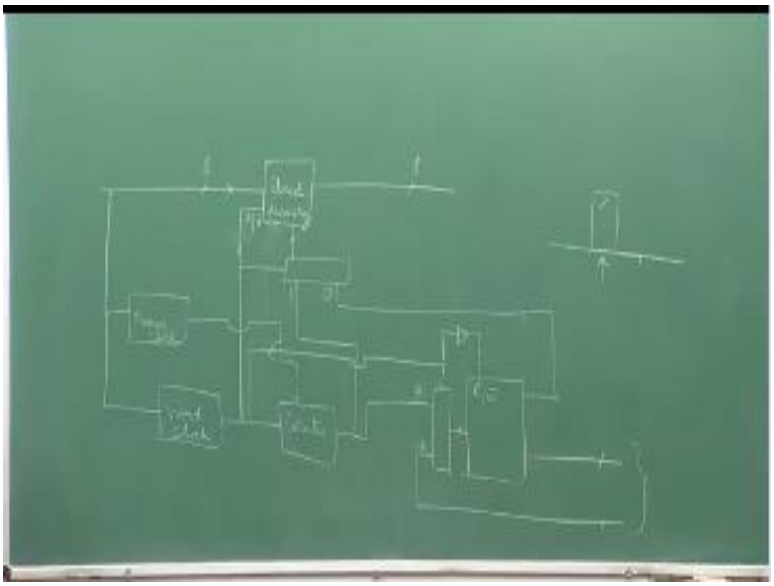

When the word clock is one okay now this frame clock will be used to the do the rest of the counter so when it is 1that time you are reading from here and for reading you are deriving you are taking the address for this speak memory from counter so this one will get connected here okay and during this period when this is one from your control circuitry from your processor you can write into the control memory that time.

So all the controls signals for this switch block and the control action is give read by this the map between input or output and this can be written when the clock is one here when clock goes to 0 this time this counter will be connected to this address bus so in which slot in which location we have to write that particular slot which is coming here that will be governed by what is written here in the memory okay so if when 1 is coming here so here the one location will tell 5 so whatever is coming in 5 will be written into the 5^{th} location in this speak memory so we will do an example whereby you can actually figure out.

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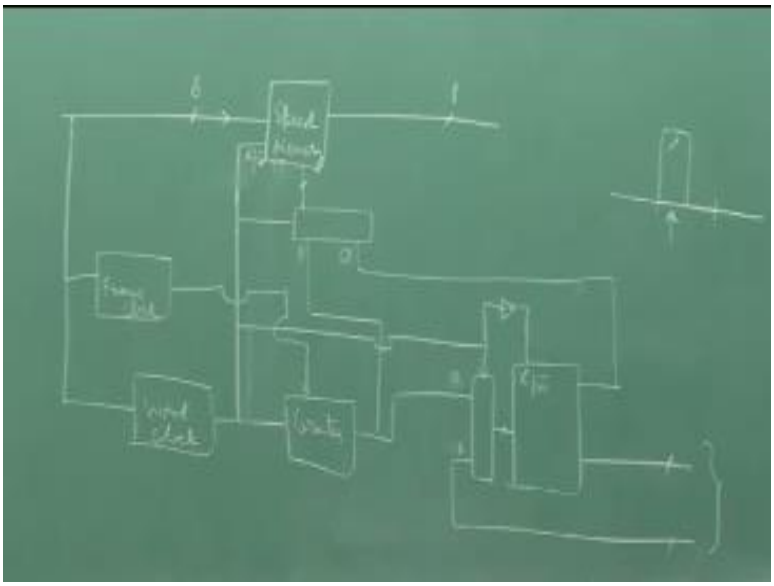

How the map happens between the 2 cases.

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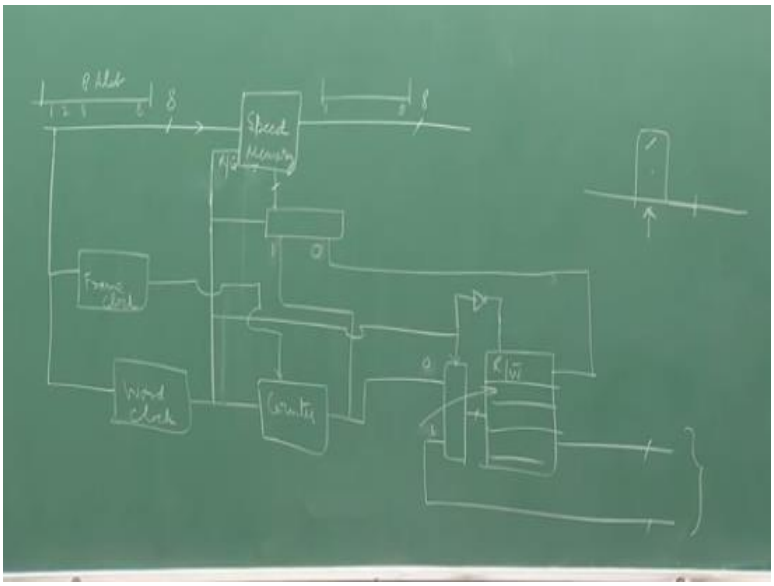

So let me take a case again this is same as I am going to have 8 slots in the frame these are counted as 1, 2, 3,4, 5 till 8 and I have again these 8 slots and the mapping as to be done between these two so I am actually taking an example whereby I have to decide that at which location what has to be written in the control memory, so let us do that. So I am actually taking a switching map.

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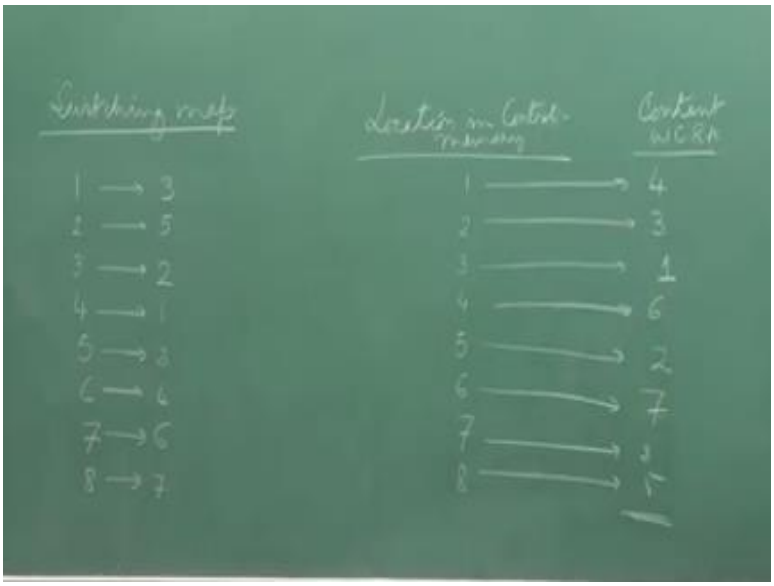

So one has to go to 1 basically slot one whatever is coming in the input has to be mapped to 3. So 2 has to be mapped to 5, 3 has to be mapped to 4, 1 has to be mapped to sorry 4 has to go to 1, 5 has to go to 8, 6 has to go to 4, 7 has to go to 6, 8 has to go to 7, in fact you can take anything this I have just taken any something which is arbitrary, arbitrary map you can take anything and you can do this exercise for your understanding.

So when I am going to have this is a location in the input, okay. And what is going to be in the control memory, this is the location in control memory sorry, location in control memory and what is going to be stored in that control memory the content part this is the content for write cyclic read a cyclic and this is the content which has to be kept in write a cyclic and read cyclic, okay.

So there will be 8 locations in the control memory because it is a 9 slot, 8 by 8 switch so I will have 1,2, 3, 4, 5, 6, 7 and 8 so if the we have WCRA switch okay, so wavelength that write is happening cyclically but read is a cyclic, so I have to connect from 1 to 3, do remember when write is cyclic this one must have been written in this speech memories first location and during third slot it should be read out.

Third slot it should be read out so third location in control memory should contain 1, okay. So 3rd slot should contain 1 so essentially I have to look at this and based on that whatever is here I have to go in the content, okay. So because 3rd slot I want to read out from the first location so third slot I want to read out from the first location, 5th slot I want to read out from 2nd one, 2nd in the 2nd slot I would like to read out from the 3rd one.

In the 1st slot I would like to read out from the 4th one, 8th slot I would like to read out from the 5th, 4th I would like to read out from 6th and 6th I would like to read out from 7 and 7th I would like to read out from 8th, so if it is a WCRA switch this is what with the content in the control memory, now let us come back to this configuration, this is the one which we have done earlier, okay.

If I use WARC which is this configuration what is going to be written in the control memory, so I am going to read out from 1st, 2nd 3rd location in order I will be in first slot will be reading out from 1st, so if I want to map to 3rd location 1 to 3 I should write in the 3rd location so in the first slot whatever is coming I should write in the third location okay, so what this actually means so that when the third slot will be coming here on this side.

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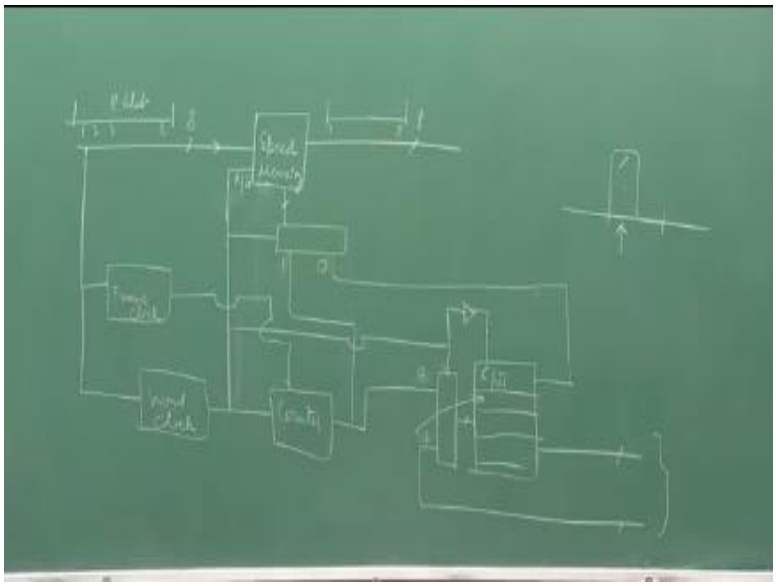

It will be the third location will be read out in the third is stuff.

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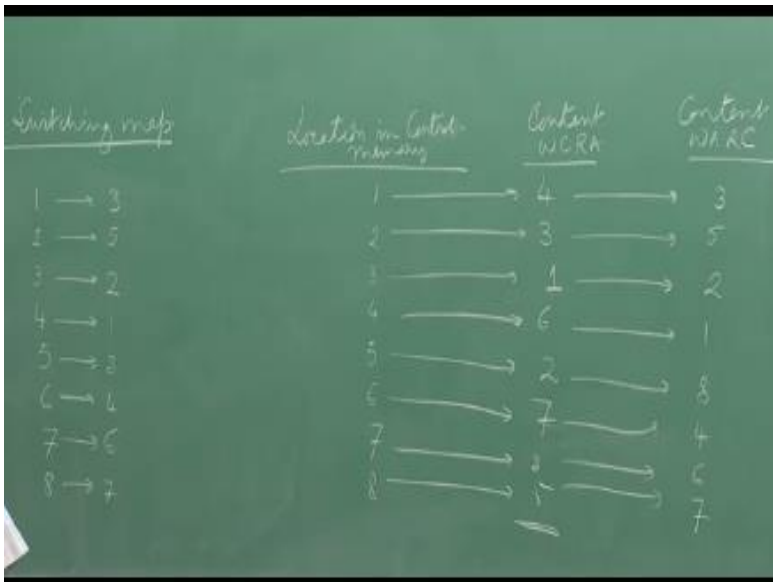

So one will map on to three two will three four to five okay and three will go to two so we will have two one eight four six and seven that is what will be the difference so you can try out various different map center right to find out what will be the content in two different kind of time switches.

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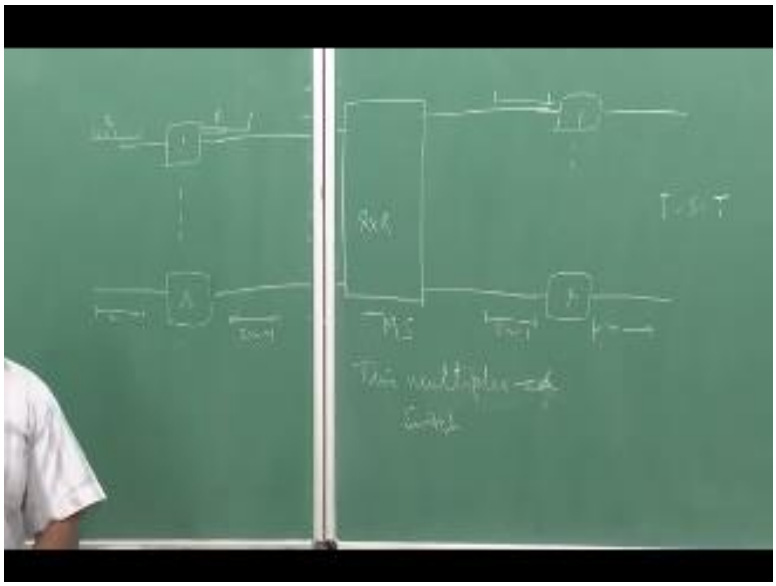

Okay now let us look at a three stage Clos network I actually discuss about three stage Clos network but I actually had used a crossbars in that case okay, so can I use this time switch to build up a three stage Clos network that is a position you would like to investigate the Clos network was something like this where I had some m/n kind of crossbar which I have been used so I had used multiple of them say r of them so in the middle stage I had used an r/r switch and correspondingly the third stage will be something like this.

I have got a crossbar now question is can I actually used time switches here yes I think this can be done I can replace this whole block by a time switch so this is an equivalent because I can have a multiplexer and then I created time multiplexed stream I can use the time switch here and then I can have a multiplexer stream where were slots have been interchanged through a time slot interchanger and I can then do time switch demultiplexing so if you look from here this is nothing but a space switch which you are using here.

So I can technically represent technically all replace all this first and third stage by these time switch blocks, so what will happen because of this so I will end up and getting a time switch and actually putting a time switch here but they are multiple of them and I can actually use debugs,

okay and I can do similar exercise here on this side this is the time switch and time multiplexers stream and I have replaced it by time switches.

Now but one important thing which you can actually observe when you have time slot one because these are this 8/8 slot for example as an example so 8 slots will be here, okay and once you have 8 slots you actually can in time slot 1 this is the switch which is will be operating all the switches are meaningless because in this demultiplexer only this will be corresponding to time slot 1, so this one corresponds to time slot 1, this will be activated in time slot 2, this will be used in time slot if it is m/m so let us time slot m, okay.

So all of them will be used only in and each one of them is r/r space switch, okay and similarly when they will be coming this will be taken in time slot 1, time slot 2, time slot m and then you get a time multiplexers stream coming out here. I can do something because all these switches are not being use simantously I can remove this and if I can only use one switch which can in one sort work like this second plot it can move and operate like this one and m slot is operates like this one I can use only one single space switch and it will work in time multiple section every slot it is configuration will change if I can do that I do not require this d max n max actually.

And we get a configuration which is called TST time space time configuration okay so this I can actually very well replace this stuff by one single switch which is r/r earlier there are many of them m of them like this and I just connect these okay, so when time slot one is there her times slot one here will be times slot one this will be one configuration input output maps so there will be m maps and they will be now changing every times slot so this switch will be changing continuously.

So I have to store it somewhere okay I will store it in a control memory corresponding to this switch these time switches any way I have control my orgy as we have discussed earlier. So I can actually built this is known as TMS times multiplex switch so it this is actually a single cross bar but due to time multiplexing it is acting like multiple cross bar switches okay. So if I have a cross

bar like this I am drawing only a small one the 4/4 so I have 1 2 3 and 4 1 2 3 and 4, so I have to decide in the first times slot which one of these will be active.

Remember this all of them cannot get active only one of the point in a column get active where multiple in the row can get active that is possible so this can snap but all these four cannot snap together only one of them so I can do addressable tuff and this can be control through a control memory so time slot one will tell which one of these so there will be two bits here because there only four possible options which required two bits so which one of the cross point will get activated time slot 2 which one of the get activated and so on.

Similarly I will use these cross points will be addressable control by another control memory another control memory and whatever is a frame clock I am going to be assumethis to be synchronised all the inputs, that word clock and frame clock actually be use, to generate the addresses here. So the similar structure what we had in the time switch will be required in this case and this TMS can be put in here, and I get a TST configuration.

So important thing is the amount of hardware reduces drastically here, because I don't required large number of cross bars, I can work with much smaller number, so far life was very simple, I had 8/8, or m/m, I have used and this configuration I know, okay, but if suppose if I want to build up a constructive non blocking switch, what I will do? So, in this case in this cross bar these three stage network, what we required was here.

If this is M I need this N, $N>2(m-1)\geq 2(m-1)$, if this condition is satisfied, I get a restrictive non blocking switch, what's a equivalent condition in this time space time switch, okay, so this condition will be when the slots here are M slots, I need here at least 2m-1 slots, but I have not talked about a time switch, which is having different number of inputs here and different number of outputs here.

And on the other side the number of inputs here are larger, it is 2m-1, and it is m, so I need an implementation of time switch, where number of inputs per frame, and number of outputs per frame are different, they cannot be implemented by one single species memory, so remember in

earlier time switch implementations, in first half of the clock, I was either doing read or write, on otherwise second half of the clock I was doing write or read, okay the corresponding thing.

So depending on weather it's a right cyclic or read cyclic, again do either way around, okay, so how to implement this time switch? So we need to look in to this aspect, so we will look this, into this thing in the next module.

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