Indian Institute of Technology Kanpur National Programme on Technology Enhanced Learning (NPTEL) Course Title

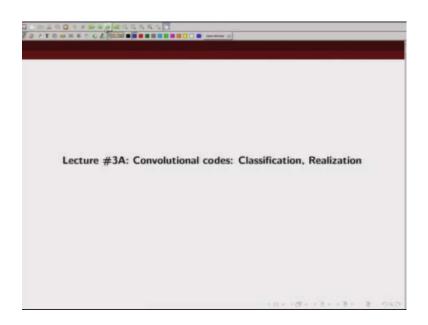
Error Control Coding: An Introduction to Convolutional Codes

Lecture-3A Convolutional Codes: Classification, Realization

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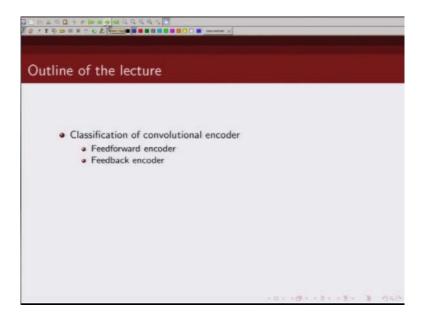
Welcome to the course on error control coding an introduction to convolutional codes. In this lecture.

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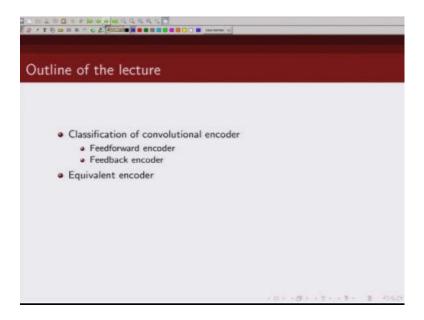
Today we are going to talk about classification of convolutional codes based on type of connections between the output and the input. Also based on what are our output bits, we will classify convolutional codes into systematic and nonsystematic codes. Then we are going to talk about how we can realize convolutional code using shift registers.

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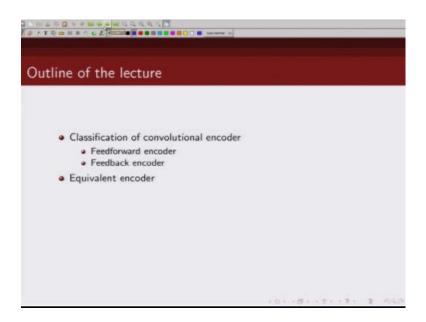
So at the set first we will talk about convolutional codes and in this we are going to talk about a classification based on types of connections between the input and output of the convolutional encoder. In this regard we are going to talk about what do we mean by feedforward encoder and feedback encoder.

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Then we are going to introduce our classification based on what are the output bits whether the information bits directly appears in the output or not based on that, there will be a classification of convolutional code.

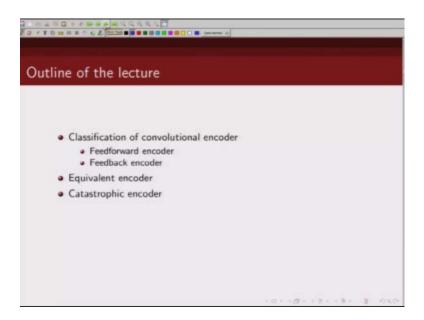
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The encoder basically where information bits can be separated out is known a systematic encoder and in nonsystematic encoder we cannot separate out information bits directly from the parity bit. So we will talk about what do we mean by systematic encoder for a convolutional code and nonsystematic encoder.

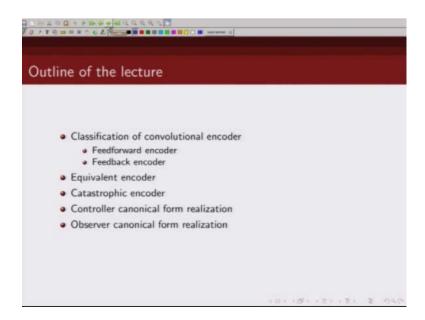
And then we will introduce this concept of equivalent encoders. So for every nonsystematic encoder there is an equivalent systematic and through an example we are going to illustrate how we can get its equivalent encoder.

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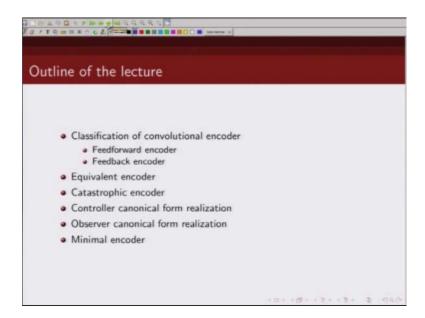
Then we are going to talk about a class of encoder where if the input bits are very high weight we can still get an output code word of very low weight and this kinds of encoders are known as catastrophic encoders.

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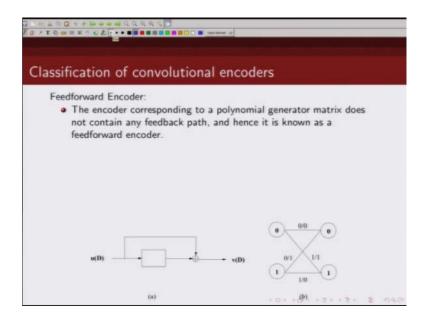
And finally we are going to talk about two different types of realization of convolutional codes using shift register. The first one which is known as controller canonical form realization and the second one is known as observer canonical realization.

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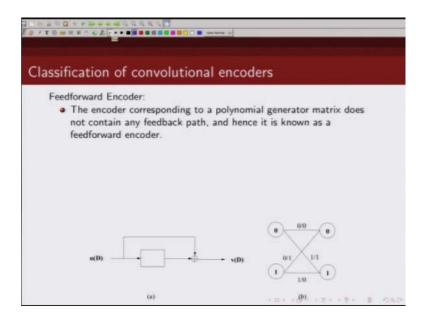
And finally we are going to conclude this lecture with the concept of minimal encoder.

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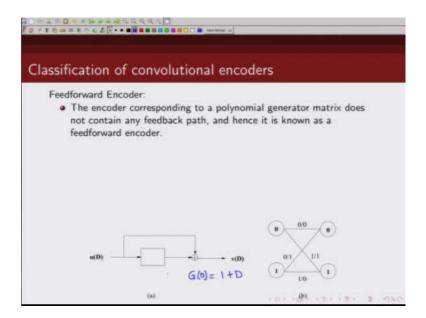
So let us start our discussion on classification of convolutional encoder the first type of encoder that we are going to talk about is known as feedforward encoder. So what is the feed forward encoder?

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The encoder corresponding to a polynomial generator matrix which does not have any feedback from the output to the input is known as feedforward encoder.

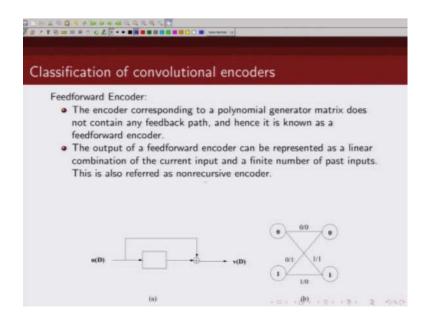
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Let us take this example this is our information sequence v(D) denotes our coded sequence. What is the generator matrix G(D) in this case it is given by 1+D. Note here the generator matrix here is a polynomial generator matrix right, as suppose to a rational generator matrix and there is no feedback from the output to the input side.

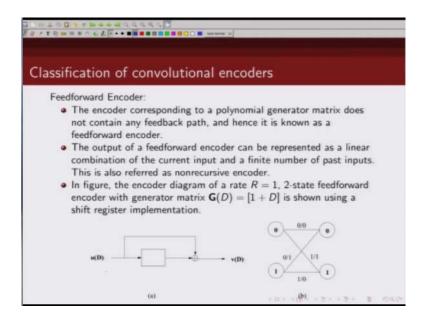
You can see basically the output depends on the current input as well as the input one pass time instance. So there is no feedback from the output to the encoder side. And this is an example of a feedforward encoder.

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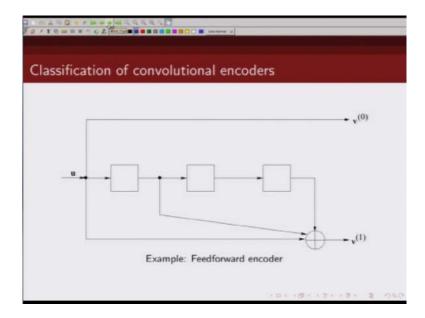


Now we can represent the output of a feedforward encoder as linear combination of current input and finite number of past inputs. We also refer this type of encoder as nonrecursive encoder.

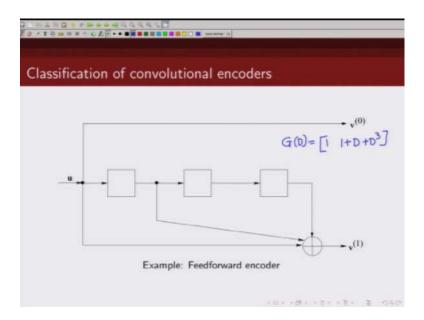
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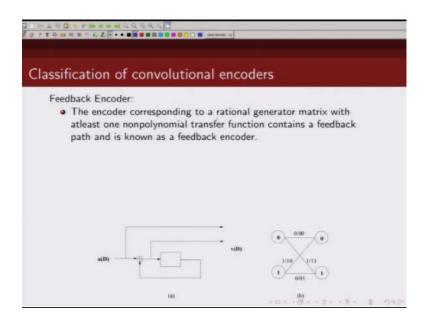
And as we said in this we have an example of a rate one code, because input to one bit, output there is one bit coming out, and the generator matrix of this rate one code is given by 1+D and you can see it this is of example of a feedforward encoder whose generator matrix is a polynomial generator matrix and there is no feedback from the output to the input side. And this is this corresponding state diagram for this feedforward encoder.



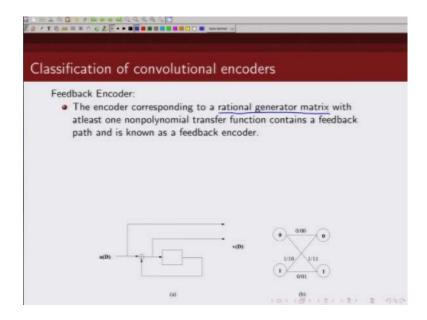
This is another example of a feedforward encoder we can write down the generator matrix for this.



G(D) $v^{(0)}$ is nothing but the input bit so this first one is just 1. And what about the second parity bit this is information bit so we have 1 plus one delayed version of this information bit plus D^3 . Because this is one, two, three, three time instance delayed version of u, so this is the generator matrix. This is also polynomial generator matrix and there is you can see, there is no feedback from the output to the input side.

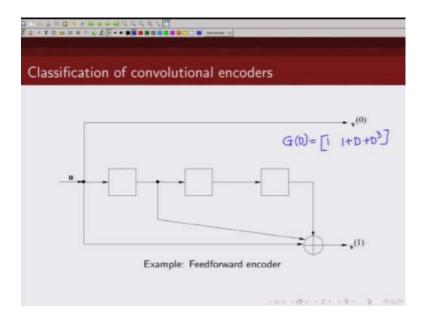


Now let us look at what do we mean by feedback encoder as opposed to a feedforward encoder.

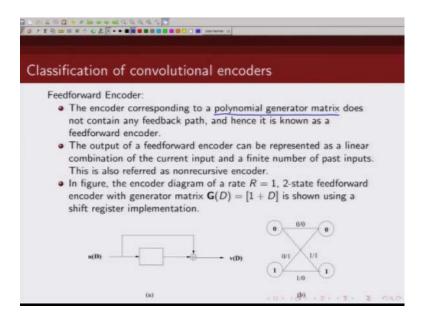


The encoder for a feedback encoder has a rational generator matrix please note here.

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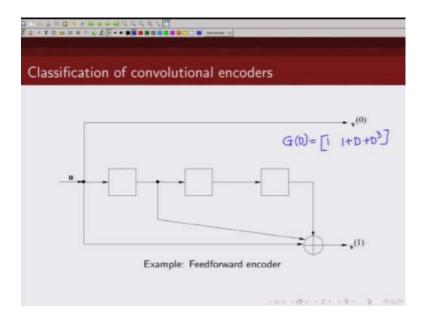


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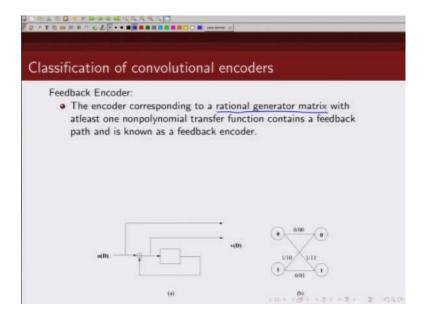


We had a polynomial generator matrix for a feedforward encoder we had a polynomial generator matrix.

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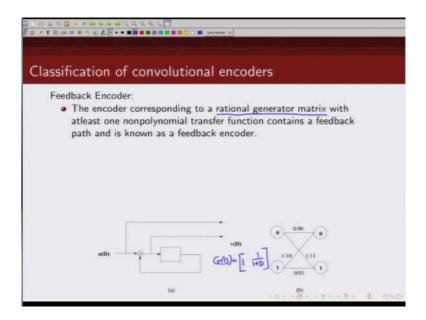


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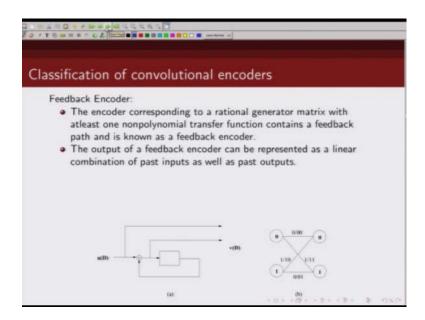
Whereas for a feedback encoder we have a rational generator matrix with at least one nonpolynomial transfer function containing a feedback path from the output to the input. Look at this example from the output we can see there is a feedback going to the input side.

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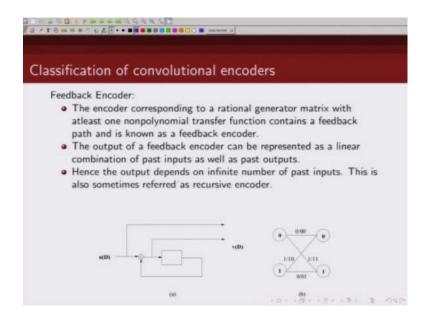
And the generator matrix for this is basically - so first coded bit is nothing but the information bit so that is one, and this is basically 1/1+D.

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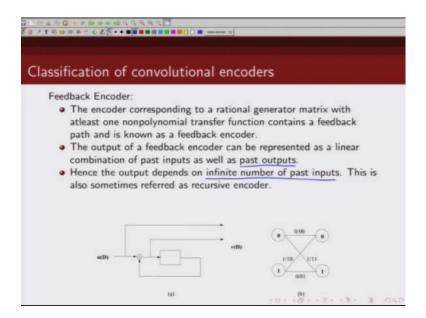
So, because there is a feedback from the output to the input side output of a feedback encoder can be written as a combination of past input as well as past outputs.

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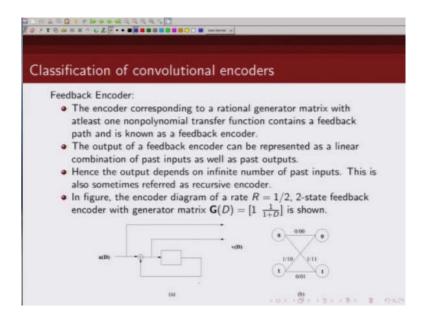
Hence the output depends on infinite number of past input.

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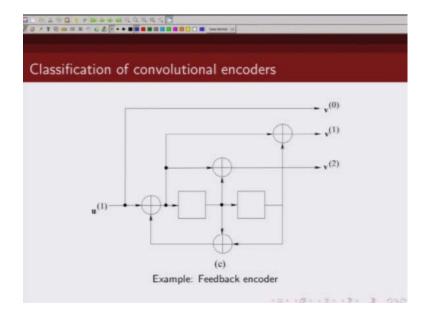
Because the current output depends also on past output and past outputs also depends on past inputs and past output. So the output will basically depend on infinite number of past inputs. Now feedback encoder is also known as recursive encoder.

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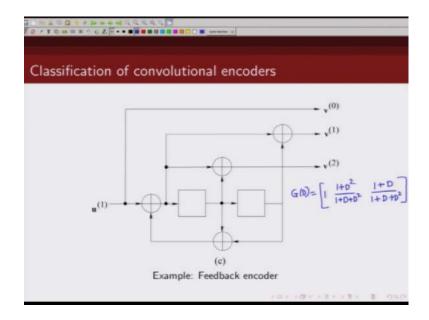


And we just now mentioned one example of this feedback encoder is given in this figure. This is a ray to one half code you can see for one input, we have two outputs and is generator matrix is given by this. This is this corresponding state diagram for this feedback encoder.

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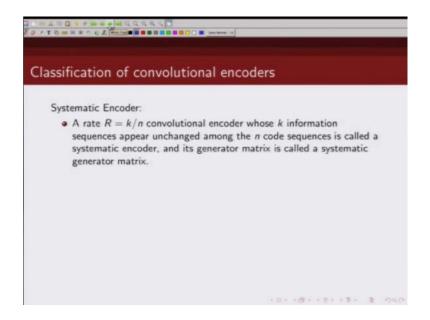


This is another example of a feedback encoder, so there is one input and there are three outputs.



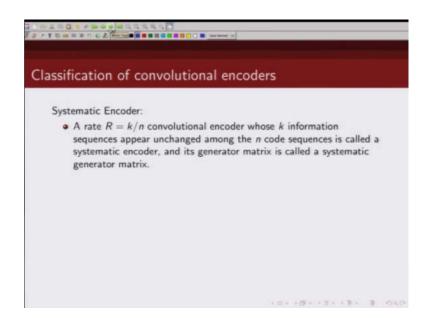
We can write down the generator matrix G(D), the first output is nothing but the information bits so that is one. Now what are the feedforward terms in $v^{(1)}$ so D^1 depends on this bit and this bit. So this is $1+D^2$ and what is the denominated term, we have basically $1+D+D^2$ term. Similarly v^2 is basically given by 1+D and this is $1+D+D^2$. So this is the generator matrix for this feedback encoder.

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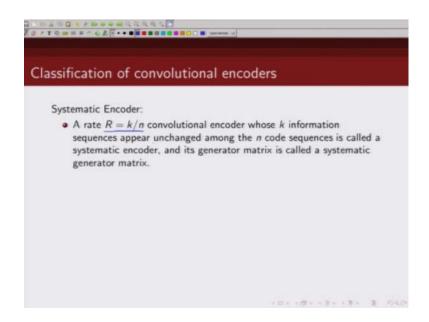


The next classification that we are going to talk about is based on output bits whether we can separate out the information bits from the coded bits.

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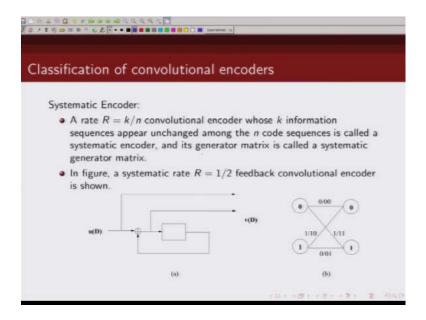


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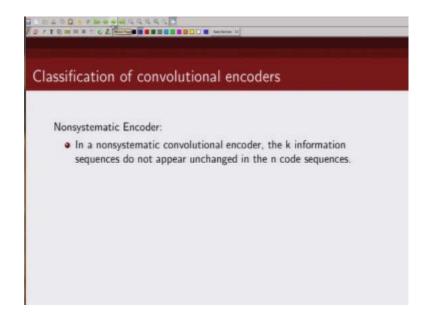
So in a systematic encoder a rate k/n systematic encoder, the k information bits appear unchanged in the output. So out of those encoded bits you can directly see the k information bits and rest n-k-bits are your parity bits.

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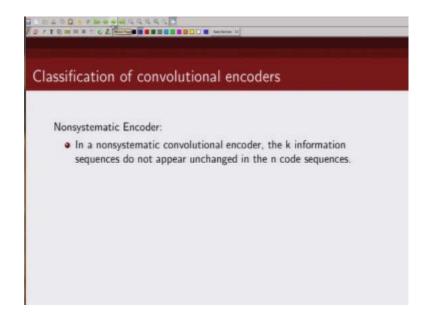


And the generator matrix corresponding to a systematic encoder is known as systematic generator matrix. Take example of this rate ½ feedback encoder you can see there is one input and there are two outputs so it is rate ½ and it is a feedback encoder there is a feedback from the output to the input side. You can see here the first coded bit is nothing but the information bit.

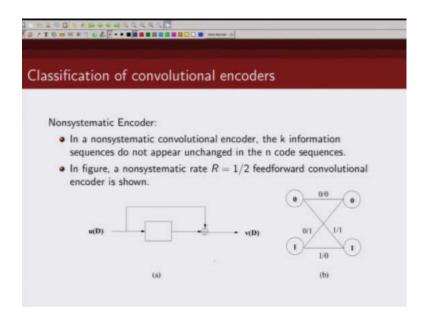
And the second coded bit is, is parity bit basically coming out from this convolutional encoder, so from these two coded bits we can easily find out what the information bit was from this bit so we can separate out the information bit from the coded bit and this is example of a systematic encoder.



As opposed to a systematic encoder in a non systematic encoder.



We cannot separate out the k information bits from the n coded bits.

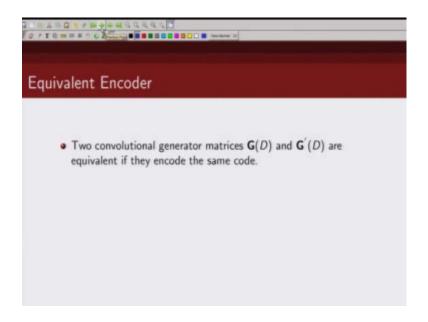


This is an example of a one second I want to make it a rate 1 this is actually rate

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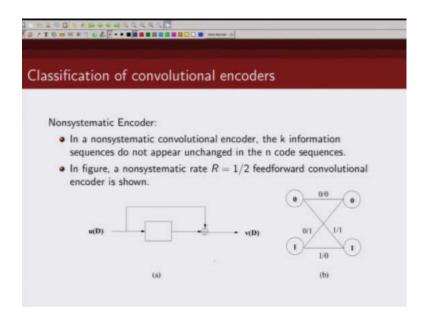
Just type this is a rate 1 code because this 1 there is input and there is 1 output this is a rate 1 and this is a feedback output this is a rate 1 and this is a feedback feed forward encoder you can see there is no feedback from the output to the input side, so it is a rate 1 feed forward encoder and you can see the output bit is given by this current input bit and this past input bit so you cannot directly take out the information bits from this coded bit. So this is an example of a non systematic encoder.

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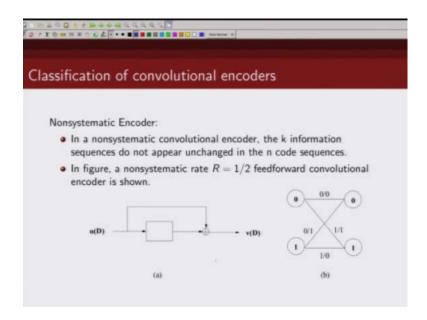
We could also define a class

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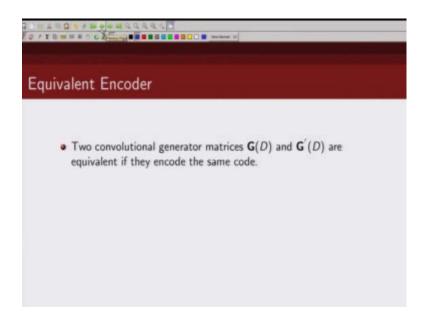
Which is called partially systematic encoder so in a partially systematic so if you have rate k/n partially systematic encoder out of those k information bits some of them appear on change in the output while some of the information bits do not appear unchanged in the coded bits so in a systematic rate k/n encoder we can see directly the k information bits I a partial systematic encoder we can see a fraction of these k information bits may be few bits like from 1 to k-1 and in an all systematic encoder we cannot see any systematic bits direct in any information bits directly in the output.

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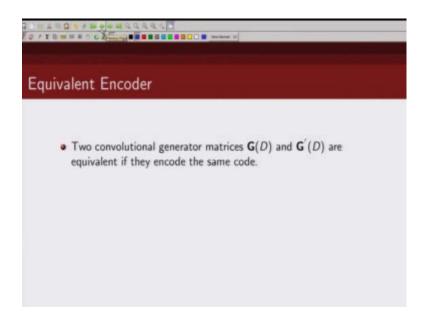
So all the parity bits essentially liner combination of current and pass inputs and outputs.

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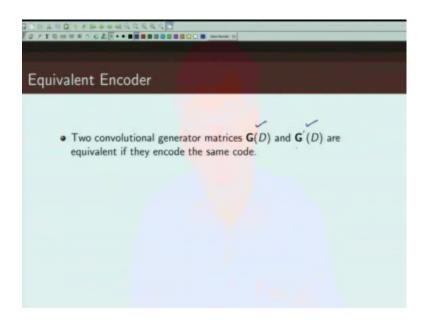
Now that brings us to our next topic of discussion which is a concept of equivalent encoders.

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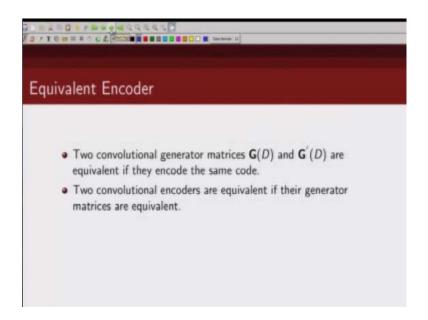
So before we defined what is an equivalent encoder we will defined what is an equivalent encoder we will defined what do we mean by equivalent generator matrices so we do convolutional generator matrix let us call it G(D) and G'(D) re equivalent if they encode the same code now what do we mean by encode the same code. So the set of

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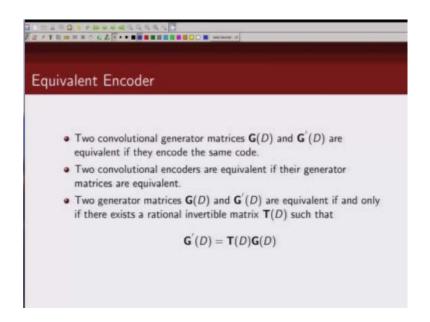
Code words generated by this and this if they are same then these generator matrices are equivalent now the set of code words generated by these generator matrix are same but the mapping between the input and the output is different in this encoder from what the mapping between inputs and output is for this generator matrix

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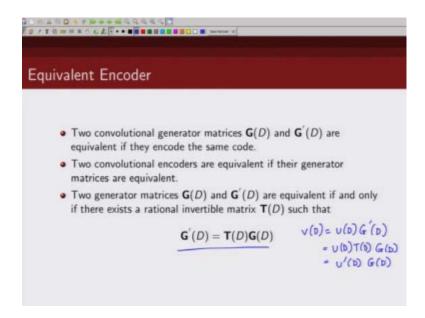
Now we say do convolutional encoders are equivalent if their generator matrix are also equivalent in other words if they are a generator matrix encode the same code then we say two convolutional encoder are equivalent.

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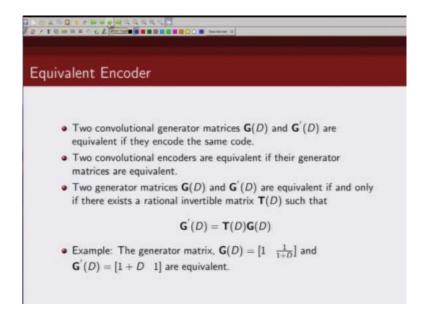
So if G(D) and G'(D) are equivalent this condition.

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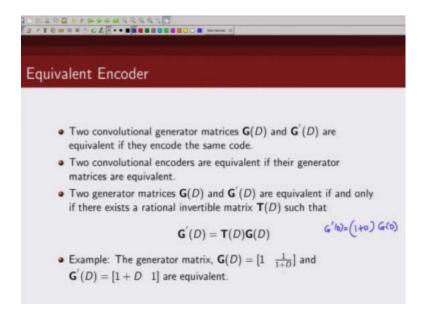
Should hold so two generator matrix are equivalent if and only if there exists a rational invertible matrix T(D) such that we can obtain G'(D) by T(D) multiplied by G(T) okay and we can see basically so let us say set of codes generated by G'(D) so that would be V(D) it will be U(D) times G'(D) now this we can write as U(D)T(D) times G(D) let us call U(D) T(D) is U'(D) G(D) okay

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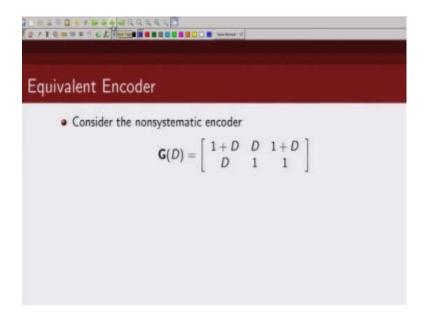
So let us take an example this G(D) 1 1+1/1+D AAND G'(D) which is 1+D 1 these are equivalent encoders because we can write

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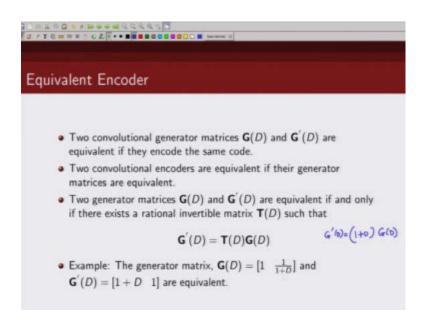
G'(D) as 1+D times G(D) okay so far and we can see this is a systematic encoder generator matrix for a systematic encoder okay now for.

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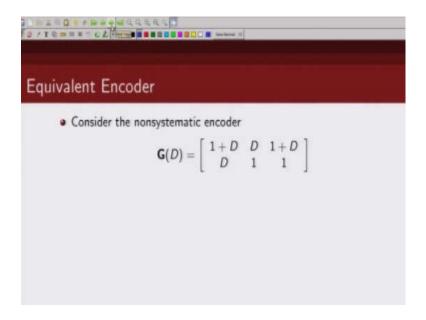
A and this is

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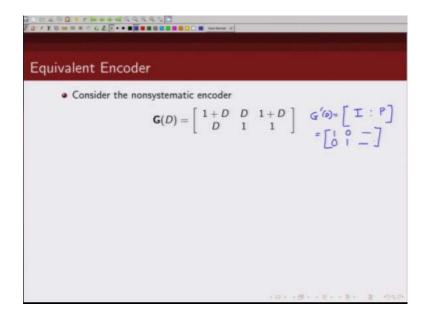
A feedback encoder this is a feed forward encoder.

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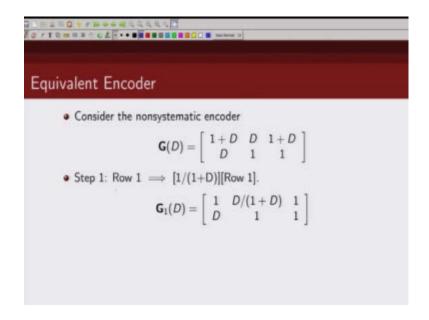
So let us take an example of nonsystematic feed forward encoder and let us try to fine it is equivalent systematic encoder s what would be the equivalent systematic encoder corresponding to this nonsystematic encoder the generator matrix

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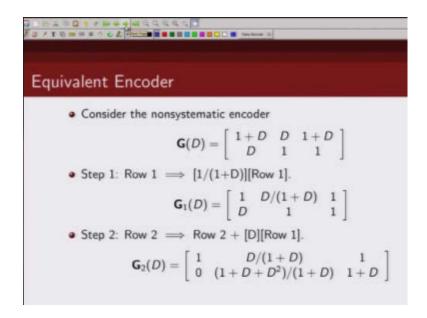
G'(D) should be of the form identity and some matrix P so what we want is basically we want this to be of the form 10 something here 01 something here so we want to convert this into a form of this type okay so we will do elementary operation to bring this generator matrix into a a generator matrix of this form.

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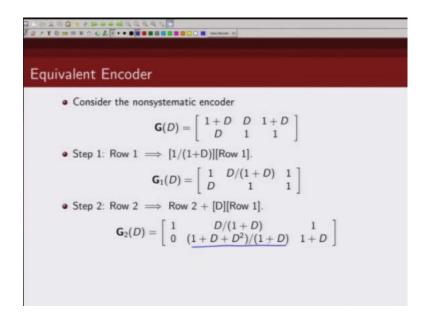
So first so we will do this transformation row 1 we will try to make this as 1 how can we make this as 1 if we multiply row 1 by 1/1+D if we do that this term will become 1 this term will become D/1/D and this term will become 1 we leave this second row unchanged next

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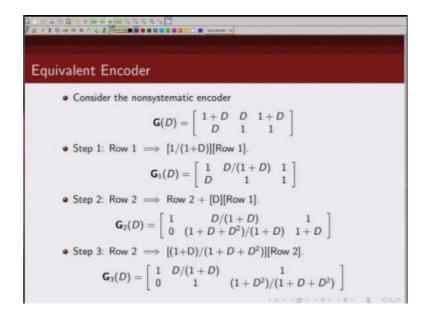
We want to get a 0 here right how do we get a 0 here we do this transformation row 2 will make it row 2 + D times row 1 so the first row is unchanged but second row we do this transformation it is row 2 + D times row 1 so row 2 here is D + D times row 1 which is another D so D + D is 0 similarly row 2 this $1 + D^2/1 + D$ this is basically given by.

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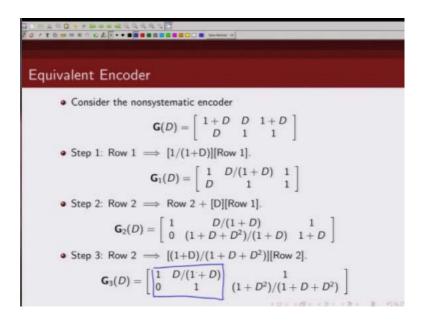
This and we have 1+D which is this term so what we have done is we have converted this into form 10 next we want to get a 1 here right we want to get a 1 here so how can we get a 1 here we will.

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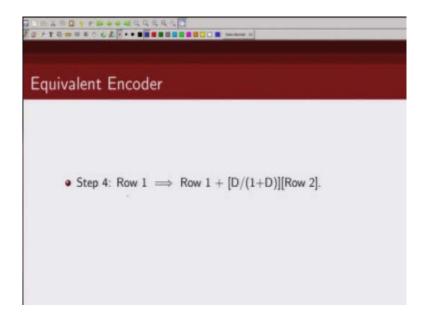
Do this following transformation so for row 2 we will multiply row 2 by $1+D/1+D+D^2$ so if we do that then this will become 1 so we leave the first row uncharged here 0 if you multiple by this it does not change if you multiply this by this we get a one here and here we get this term so now what we have got so far is we got 1 here we got a 0 here we got a 1 here now what else is remaining we have to make this a.

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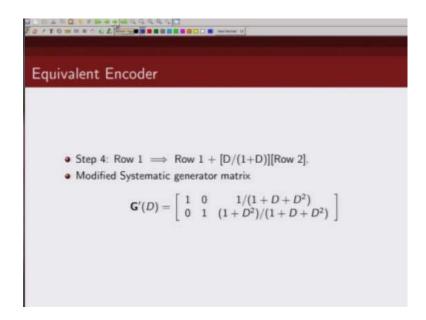
We make this a identity matrix so we have to make this as 0 how can we make this as 0 we multiply this by this and added up to the first row we can make it as 0 so next.

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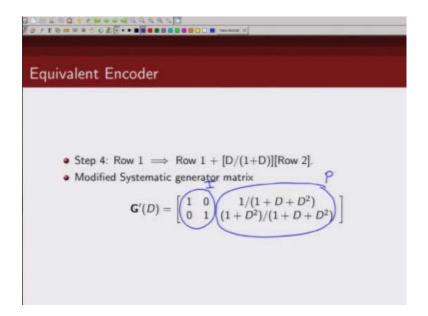
To row 1 we add D times 1 1+D times row 2 if we do that

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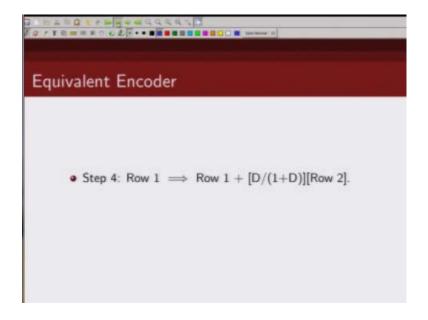
The modified generator matrix that we get is this note now this a generator matrix for a systematic encoder you have your identity matrix here

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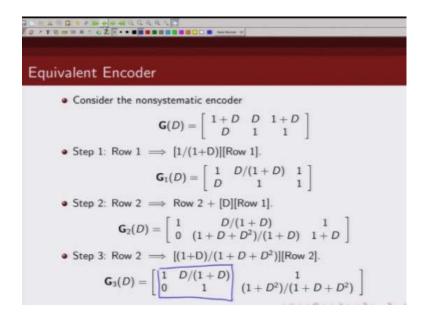
And you have some matrix here which is your P matrix so this is basically the generator matrix for a systematic encoder.

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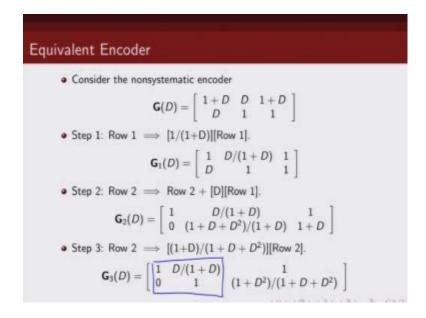
So note now.

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By simple row operations we were able to get an equivalent systematic generator matrix for a none systematic encoder

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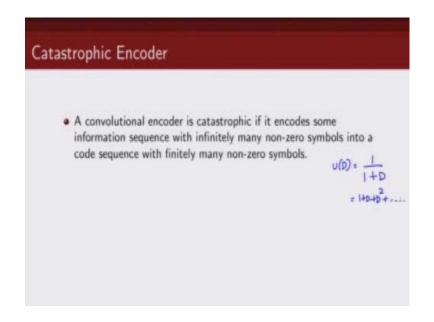
By simple row operations we were able to get an equivalent systematic generator matrix for a nonsystematic encoder whose generator matrix is given by this.

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A convolutional encoder is catastrophic if it encodes some information sequence with infinitely many non-zero symbols into a code sequence with finitely many non-zero symbols.

Next we will explain the concept of catastrophic encoder, so convolutional encoder is catastrophic if it encodes some information sequence which has large weight which has large number of once into a code sequence with finite number of once so if you have an informational sequence let us say u(D) which is 1/1+D.

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Now this is a sequence of all once, this is basically nothing but 1+D+D² so this is a sequence of one all once. Now if you have an encoder which maps a sequence input sequence which has large number of once into a sequence coded sequence with finite number of once now that type of encoder is known as catastrophic, catastrophic encoder.

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Catastrophic Encoder

- A convolutional encoder is catastrophic if it encodes some information sequence with infinitely many non-zero symbols into a code sequence with finitely many non-zero symbols.
- This means that a finite number of channel errors may result in infinitely many errors in the receiver.

Now why is it catastrophic? So to illustrate it we will take an example it is a catastrophic encoder because a finite number of channel errors can result in infinite number of input errors because you had well inform just sequence which has large number of once possibly infinite number of once because that information sequences getting map to a coded sequence with finite number of once if error happens in those locations.

Where you have finite number of once then your output sequence will get transformed into an all zero sequence and your decoder will think that you have transmitted and all zero sequence, whereas actually you where transmitted a sequence of all once so finite number of channel errors in case of a catastrophic encoder can result in infinite number of input errors.

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Catastrophic Encoder

- A convolutional encoder is catastrophic if it encodes some information sequence with infinitely many non-zero symbols into a code sequence with finitely many non-zero symbols.
- This means that a finite number of channel errors may result in infinitely many errors in the receiver.
- Example:

$$G(D) = [1 + D \ 1 + D^2]$$

Let us take an example of this encoder with generator matrix G(D) which is given by 1+D and 1+D² and let us feed input which is all sequence of all once which I can write as 1/1+D.

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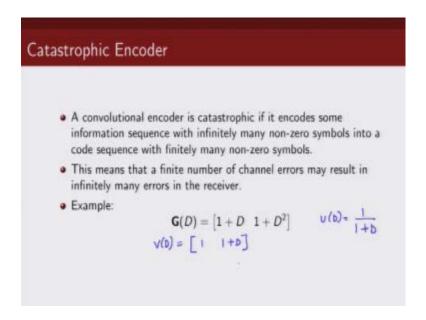
Catastrophic Encoder

- A convolutional encoder is catastrophic if it encodes some information sequence with infinitely many non-zero symbols into a code sequence with finitely many non-zero symbols.
- This means that a finite number of channel errors may result in infinitely many errors in the receiver.
- Example:

$$G(D) = [1 + D \ 1 + D^2]$$
 $V(b) = \frac{1}{1 + b}$

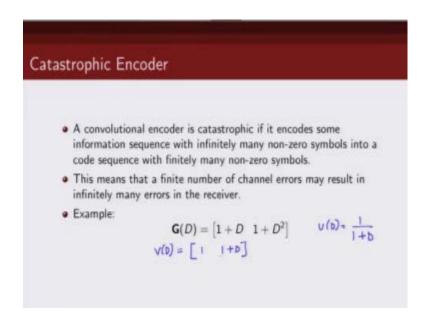
Now if this information sequence passes through this encoder what would be your output sequence it output sequence would be 1 and this will be 1+D.

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So what you will get is, you will get an output sequence which has weight only three, whereas your information sequence has infinite number of once so here is an example where an input sequence of very large number of once getting mapped to an output sequence of only weight three, what if error happens in these three locations where you had once? Then your output sequence that the decoder will receiver will receive will be all zero sequence and the receiver will think that you transmit you transmitted all zero sequence.

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Whereas the input is all one sequence, so you can see in case of a catastrophic encoder a finite number of error in this example only three errors can result in infinite number of errors input errors, okay.

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Catastrophic Encoder

- A convolutional encoder is catastrophic if it encodes some information sequence with infinitely many non-zero symbols into a code sequence with finitely many non-zero symbols.
- This means that a finite number of channel errors may result in infinitely many errors in the receiver.
- Example:

$$G(D) = [1 + D \ 1 + D^2]$$

• If the input sequence u(D) = [1/(1+D)] = 1+D+D²+···, then the output sequence, [1 1+D] has only weight 3, even thought the information sequence has infinite weight.

This I have explained.

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Controller Canonical Form Realization

 In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.

Next I am going to come to the topic of realization of a convolutional encoder how can we represent a convolutional encoder using shift register so given a generator matrix how can you implement a convolutional encoder, so in this we are going to talk about two such type of realization, the first one that we are going to discuss now is known as controller canonical form realization.

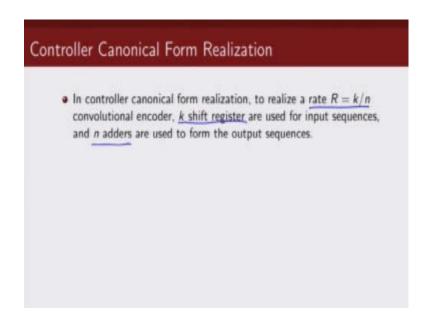
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Controller Canonical Form Realization

 In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.

So in a controller canonical form realization if you have a rate R=k/n convolutional encoder we use k shift registers.

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So the number of shift registers used is equal to number of information sequence that you have and the output is obtained by using n set of adders one for each output sequence.

(Refer Slide Time: 27:02)

Controller Canonical Form Realization

- In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.
- the k input sequences enter the shift registers at the left end of each shift register.

And In this case the k input sequences enter the shift register from the left and side and we take the output from the right and side.

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Controller Canonical Form Realization

- In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.
- the k input sequences enter the shift registers at the left end of each shift register.
- The n adders used to obtain output sequences are external to the shift register.

The next point to remember here is in case of a controller canonical form realization these n adders that are used to obtain the output sequence the coded sequence these adders are external to the shift registers.

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Controller Canonical Form Realization

- In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.
- the k input sequences enter the shift registers at the left end of each shift register.
- The n adders used to obtain output sequences are external to the shift register.

So they are not inside the shift registers.

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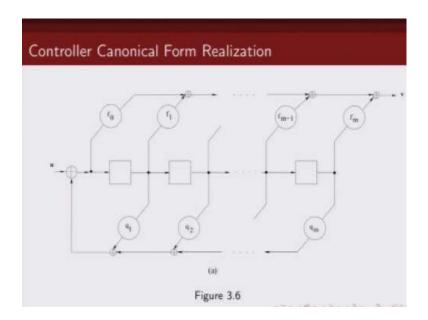
Controller Canonical Form Realization

- In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.
- the k input sequences enter the shift registers at the left end of each shift register.
- The n adders used to obtain output sequences are external to the shift register.
- In Figure 3.6(a) (next page), a rate R = 1, nonsystematic convolutional encoder with following generator function G(D) is implemented in controller canonical form realization.

$$\mathbf{G}(D) = \left[\frac{f_0 + f_1 D + \dots + f_{m-1} D^{m-1} + f_m D^m}{1 + q_1 D + q_2 D^2 + \dots + q_m D^m} \right]$$

So let us take an example for rate one in all systematic convolutional encoder whose generator matrix is given by this, so in the numerator you have $f_0 + f_1D + f_2D^2$ like that similarly denominator you have $1 + q_1 D + q_2 D^2$ like that so how can we implement this using controller canonical form realization so let us go back so we are going to use k shift registers so this is a rate one 1/1 so there will be only one shift register.

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So we use one set of shift register corresponding to one input sequence, next.

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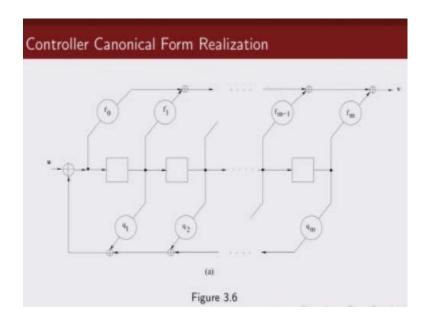
Controller Canonical Form Realization

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We use n set of adders now what is n here? Because is a rate one so n is also one so we will use one set of adders.

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And these set of adders basically this output that we are seeing we have this n set of adders that we are using to obtain this coded sequence v.

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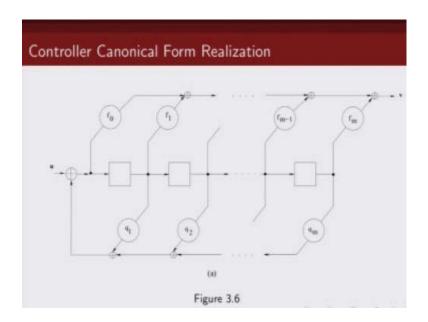
Controller Canonical Form Realization

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Now the key input sequence enter the shift register from the left and side so we can see here.

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The input is entering from distance i, so since this is feedback encoder so let us first look at the numerator term.

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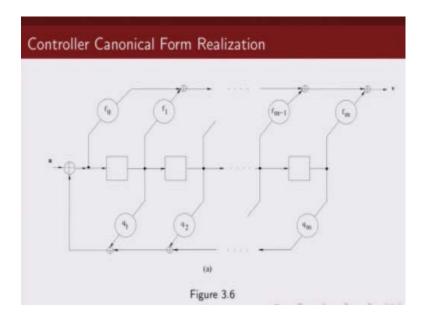
Controller Canonical Form Realization

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What do we have here we have $f_0 + f_1 D + f^2 D$ so this input is basically multiplied by f_0 .

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So the current input is getting multiplied by f_0 then one delayed version of the input is getting multiplied by f_1 two delayed version is multiplied by f_2 so you can see this is an f_0 this is f_1 this is f_2 and again whether there is a connection from this input to the output depending on that f_0 f_1 f_2 will be either one or zero if there is a connection this will be one if there is no connection this will be zero. So you can see this, this is f_0 this is f_1 D, f_2 D² like that basically if this is emit delay element this will be f_m , D_m . Similarly you look go back and look at the denominator.

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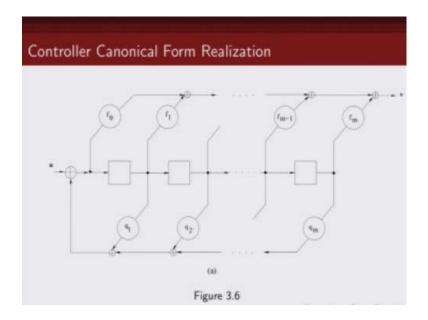
Controller Canonical Form Realization

- In controller canonical form realization, to realize a rate R = k/n convolutional encoder, k shift register are used for input sequences, and n adders are used to form the output sequences.
- the k input sequences enter the shift registers at the left end of each shift register.
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- In Figure 3.6(a) (next page), a rate R = 1, nonsystematic convolutional encoder with following generator function G(D) is implemented in controller canonical form realization.

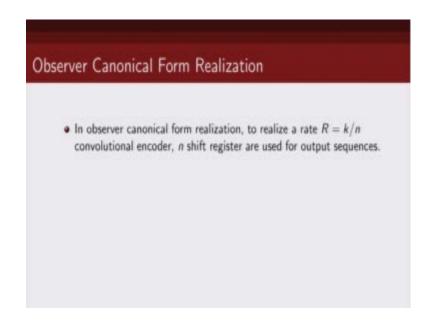
$$\mathbf{G}(D) = \left[\frac{f_0 + f_1 D + \dots + f_{m-1} D^{m-1} + f_m D^m}{1 + q_1 D + q_2 D^2 + \dots + q_m D^m} \right]$$

We have $1+q_1 D + q_2 D^2$ like that.

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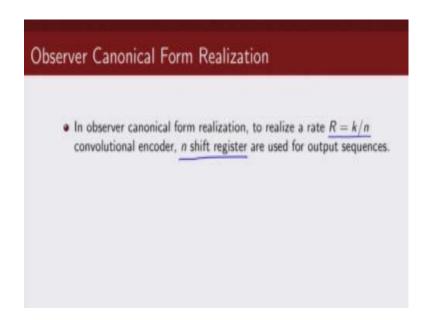


So this the input one this is the D term u_1 D term so this is multiplied by q_1 this is D^2 term multiplied by q_2 like that and then finally you have D_m term which is I am getting multiplied by q_m . So you can see this is how we can realize a convolutional code using controller canonical form realization please note these adders are external to the shift register so there is not adders here internal to shift registers. The inputs are entering on the left and side where the output is taken from right and side.



Now contrast is with observer canonical form realization so now observer canonical form realization we need to realize the rate k/n encoder we require n shift registers.

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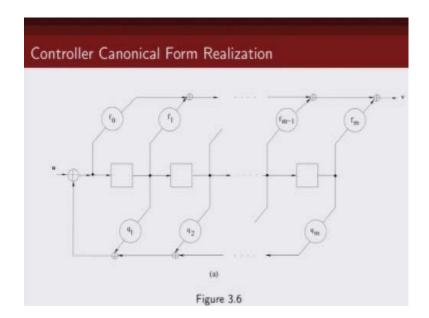
Now please note for the controller canonical form realization we required k set of shift registers whereas in this case we require n set of shift registers one for each of the coded bits.

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Observer Canonical Form Realization

- In observer canonical form realization, to realize a rate R = k/n convolutional encoder, n shift register are used for output sequences.
- The k input sequences enter the adders internal to the shift registers.

The second difference is the key input sequence is in the observer canonical form realization these key sequences enter into the shift register and these adders are internal to the shift register if you recall.



In case of a controller canonical form realization the input is entering here and a t time is still set when your clock comes they move they shift to one location to the right, this will move to here, this will move to here. (Refer Slide Time: 32:11)

Observer Canonical Form Realization

- In observer canonical form realization, to realize a rate R = k/n convolutional encoder, n shift register are used for output sequences.
- The k input sequences enter the adders internal to the shift registers.

Whereas in the observer canonical form realization these inputs are directly entering into the shift register and these adders are internal to the shift register we will give an example to illustrate what we mean.

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Observer Canonical Form Realization

- In observer canonical form realization, to realize a rate R = k/n convolutional encoder, n shift register are used for output sequences.
- The k input sequences enter the adders internal to the shift registers.
- The lowest degree term in the generator polynomial represent the connections to the right hand side of the shift registers.

The lowest degree term generator matrix represent the connection to the right and side of the shift register, in case of controller canonical form realization the lowest degree term was on the left and side here the lowest degree term will be on the right and side.

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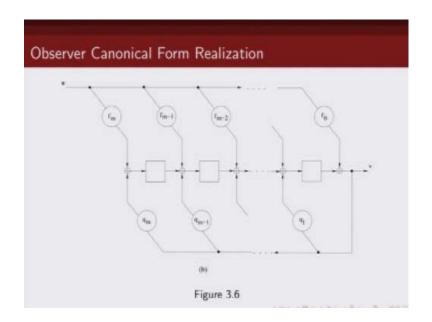
Observer Canonical Form Realization

- In observer canonical form realization, to realize a rate R = k/n convolutional encoder, n shift register are used for output sequences.
- The k input sequences enter the adders internal to the shift registers.
- The lowest degree term in the generator polynomial represent the connections to the right hand side of the shift registers.
- In Figure 3.6(b) (next page), a rate R = 1, nonsystematic convolutional encoder with following generator function G(D) is implemented in observer canonical form realization.

$$\mathbf{G}(D) = \left[\frac{f_0 + f_1 D + \dots + f_{m-1} D^{m-1} + f_m D^m}{1 + q_1 D + q_2 D^2 + \dots + q_m D^m} \right]$$

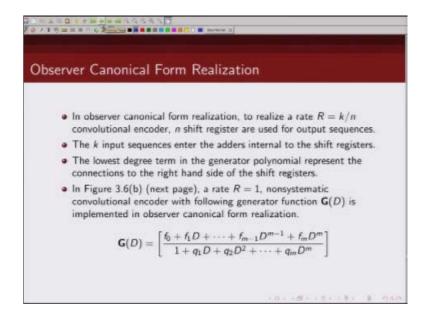
So let us take the same example that we considered earlier so we are considering the same generator matrix and we are going to realize this generator matrix now using observer canonical form realization. So again here k is one n is one so we have n is one so we have one set of shift register this is one set of shift registers.

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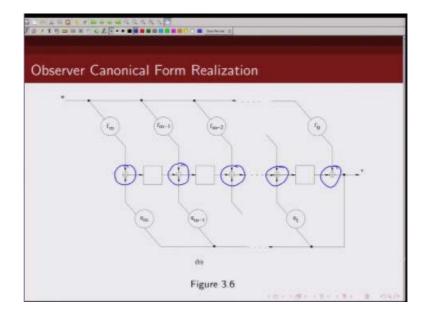
Next what did we say?

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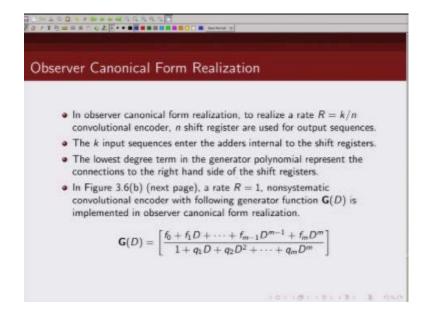
The key input sequence enter the adder internal to the shift register.

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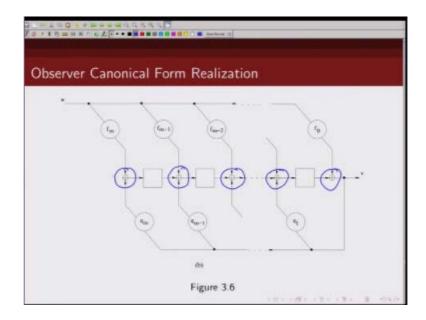
And what do we mean by internal. So these are the shift register elements delay elements, and no more these adders are in between the shift register these adders are internal to the shift registers okay.

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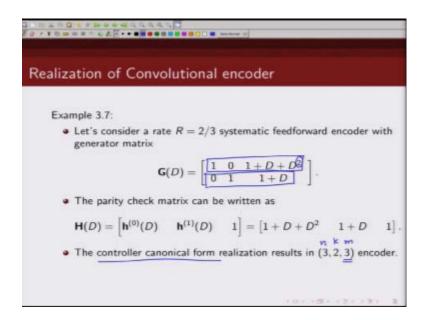
And next thing that we said was a lowest degree term in the generator matrix, represents connection to the right hand side.

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You see here, the inputs are directly coming to the adder. So this term is corresponding to S0 u(d) this term is corresponds to f1 d of u(d). Where as in the controller canonical form the left most term was f0 and the right most was fm. Here, is just opposite, so you can see this is f0 term, f1 term, f2 term and similarly in the denominator you can see this is q_1 , this is q_2 like that this will be q_m . Same generator matrix can be realized using two different forms.

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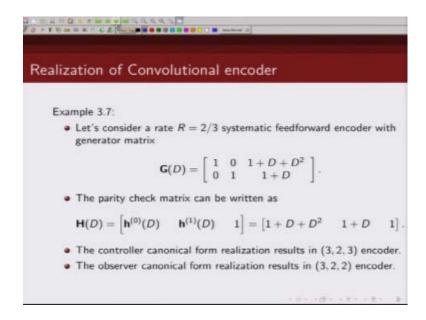


So let us take an example to illustrate this, so we are considering our rate 2/3 systematic feed forward encoder who generator matrix is given by this. Now let us try to realize this generator matrix using controller canonical form realization and observer form realization. So the parity check matrix for this is given by this expression we will just show you that so in controller canonical form realization we have so there are two inputs here so we will have one set of shift register for each of the input.

So we will have one set of shift register for this and one set of shift register for this. And to realize this we need two memory elements because here the highest degree of D is 2. And to realize this we required one memory element.

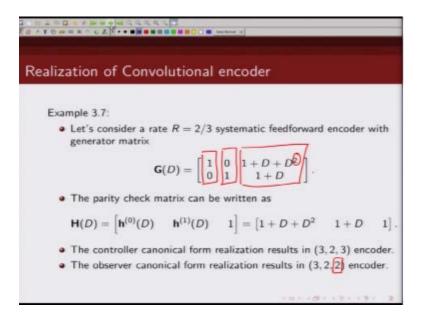
So total we will require three memory element so that is what I said for the controller canonical form realization for this rate two third this is my n, this is k, and this is the memory order. We basically require three memory elements to represent this convolutional encoder in the controller canonical form realization.

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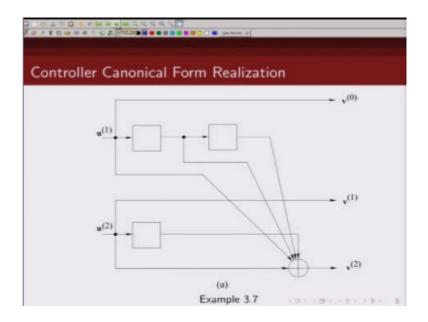
Now what about observer canonical form realization in observer canonical form realization we use wise set of shift register for each of the end coded bits.

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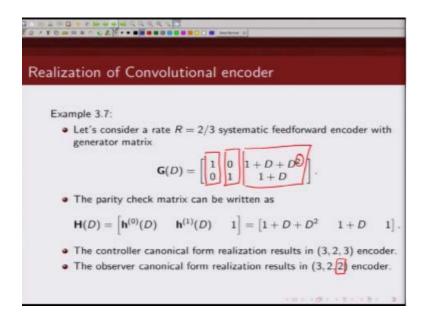


So how many coded bits we have, we have three, one is this, one is this and one is this. Now how many memory elements you required to represent this 0 is directly the input coming in here. Here, 0 because the direct input is coming here, and what about this its maximum degree is 2 so we will require 2. So over all for this generator matrix if we try to realize it using observer canonical form realization, we require only two memory elements. And in the next slide I am going to show you those two encoder realization.

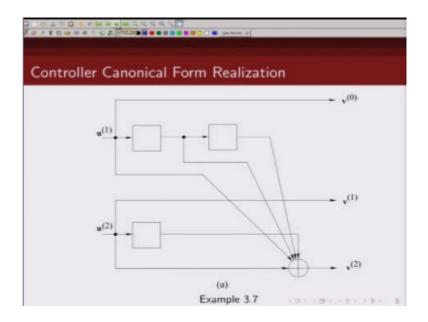
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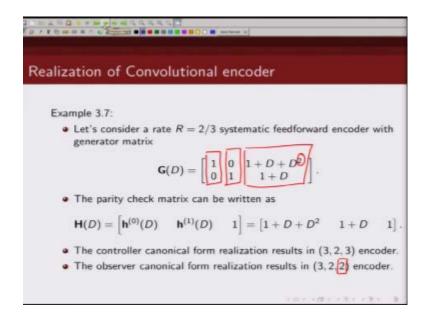


So let me just write down the generator matrix.

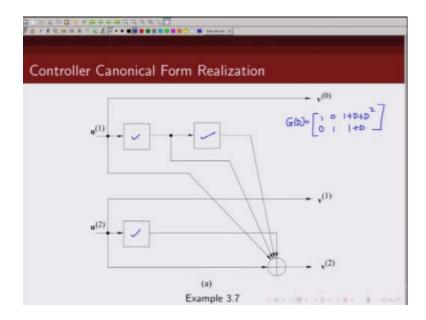


So my generator matrix G(D) is 1001.

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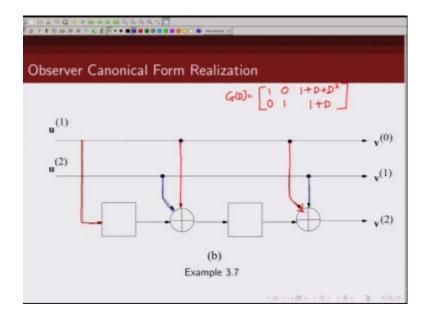


Then do we have $1+D+D^2$.



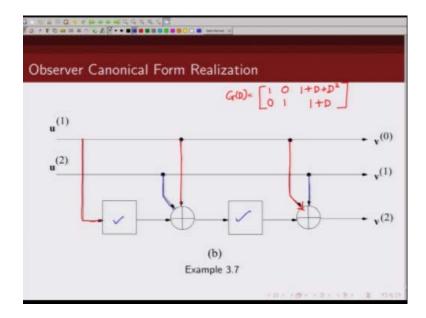
 $1+D+D^2$, 1+D. so one set of shift register for this, so this maximum degree is of this is 2 so we use two memory elements and for this maximum degree of D is 1 so we use one memory element okay. Now what is the first output first output is directly input $u^{(1)}$ so this is my $u^{(1)}$ second output is directly $u^{(2)}$ this is basically this and the third output is $1+D+D^2$ of $u^{(1)}$ so this is u, this is the D of u D, $u^{(1)}$ D and this is $u^{(1)}$ D plus $u^{(1)}$ D plus $u^{(1)}$ D meaning one term is $u^{(2)}$ and second is delayed version of $u^{(2)}$. So this will be my third coded bit. So you can see to realize this generator matrix, we required total three memory elements one, two and three.

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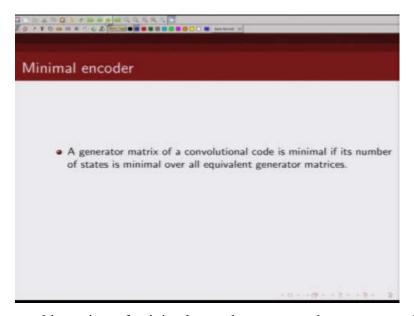
Now let us see for the observer canonical form realization, again let me write down my generator matrix this is 1001, $1+D+D^2$, 1+D. So we said one set of rows, one set of shift register for each of the coded bit for each column there is one set of shift register what some maximum delay element here 0 so you can see directly. What about this again there maximum degree of D is basically 0 so this no shift register. And here for the third line D is 2 so we took 2D. So what is the final output then first one is first, first coded bit is just $u^{(1)}$ of D that is what it is.

Second coded bit is $u^{(2)}$ of D straight this and third coded bit is $1+D+D^2$ of $u^{(1)}$ of D. So what is $u^{(1)}$ of D, $u^{(1)}$ of D is this one. What is D times $u^{(1)}$ of D that is this term, and what is D^2 $u^{(1)}$ of D that is this term. Find plus 1+D times $u^{(2)}$ of D. So then what we have is $u^{(2)}$ of D is this and D times $u^{(2)}$ of D is this. So this is our observer canonical form realization for this convolutional encoder with this generator matrix and note.



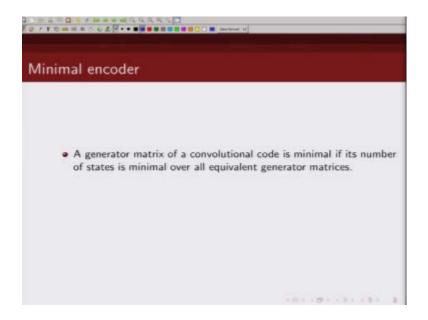
We only required 2, 1, 2 we required only two memory elements. So same encoder here require two memory elements for the controller canonical form realization we required three memory elements.

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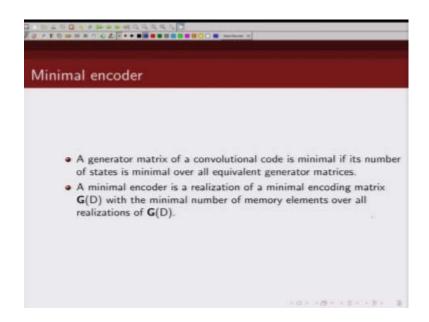
So that brings us to this notion of minimal encoder we saw the same encode convolutional encoder with same generator matrix can be realized using two different ways one that resulted in three memory elements other that resulted in two memory elements.

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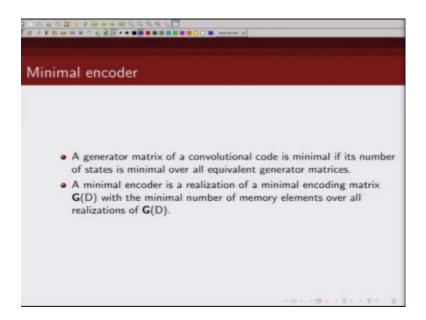
So we say a generator matrix is minimal if the, if its number of states is minimal over all possible equivalent generator matrix.

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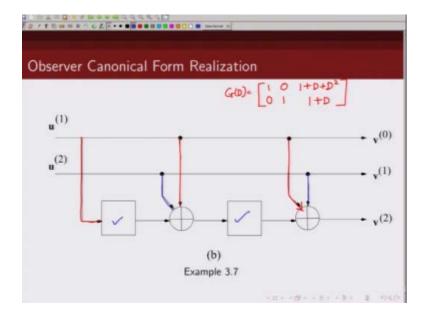
And among the minimal encoder matrix are minimal encoder is basically our realization of a minimal encoding matrix which will result in minimum number of memory elements use to represent that, that particular convolutional encoder. So we define a minimal encoder as.

(Refer Slide Time: 42:21)



The minimal realization of a minimal encoding matrix, so the minimal encoder should result in minimum number of memory elements used to represent that particular convolutional encoder.

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And for the example that we have considered this in this case you can see from the generator matrix the maximum degree of these two so we atleast made two memory elements to represent it and you can see the observer can undergo form realization in this particular example we will result in minimal encoder on this convolutional encoder. So this realization will result in minimal encoder realization for this convolutional encoder. Thank you.

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Tapobrata Das

Ram Chandra

Dilip Tripathi

Manoj Shrivastava

Padam Shukla

Sanjay Mishra

Shubham Rawat

Shikha Gupta

K. K. Mishra

Aradhana Singh

Sweta

Ashutosh Gairola

Dilip Katiyar

Sharwan

Hari Ram

Bhadra Rao

Puneet Kumar Bajpai

Lalty Dutta

Ajay Kanaujia

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