Principles of Modern CDMA/MIMO/OFDM Wireless Communications

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Lecture – 28
Code Generation for CDMA

Welcome to another module in this Massive Open Online Course on the Principles of CDMA, MIMO, and OFDM Wireless Communication Systems. In this module, let us look at another aspect of a CDMA system that is Code Generation. How to generate the codes that are used in the CDMA system? Let us look at the code generation of a CDMA system. Now, if we look at a typical code in the CDMA system.

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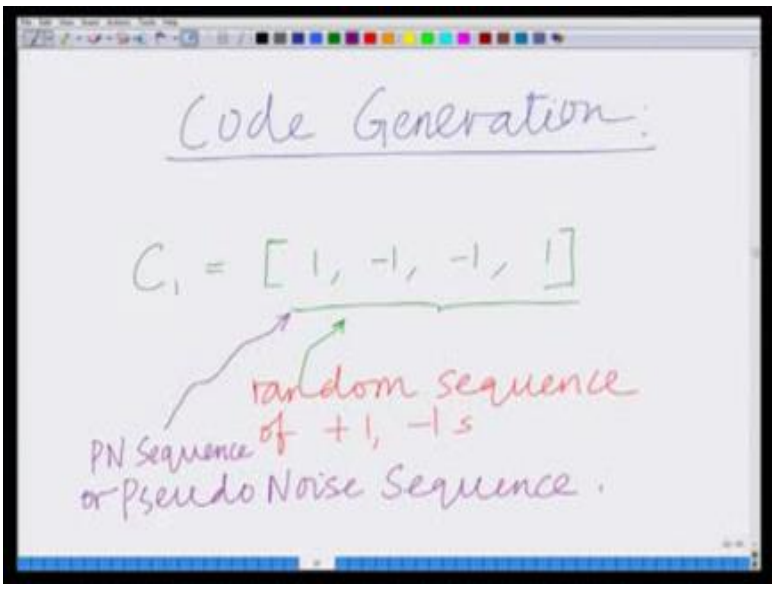

Let us look C_1 which is 1, - 1, - 1, 1. If you look at this, this looks like a random sequence of 1, - 1, which looks as if it is a sequence in which 1, - 1 symbol, have been randomly generated, such a sequence is known as a Pseudo Noise Sequence. It has it behaves as if a noise sequence of 1 and - 1s, this known as a Pseudo Noise Sequence. Because it is not actually a noise sequence but it resembles a noise sequence.

Therefore, this is known as a Pseudo Noise Sequence. This is known as or basically your such a sequence is known as a PN Sequence or a Pseudo Noise Sequence and therefore, the codes are generated in a CDMA system as PN Sequence or a Pseudo Noise Sequence

and how do we generate such PN Sequences. This is by using a mechanism or a structure known as a Linear Feedback Shift Register.

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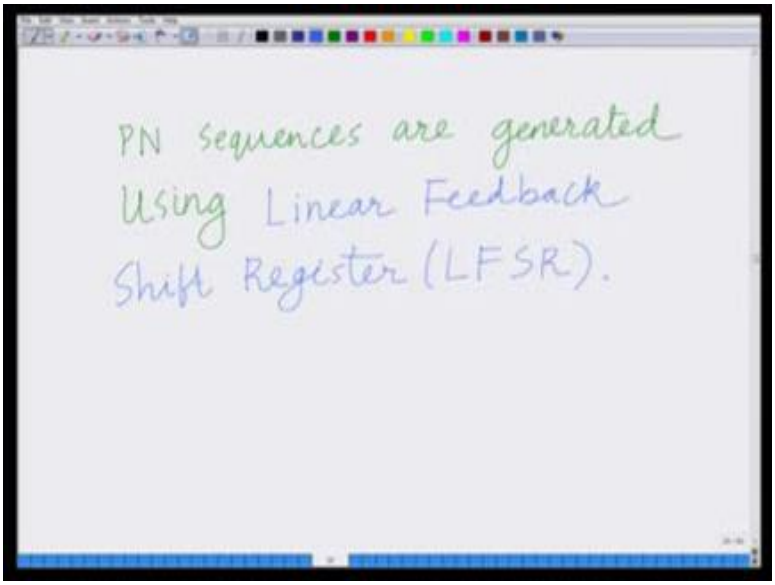

PN Sequences for CDMA system, are generated using what is known as a Linear Feedback Shift Register also termed as LFSR.

So, PN Sequences for CDMA systems are generated using the Linear Feedback Shift Register mechanism. This shift register, you might have studied in your digital circuits; which basically store and advanced data in a digital circuit or binary data. And this linear feedback the shift register mechanism with feedback which is also termed as Linear Feedback Shift Register is used to the generate the PN Sequences and this can be described, a simple example can be described as follows.

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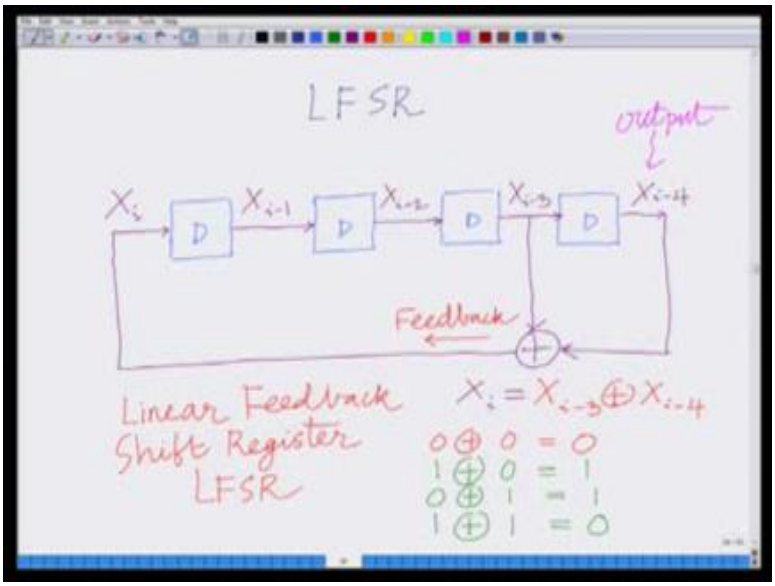

For instance, let us take a look at this LFSR, Linear Feedback Shift Register circuit with 4 registers, I have a shift register, I have a delay register, I have 4 delay registers and there is a feedback mechanism in this correct.

Let us say, the input is x_i after the first register, I have the delayed version that is x_{i-1}. After the second register I have the delayed version of x_{i-1}, that is x_{i-2}, the third register I have x_{i-3} and after the 4th register I have x_{i-4} correct. And now I am taking x_{i-3} and x_{i-4} performing the xor operation and then I am feeding this back as input to the register. I have x_i which is equal to $x_{i-3} \oplus x_{i-4}$ and this is being fed as, this is the feedback path. Therefore, what I have is, I have shift registers in this and there is a linear operation that is being performed which is the xor operation.

And there is a feedback mechanism that is I am feeding back $x_{i-3} \oplus x_{i-4}$ as x_i. So, this x_i is being fed back as the input. So, there is a feedback mechanism in the circuit. Therefore, this is known as a Linear Feedback Shift Registers circuit. Hence this is known as a Linear Feedback Shift Register or LFSR circuit. Because it is linear the xor of operation is a linear operation. There is a feedback mechanism, that is output is being fed back to the input and also this circuit involves shift registers. Therefore, this circuit is

known as a Linear Feedback Shift Register circuit. And you must be familiar with the xor operation; the xor operation takes 2 binary variables as input for instance

$0 \oplus 0$ equals 0.

$1 \oplus 0$ equals 1.

$0 \oplus 1$ equals 1.

$1 \oplus 1$ equals 0.

This is the basic $1 \oplus 1$ equals 0. This is the basic operation or basic principle of the xor operation.

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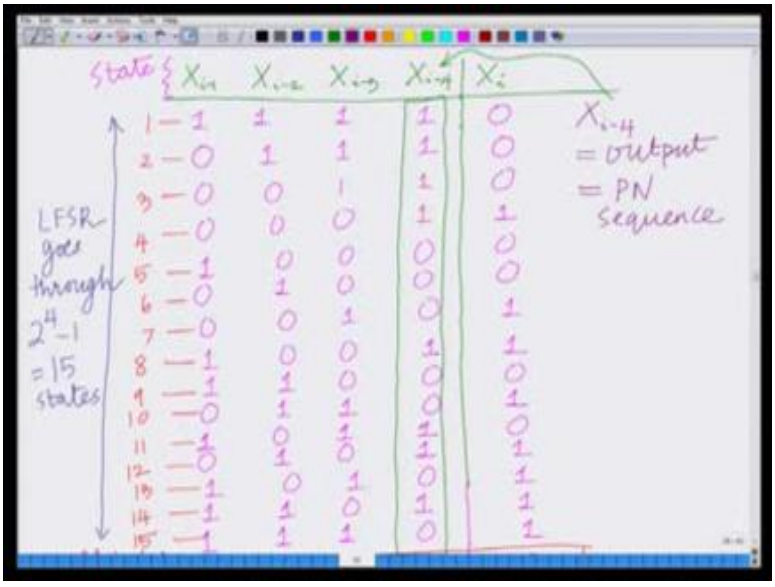

Now, let us look at the operation of this Linear Feedback Shift Register circuit. Let us look at the variables $x_{i-1}, x_{i-2}, x_{i-3}\ x_{i-4}$ and let us look at the corresponding generation of x_i at each time instant. Let us look at x_i; now let us start with I can term this x_i as $x_{i-1}, x_{i-2}, x_{i-3}\ x_{i-4}$ as the state of the system. $x_{i-1}, x_{i-2}, x_{i-3}$

x_{i-4} can be collectively termed as the state of the system. So, these I am going to call these as the state of the system.

Further, if you look at this circuit x_{i-4} is the output of the system. Now, let us consider this system starting in the all 1 state. That is $x_{i-1}, x_{i-2}, x_{i-3}\ x_{i-4}$; all of them are equal to 1. Now if all of them are equal to 1, x_i = x_{i-3} xor x_{i-4} is equal to $1 \oplus 1$ which is basically equal to 0 therefore, x_i will be 0. Now in the next time instant, remember x_i is being fed to the delay element. In the next time instant x_i will become x_{i-1}, x_{i-1} will become x_{i-2}, x_{i-2} will become x_{i-3}, x_{i-3} will become x_{i-4}. And therefore, what will happen is the state will become x_i, x_i will become x_{i-1}. So, x_{i-1} will be 0, x_{i-2}, x_{i-1} will become x_{i-2} that is 1 x_{i-2} will become x_{i-3}. That is 1 x_{i-3} will become x_{i-4} that is 1 and now the new x_i is x_{i-3}, xor with x_{i-4} which is again equal to 0.

And, now proceeding in this fashion, you can fill the rest of the sequence. The rest of the sequence will go as follows 0 0 1 1 and the output will be 0. The next state will be 0 0 0 1 and the output will be 1. The next state will be now 1 0 0 0 and the next x_i will be the 0 the next state will be 0 1 0 0 and the next x_i will be 0 and the next state will be 0 0 1 0 and the output will be $x_{i-3} \oplus x_{i-4}$, x_{i-3} is 1, x_{i-4} is 0. So, x_i is 1, xor 0 which is 1 and now x_i will become x_{-1i}in the next state. The next state will be 1 0 0 1 and the output is 1. Then you have 1 1 0 0 output is 0; then you have 0 1 1 0 output is 1 or x_i is 1 then you have 1 0 1 1 x_i is 0, then you have 0 1 0 1 x_i is 1 then you have then you have 1 0 1 0 x_i is 1.

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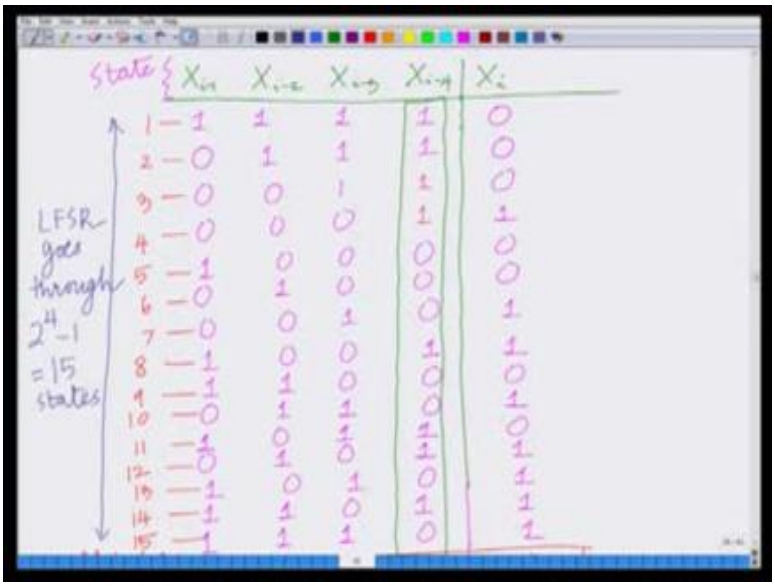

From this table that I have drawn, you have 1 1 0 1 x_i is 1 and then you have correspondingly you have 1 1 1 0, x_i is 1 and after this stage what you will have is that the next stage will be 1 1 1 1 and the corresponding x_i will be 0. And at this point now, you can see that we have come back to the all 1 stage that is 1 1 1 1 and here from this stage onwards the sequence will repeat itself from this stage onwards the sequence will after this stage you can see the all 1 state. So, the sequence repeats itself.

And therefore, what we have is we have generated we have gone through let us count the number of states; that we have gone through 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15. We have gone through at total of 15 states. What we have is, we have gone through a total of basically 15 states before we come back before we come back to the all 1 state and after this all 1 state the output repeats itself. After this the output repeats itself and now if you can look at the output, we said x_{i-4} is the output of the system. This column here is the output sequence of this system, which is the PN Sequence. Let us write this column which is the output.

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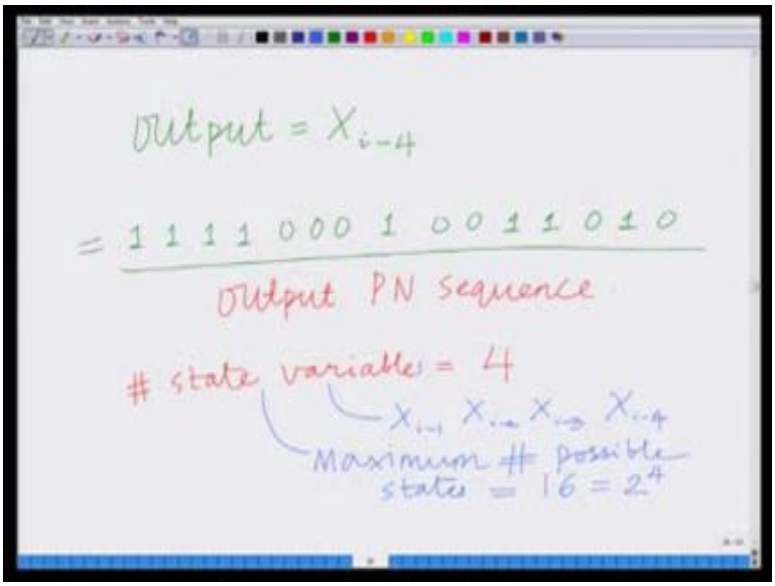

So, the output equals x_{i-4} which is basically equal to 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0. So, this is the output sequence. This is the output PN Sequence of this Linear Feedback Shift Register mechanism. And what we have seeing is that this LFSR Linear Feedback Shift Register is going through 15 states, 15 states none of which are identical. It is going through 15 states. Now you can see the number of state variables equal to 4. The state variables are basically $x_{i-1}, x_{i-2}, x_{i-3}\ x_{i-4}$. And we have 4 state variables each of which can take 0 or 1. Number of maximum number of possible states is equal to 16. That is equal to 2^4.

However, if you look at this for the Linear Feedback Shift Register, you can see that the Linear Feedback Shift Register goes through 15 states. That is 16 - 1. So, it goes back through $2^4 - 1$ state. So, the LFSR the Linear Feedback Shift Register goes through $2^4 - 1$ equals 15. So, you can see there is 1 state that is out of 16 it goes through 15 states there is 1 state through which it does not go through that is all 0 state. So, the Linear Feedback Shift Register goes through all the 15 states out of the 16 states it goes to the it goes through all the 15 states, but does not go through the all 0 states.

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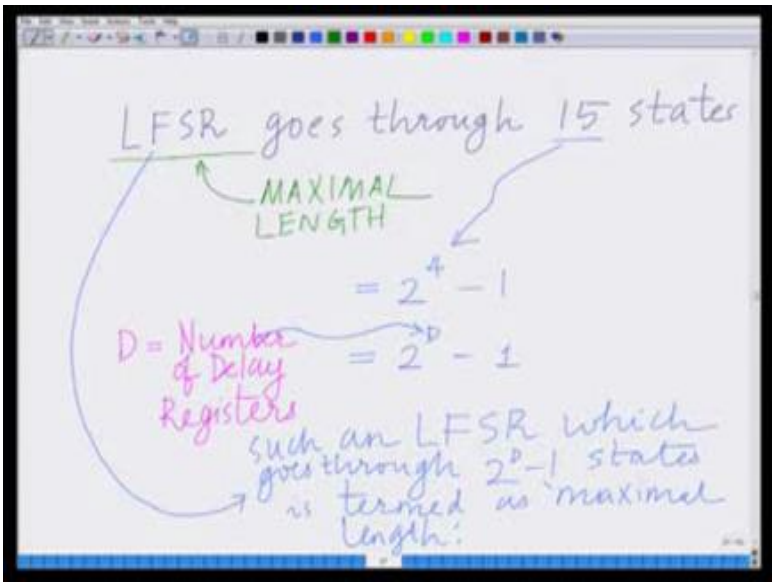

If the LFSR, the Linear Feedback Shift Register goes through 15 states. Which is equal to $2^4 - 1$ which is basically equal to $2^D - 1$, where this D equals the number of delay registers? The number of delay register is 4; total number of states is $2^4 - 1$ that is 16. The Linear Feedback Shift Register goes through $2^4 - 1$, that is 15 that is 16 - 1; that is 15 state and such a feedback shift register architecture which goes through all the possible states except 1 state before coming back to the original state is known as a maximal length Linear Feedback Shift Register.

Such a Linear Feedback Shift Register such an LFSR which goes through $2^D - 1$ state is termed as the maximal length Linear Feedback Shift Register. What we have seen this Linear Feedback Shift Register circuit which is going through all the possible states; except the all 0 state and if you look at the output generated by this Linear Feedback Shift Register that output forms the PN Sequence.

Therefore, if you look at the output the output is x_{i-4} remember we said x_{i-4} equals the output of the Linear Feedback Shift Register. This output sequence forms the PN Sequence. So, this output equals the PN Sequence or the Pseudo Noise Sequence which is used as a code in the CDMA system and this output sequence.

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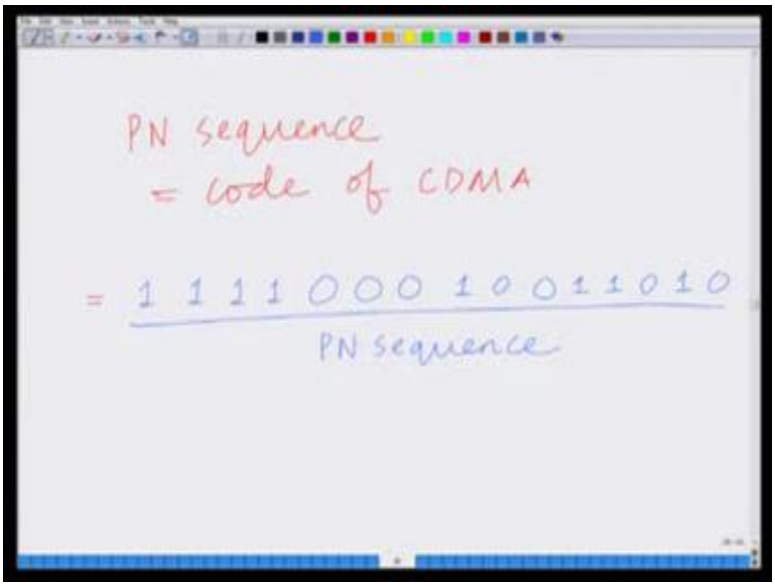

Let us write this PN Sequence again corresponding to this LFSR circuit. So, the PN Sequence; which is also equal to the code of the CDMA system is given as basically 1 1 1 1 0 0 0 1 0 0 1 1 0 1. So, this is also given as 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 and this is basically your PN Sequence which can be used as a code in the CDMA systems.

So, this is how codes are generated for a CDMA system. They are generated as PN Sequences or Pseudo Noise Sequences. This Pseudo Noise Sequences are generated as the output of a Linear Feedback Shift Register circuit. It has shift registers it performs a linear operations and it involves feedbacks and we have seen an example operation of the Linear Feedback Shift Register circuit for D = 4 shift registers and we have said that this circuit goes through all the possible state except the all 0 states.

So, it goes through $2^D - 1$ that is $2^4 - 1 = 15$ states. And therefore, this is known as the maximal length Linear Feedback Shift Register circuit. And we have also seen the corresponding PN Sequence which is the output of this Linear Feedback Shift Register circuit. This explains the concept of code generation for the CDMA system.

So, we will stop this module here and we will look at the properties of the PN Sequences in the next module.

Thank you very much.