Digital Switching
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Lecture – 29

We forward from where we left last time and such there is a midsem break. So, I will not be taking up anything new; we will be just finishing analysis when t select is 0, okay, and we will just understand that. So, basically today we will be devoting our time for adding define transition matrices; rest all methods actually remain the same. And you will now also basically appreciate the difference between the two mechanisms, and of course, it is possible to analyze the midway mechanisms. For example, when t select is 50 percent and t pass is also 50 percent of t delay; that kind of analysis is also possible.

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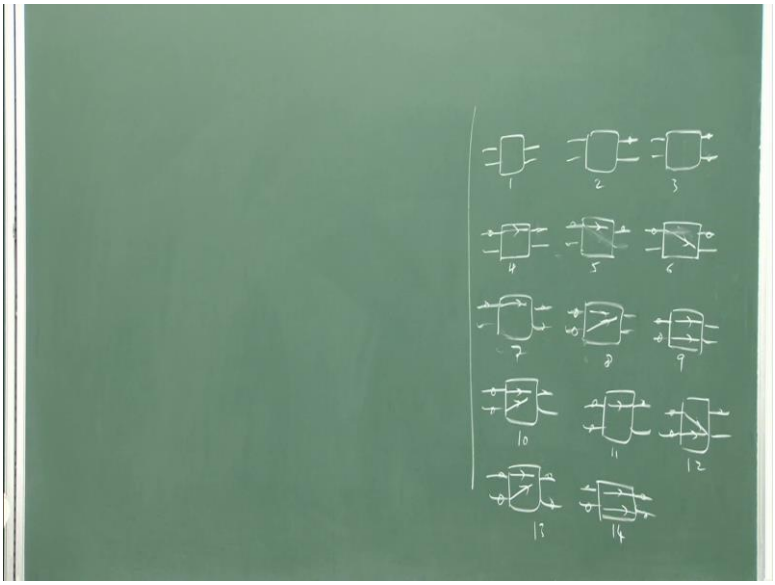

So, I think again we require those fourteen sets. So, should I write it? Maybe for the people who are recording will be actually reviewing it later on. So, this needs to be done. So, these are those fourteen states.

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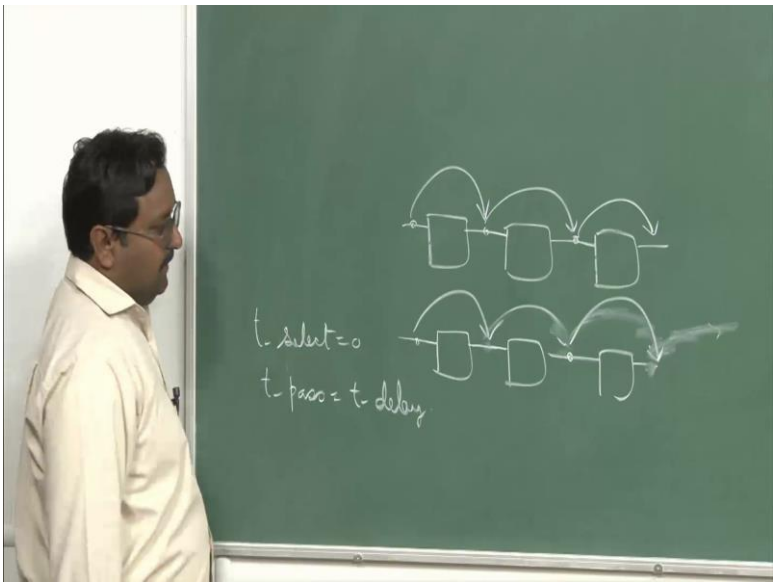

So, now when t select I have already given an example whereby if you do a cascading for example, of a switch; earlier case if all of them, for example, have this packet, and this is the last stage or whatever it is. So, they will just be deciding in the whole t delay slot which will be happening parallely for all the three that where the packet has to go. Once that is done, this packet will be read out almost instantaneously, and within the same instant, this packet will also be read out; this packet will also be read out, okay. But once it is come here, again it has to decide way, on which port it has to go; that is why it cannot jump, but all three packets can jump together, okay.

So, usually that is why the t select there were actually three phases. One is the packet going out, then packet jumping, and then packet coming in were actually were kept separately for a one particular switch, because things were happening simultaneously when the packets are being transitioning continuously, okay, so that you can do that computation. Now for our case now when t select is going to be 0 and t pass is finite. So, remember packet can move even if the outgoing buffer is busy; it is occupied, then also packet can move subject to condition that is also moving out.

So, that is why you are first of all finding out whether this will move out or not, and based on that, whether this will come here or not; if this comes here, then some other packet commit higher or not. So, there were three steps involved, and those are being iterated in one time slot in the backward direction. So, all three transactions can happen,

but now the case which we are looking is if this is the situation, they will immediately select where it has to go. Now this packet cannot move here unless this buffer is empty, because this whole writing itself take t delay, and this packet cannot go instantaneously out; this also will require same amount of delay and unless this is free this cannot start.

So, first time slot, this will move, and you will get a packet not here; after one time slot t delay, you will be in this situation. Next time slot, only this packet will move here, and this packet will be read out. This will be happening parallely. So, there is a gap hole which gets created between the two, okay, and this packet cannot break, because this buffer is not empty. So, after some time when this packet will be here, this packet will be read out this packet. So, in next time slot third time slot, then this will be transferred here, and this will be transferred here.

So, that is the difference which comes when t select is 0 and t pass is nothing but t delay. So, we expect the performance to be poorer in case when t select is 0, okay. Now important thing I do not require those three steps; one, two, three, and three will become 0 for the next time step; that is not required. I can only do with one single step. So, that is what we are going to do actually here.

Student: Sir it is zero, to make the calculation simple or some other reason?

Where?

Student: You have chosen in two cases t select zero.

Ideally, it is right; none of them will be 0.

They have to be finite; they have to be some intermediate value, but these are the two extreme situation of the performance. These are two extreme situations. So, these can be analyzed simply in computational procedure for doing; for example, 50-50, it is going to be slightly tricky. It is not that easy, okay, because writing into memory and reading from a memory cannot happen simultaneously older people. Older packet cannot be read out while a new packet is being written, and that is not possible.

And they do not have a dual buffer system the way we had in switches. See while you are reading in a slot from one memory, you can write in the same time slot in some other memory, then you switchover the memory. That option is not implemented here. If you

can implement that option, then of course scenario will be very different; that is technically what when I am saying t pass is 0; that is what we are indicating actually. We are having a dual buffer system technically.

So, once we have decided I have within t select period or t delay period where the packet has to go, after that it does not matter. So, writing out of the packet to the outgoing buffer will not interfere with the writing in of the packet, and that can happen with dual buffer system, okay, but notionally, there is only, yes, one single buffer at per out input port with this condition. So, now the changes which will happen is you will have p j which will be defined as it is p j tilde will be as it is. P j bar will be as it is. P j tilde was the packet will go out of your outgoing port; p j is that packet is present at a port, okay, and p j bar is packet is going to come into your incoming port incoming buffer. So, these definitions remain intact.

In fact, even those whatever we had the states we had defined the state probabilities; those will also remain the same. Now only thing which will happen is this will be the only thing which will be available. We will be only working with this, because p 1 will not be there; there is no step 1. Step 1 actually technically gets merged, okay. So, only problem which is there that p 1 calculation which you had; sorry p j, there is no p 1. So, p j tilde p j bar and p j, there were three calculations, and they require probabilities after step one; probabilities after step one actually, remember p 1 we were always writing. So, what will be the state probability of either j minus first stage or j th plus first stage or j th stage; there were three actually configurations.

In that case, all p ones will be simply replaced by p 0, because there is no conflicts. So, I am not actually having three steps. So, probability that after step after a time slot t, my packet will be going out will be decided by p j tilde where the probabilities here. Those expressions will still remain exactly same; they would not change. They will come from there. So, if you wish, I can reiterate or you can just simply replace; both ways it is fine. So, maybe for p j tilde, we can do this, okay. So, p j tilde that probability that packet will go out, okay, n time slot tau k which starts from t k to t k plus 1.

So, at t k this is the probability that conditional probability that packet will go out. So, denominator you have to put all those states where you will have packet at the input. So, there will not be one anymore p is 0 which will be coming. So, when the packet is there

at the input port or the outgoing ports, sorry. So, it is half of p 0; that is the only change which will happen, p to j that is the variation which will come. I think earlier case it was, no, no, I think everything will remain still the same.

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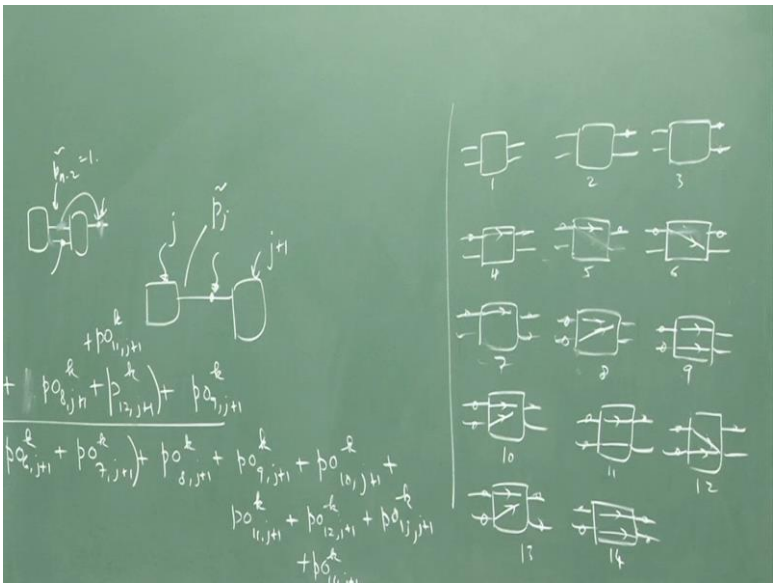

Except I have to look at j plus first stage, I have to look at all the states where the packet is there at the input, okay, j plus first, and then I have all those states will be put in denominator. In the numerator I will put all those states where the packet will actually move out from here to here. So, that will give the conditional probability of packet going out from here. Only thing it will become p 0 instead of p 1 which was there earlier, not two it will be actually four first.

So, I am just putting a bracket for all half. So, I will just add here, okay. Five, this will be six, seven and then remaining ones actually will come p 0 8 j plus 1 p 0 9. So, this is what will be the denominator. Now this identifies the probability that a packet will go out, okay. So, I think because time slots have to be clearly specified; this is at this particular time step just before, this is you are in probability of in this state just before this particular step starts and this particular time slot starts. This is after step 0 in k minus 1 I think; that is the only variation which will come, okay, and then you find out all states where the packet will be moving out in this time slot t.

So, this is nothing but p j tilde is the probability that at the end of this time slot, packet will go out; condition on if the packet is present at this point. So, I think this is the only

thing which we have to define clearly, because earlier case, this was not the issue, because all the packets all three packets can jump together, here they cannot. So, there is a minor variation in the definition here that is not explicitly stated. So, this will basically depend on this is a probability that packet will be going out of your outgoing port or outgoing output buffer conditioned on the packet was available at the beginning of the time slot.

And packet will be going out after the time slot, or it will be actually moved out by that time; it will not be there. So, this p j tilde is that probability. So, this is the condition on that packet is present here, and packet will be moved in moved out by this time. So, what is the probability that packet would have moved out by the end of the slot? Condition that packet was there in the beginning of the slot. So, this gives the probability that packet was there in the beginning of the time slot, and I am now choosing in the numerator only those states for which in this time slot, packet will actually move out; look at only those conditions.

So, those will correspond to; for example, four? Yes, packet will actually move out surely. So, you can put p 0 4 j plus 1 k. Five, it will not be moving out; six, it will be moving out; eight will be moving out similarly.

Student: Moving out from which port sir?

Hmm?

Student: Moving out from input port sir?

Output port of j th stage and input port of j plus first stage; I am talking about j plus first stage here.

Student: This corresponds to input port of j plus first?

See because your probability that the packet from your output is going out will depend on the.

Student: Yes, because this is the input port of j plus 1.

Input port of j plus 1, right. So, this is the j, and I am trying to estimate p j tilde.

This will be exactly same expression I think, because in principle we had followed the same thing. Then p 12 will be coming; that is it, and for eleven I think I have missed out something. Eleven will also come, right; both will go in nine. So, I am writing nine, but this is only which is with half actually; the full ones now we will write. Use the same expression. So, full only happens for nine I think nothing else; rest all is half. It must be same expression. So, in principle it is also true for p j bar and p j same way. P j will give you the probability that packet is there at your outgoing port.

So, look at j th stage, find out in j th stage the switch will be in which particular state, and sum up all those probabilities. These are absolute probabilities; I am coming to that. You have to understand p n minus 2 tilde is 1.0 in the earlier case. Now p j n minus 2 tilde is not 1.0; it is going to be less than that, okay. And that will cause the impact because now we are doing backward propagation. Ultimately, that probability what gives you the throughput; throughput will be lower in this case intuitively. Now the condition here is not this will be 1.0. It is not p n minus 2; it is p n minus 1 tilde. There at the output, packet was instantaneously taken out n minus 1 stage.

So, at n minus 2 output if there were two packets, both of them will also be taken out immediately, because there was a instantaneous read out, but here it is not instantaneous. So, reason for this will be now even if this is the last stage, you have a packet here pushed out. This will not be read out immediately; it takes one full slot to read out. Earlier it was instantaneous. So, only if the packet here, it will be read out. So, if there are two packets sitting here for example; in earlier case, both of them will be even if they are going to the same port, they will be taken out and read out instantaneously. We kept this thing as t of n minus 2 tilde as 1.

Now it is not possible. When this will go out, it will become empty; only one of them will go. Other one will still be hooked up here; earlier case even this was going out. So, this has hidden impact. So, intuitively, yes, the performance has to be lower than the earlier case. So, now coming to the state transition table, we will not be having state transition table after step 1, step 2 or step 3; those are not there. We have only step 0, only one step every time slot. So, in that step only all transition can happen.

Now only change which we will have; we will still have three transition tables. One for the input stage first stage of the switch, one for the output stage, because input stage p j

bar is going to be or p 0 bar which is always 1.0. The weight was there even in the earlier switch, and the output stage p n minus 2 or p n minus 1 tilde is going to be 1; in between your state transition depends on the incoming rate and outgoing rates both, because there it is not broken into three steps.

So, we have to use the compound formation basically. Transition will be simpler; matrix will be simpler in this case, it is not complicated. So, I think in same way, we can build up for p j bar and p j. So, I need not probably do that and that can be written by you. If you wish, I can write down the expression directly or earlier expressions which we had; we had simply replaced all p ones by p zero. All ones will be replaced by zero; that is it, rest everything is same.

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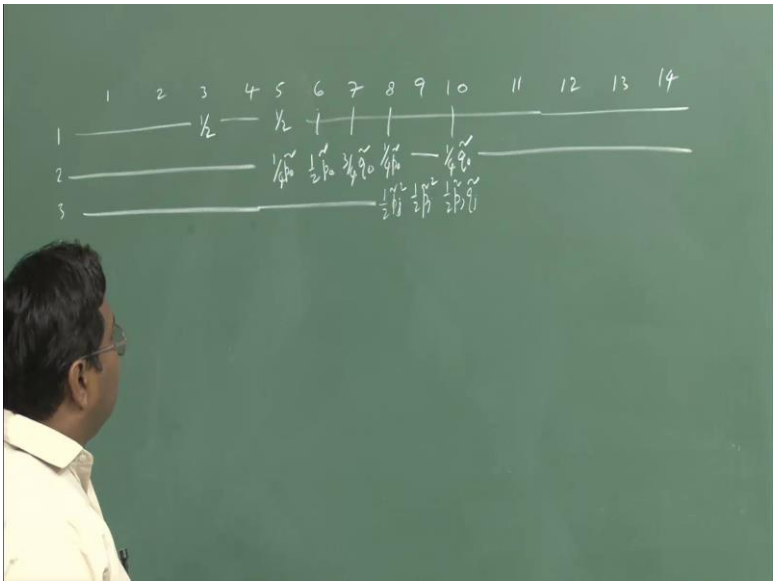

So, first is state transition matrix because. So, we had already three transition matrix done earlier. So, this will be identified at superscript four, but this is for t select is equal to 0 is for this case. So, now you have the states and then now we can build up with this, and you have to remember that your p 0 bar is 1, okay. So, look at your state 1. In state 1, what will happen where you will go? P 0 bar is 1 remember. So, packets have to arrive. If both packets will arrive, they will be going where? You will either come to a state eight or nine; there is no other possibility, and no, eight or nine not. See, I am looking at a transition from this time slot to this time slot what happens at after this time slot.

I am not looking into zero one two three steps. I am looking at after the complete step. So, at this point, suppose you are in the state 1, both packets will arrive. So, both packet out of these t select is 0, immediately a decision will be made where the packets have to go if both of them are directed to the one outgoing port. So, one will be at the input and one will be at the output. So, that state will be your 5 state, okay. If there is no conflict between them, both of them will be on the outgoing port; that state will be three. They cannot move to the output of the next stage, because it is not possible. One time slot only one read out is possible; again there is a buffer.

So, next read out will take another time slot; that will happen in the next one, okay. So, this actually means you will have half here and half here, okay. Now look at the state two. If your input switch is in state two, both packets will come. They will select; immediately selection will be done where they have to go. They both might would like to go to the same port where the half packet is already there at the output. They both may like to go to the free one or they can do a crisscross. So, based on that, you will find that and you have to also look at what will happen in after the step 0, whether this packet will go out or not go out. See outgoing packet also has to go out; this particular switch packet which is there in this state.

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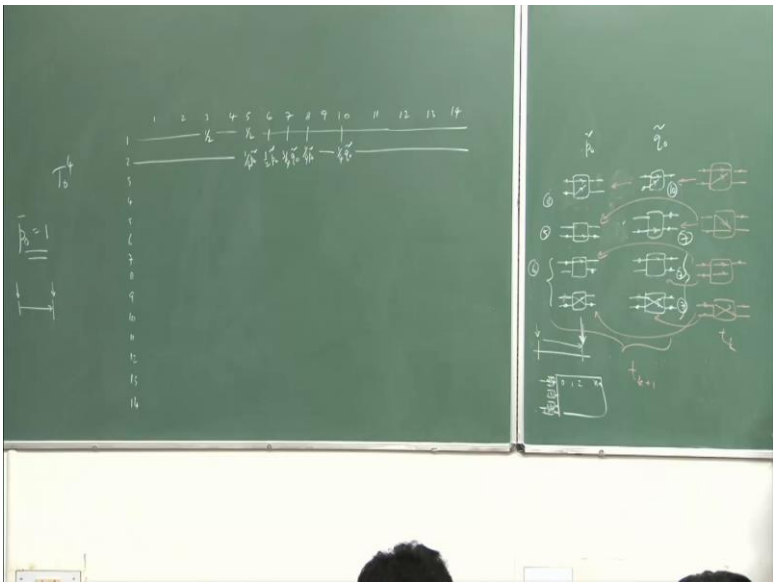

Important thing now; even if it is being read out by the next one, you cannot write anyone of these two packets in this slot; read and write cannot happen simultaneously.

So, these two packets cannot move here; that is not possible. This can be read out or may not be read out; both are viable. So, with probability or p 0 tilde, this will be going out, and with q 0 tilde, this will not be going out, okay. Now these two packets if you look, they just come; they can be directed with equal probability to anyone of these ports. So, now I have to look at iterate on the cases actually.

So, let me write all cases one by one, enumerate them and then estimate the probability. So, first case is when the packet actually moves goes out. So, I have p 0 tilde with this; this will be happening. So, I will not be having any packet here. So, one possibility is both of them direct to the above side, and they cannot move. So, I will end up in this state after time slot; if both of them are directed to the bottom side, I will end up in this state. If both of them are going to be in parallel, I will end up in this state. If they are crisscross, technically these two sheets are same; they are not different.

If the packet does not go out, I will still get the same scenario; they are not. Again these two states are same; all of them are happening with equal probability. This will be happening with 1 by 4 p 0 tilde. This is happening 1 by 4 q 0 tilde for all four of them. So, let us identify; this one is which particular state, eight, okay. This one is five; this one will be six, both of them.

Student: Sir, can you describe how the six step comes step six when both packets come, is it parallel.

What?

Student: In case one when packet moves out, how do you reach the state five after eight, first case first case.

First case, this one?

Student: After that, packet move out from output port, two packet arrive and then.

Two packet arrive, they cannot be returned into this buffer.

Student: That is true.

They both are directed to this. So, after that, see this is the time which is starting.

You started at this point, two packets arrive [FL] in the incoming port. Now at this point, the packet has been read out from the outgoing port. At the end of this time slot, what will happen? This packet is no more there in this buffer, but these two packets cannot be moved, because they both were directed to that particular thing. So, this decision was done instantaneously, t select is 0. So, both of them have to remain here, and they are still directed towards that direction. So, this scenario looks from that table is stated.

Student: Next five.

This one; so if the packet is again going out. So, next one is when both of them were directed towards downward actually. When both of them are directed towards this case comes when both of them are directed towards downward state. So, this was the situation at t at this point. By this time you reach here, this one packet will be pushed here. See, this is before at this time; at this time, what will happen? This packet will go out when this packet will move from here to here; you will end up in this situation. Okay, maybe I can write it in a slight; I will use a different color and show what is this situation at this time and this is the situation at this time actually, okay.

So, just before the start of slot, I am like drawing with that different color. So, just before the start of the slot, this is the situation just before the start of the slot in this case. So, if the packet does not go out, you will end up here; packet goes out, you will end up here output port packet. In this scenario, this is at the beginning of the slot which is happening. If the packet goes out, packet is no more here; one of these packets will be coming on this side. One of these packets will be coming on this side actually, because this output buffer is empty. This read out can happen in this slot.

So, if the packet is not going out, you are here; otherwise, you are here. The initial thing in this scenario will be this or this; if the packets move out, you come here. This packet goes out; this remains there; this one will move on the outgoing side. If packet does not move out, this still goes to the outgoing port, comes here; this will remain blocked, and this will remain as it is intact there two situations, same here and in this clarifies. So, this is at t k and this situation is t k plus 1. And then of course, whatever are the stages which you arrive after in time slot tau k, I just give them the numbers, and based on that I will fill up the matrix.

So, this one is six, this one is five, eight; this is ten, seven; this is also seven, and this is also seven. So, seventh I can write here 3 by 4 q 0 tilde; ten I can write 1 by 4 q 0 tilde; eight I can write 1 by 4 p 0 tilde; five is also 1 by 4 p 0 tilde; six I can write as half of p 0 tilde, fine.

Student: Sir, seven should be p dash comes three times.

Seven comes three times, 3 by 4 q 0 tilde.

This row happens with probability p 0 tilde, packet goes out; q 0 tilde packet does not go out. P 0 q 0 tildes depend on the state of the next state. So, only thing important is packets are coming immediately into port the movement those are free. So, I am assuming there are infinite buffer here; packet is always here present. So, it is not that when you read out this packet. So, no other packet can be written in that same time slot. It will be instantaneously written in the input port; maybe that is the only variation which you have to careful about.

Student: Why we are not taking finite buffer not only single buffer.

Where.

Student: This input port sir.

[FL] All switches have input single buffer, single buffer per input port. I am talking about the complete switch at the input of the zero th stage.

So, there I say if the packet goes out in the next time slot, instantaneously another packet is available. See what happens is you have a packet here; it takes whole one slot for this to be read out. What happens in the next one? You cannot write the packet instantaneously in this buffer. Usually, it should remain vacant for the next one no; that is not the case. I am always assuming that p 0 bar is always one. So, zero th stage, the packet will be always there in every stage.

So, even if the packet is read out, it takes whole time; next slot the packet will be immediately available. So, that is the maximum loading condition. Now staggering of the packets or they are being stopped because they cannot be read out is happening inside this switch. I am not looking at the input. So, input technically if there is large switch

with multiple stages 0 1 2 to some whatever it is n minus 1; at this input, I am assuming it is like a large number of packets are there. So, at least two three buffers must be there at least always, and they are always present while this does not happen inside.

So, that is the reason why you could not have when this packet was going out, you cannot move a packet here, because there was only one single buffer here. But at the input of the whole switch packet is always available which actually means there is no single buffer; there is going to be more than one buffer present there; that is the thing. Otherwise, I cannot take this case, and that is the condition for maximum loading; we are trying to compare. So, there has to be equal testing ground for the both kind of models. So, remaining ones I am just writing it down by looking from the paper for this particular matrix

Okay, we do not have much time. So, this p j tilde square or maybe you can actually look into the paper and get the whole table; I need not write it down. Important thing is that how to get the table; now you can even drive on your own also. So, let me just quickly go through the middle stage what happens. There is now arrival and departure probabilities, both are there.

Student: This will be j sir if you are talking about input step zero.

This will become 0; j is equal to 0. They actually have given it in general form; again you will have the equation; I think this I can now remove this.

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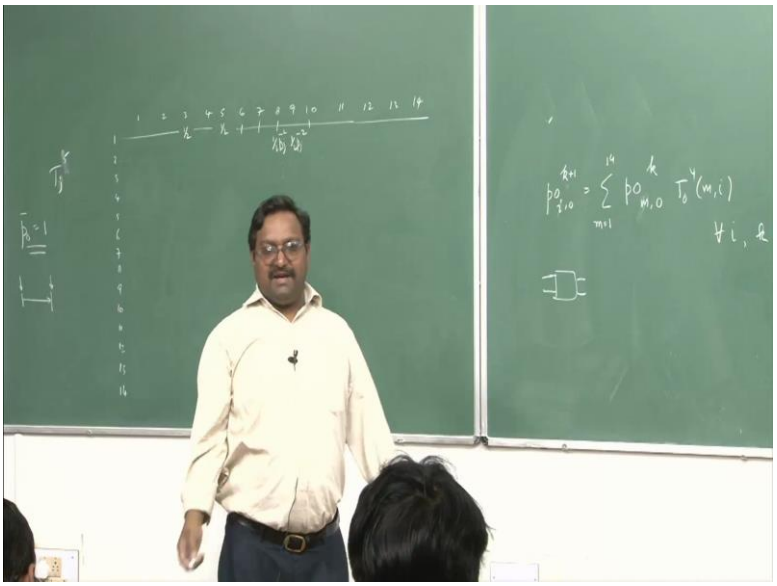

Okay, this is for a state I how you will compute time step k plus 1. This will be nothing but your transition matrix which will be there m is equal to 1 to 14 p 0 m zero th stage whatever was in k. So, this will be happening for all i. So, i goes from one to fourteen in all k's. So, this will be transition matrix; it is very similar thing what we did earlier. Now let me define this thing as t 0 t j 5 we call it, not t 0 and we have t n minus 1 6. So, this for j th stage in general not for zero th stage. Zero th stage case is different, because the input probability is this.

But now there is an input probability p j bar and p j tilde; both have to take part. So, first one you take; for example, you are in state one. I am only looking at this, okay. So, what will happen? Only packets can arrive, packets cannot go. So, packet will arrive with probability p j bar. If both the packets will come, it is a p j bar square which will happen and then you will end up in state of eight and nine, eight and nine; that is what will happen. So, you will have half p j bar square half p j bar square here. If none of the packets come, you end up in same state; oh sorry, upper line also need to be removed; this should have been here q j bar square and of course only if only one packet will come, then you will be in state four p j bar q j bar; that is all.

Next one if you want to build similarly, what will happen if you are in step. So, now you have to look at the arrival as well as departure both probabilities together. So, you are in the beginning of time.

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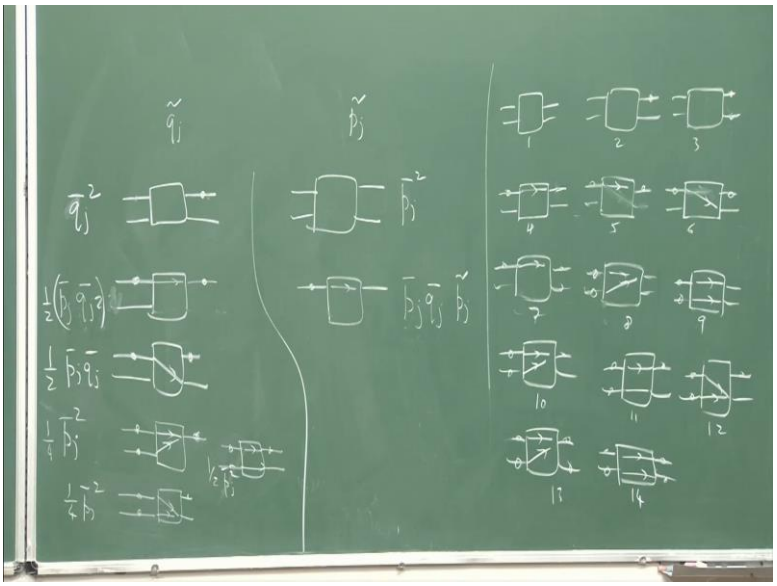

Beginning of tau k, you are in step this particular step, no packets there is only one packet. This is the state to begin with. Now you can actually have your initial state; basically, what will happen after your. You started at this time; at this time what will happen? Packets can arrive, but they are not instantaneous arrival the way it was happening in the first stage. First stage was or the zero th stage; here packets can come or packets may not come, and this can go out independently, okay. Only if packet is already available, it will move here if that slot is available, but when packet is being pushed in, this will take this much time, and packet will be available only at this point at the input in the input buffer. So, they cannot be moved to the outgoing port.

So, with this now the probabilities are this is remember with q j tilde, you will have no packet here with p j tilde from state two. So, I have written those two, and depending on the situation, this will be now corresponds to q j bar square. You can have a packet p j bar q j bar, okay, directed to this half probability. Remember, this only one packet coming in can happen with 2 p j bar q j bar actually; half of it will be directed here, half of the time it can be directed here. These two are different cases. So, only one packet arriving and this can be directed to anyone of them with equal probability. So, the remaining half will come here.

So, I have to multiply this by this actually to write in the matrix and next probability that two packets will come; this still remains. The two packets will come. This is p j bar

square. Now they can be directed here. So, this probability is 1 by 4; they both are directed to the bottom side this 1 by 4, and then of course, there is a case. So, this can be crisscross also; it will be 1 by half actually p j square bar. So, equivalent things you have to write with p j tilde; this is with q j tilde. So, you can then identify the state and then build up the row.

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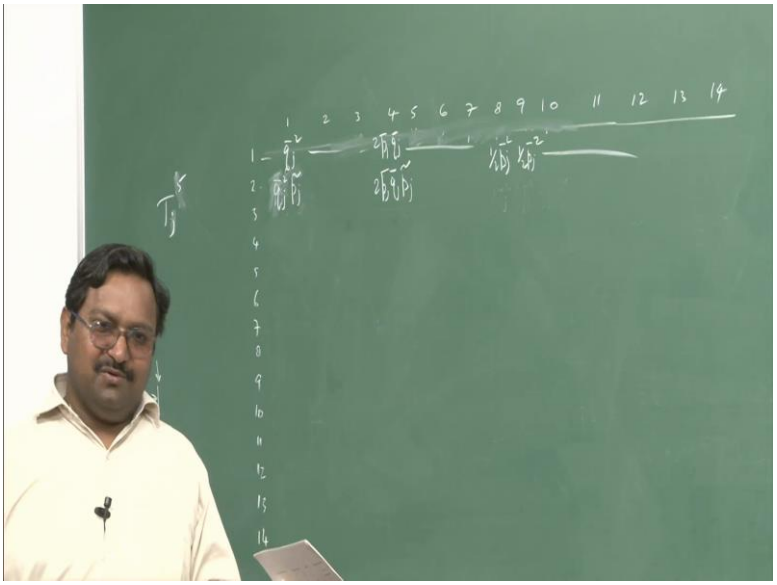

So, I can just quickly write what you will get is q j tilde, no packet, okay p j square. Okay, bar part I will always write first; no packet arrives q j square p j tilde were two different things which I am multiplying; I will remain in the same state. I will end up in this state, no packet arriving. You can similarly build up only one arriving, going to one free port p j bar q j bar p j tilde.

Student: First state will be sir; first state, sir? First state is p j square sir p j bar tilde square sir q j bar sir sorry.

Sorry; sorry, this will be q j; same thing will come, sorry. These same expressions will come here except the outgoing packet will not be there; that is the only difference. So, you will be in state two with, okay, let me just identify those states which I am doing; that is the state four. This also I need to include; these two are technically same states; here they are not same states, there they are same states actually when the packet is going out.

So, I have to multiply it by two. So, this is fourth state; it will be 2 p j bar q j bar p j tilde. So, this is an example. So, I think you can build up in this fashion for this particular row. So, again you can look into the paper. Important thing that you appreciate the method that now both incoming probabilities and outgoing probabilities have to be considered while building up the transition matrix; it is not like the earlier cases. So, I am actually stopping here.

The last one is for the outgoing port or what you call n minus first stage outgoing port based on that, okay. So, remember the packets will certainly be going out; your p n minus 1 tilde is always 1. Only the arrival probabilities will be participating. Remember when I did for the input stage or the first zero th stage, there was only outgoing probabilities which are participating. In intermediate stages, both of these will be participating. On the outgoing on the last one n minus first stage, only incoming probabilities will be participating; outgoing means 1.0 defined there. So, in the very same fashion actually we can do that and we will define that thing by 6 n stages n minus 1, okay. So, same fashion actually you can build.

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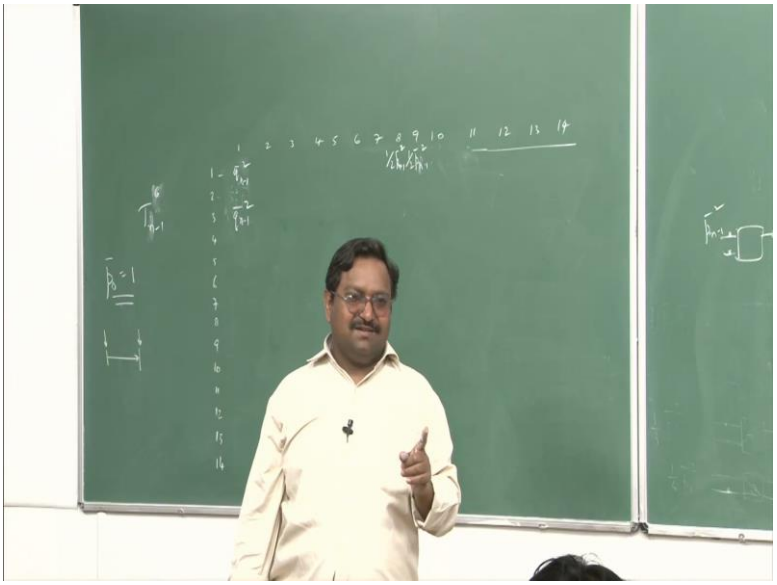

See for example, you take state two, because there is the packet on the outgoing side; I am taking only that example. This packet will certainly go out; you cannot stop it, it is 1.0. So, once it is 1.0. So, only the packet which can come at the input that is important. So, no packet come its q j square q n minus 1 bar square. So, you will come here as q n

minus 1 bar square. You will remain in the same state, outgoing port will go. If you are in state 3 for example, both packets at the output port will certainly go out, okay. You will come to state 1 from 3 if no packet comes in same fashion, okay.

If for example, both packets will come, then two will turn into either ten or nine for example. If both packets will come, you will either become ten or you will become nine one of the two, depending on how the packets are being directed. So, you have to have half for p n minus 1 bar square.

Student: If both packets come?

Both packets are arriving.

Student: Yes sir

So, this arrival happens with p n minus 1 bar square probability. Outgoing packet it does not matter, they will anyway will be removed; that probability is one.

Student: Okay, in that case it will go to eight no, sir.

So, both of them are here; they both can go to the same port, or they both can be directed to its separate ports. So, if they go to the separate ports is nine.

Student: Nine.

Sorry, eight and nine; eight and nine, you are right.

This has to written at nine; that was not visible from here, okay. In fact, if you are carefully observant enough, you can just simply put in that t j 5 case your outgoing probability equal to 1, and you will get the same matrix actually. So, the middle one or t j 5 is what is important; from that you can actually get the first one as well as the last one. Only thing you need to know the boundary conditions, okay. So, if you just apply the boundary conditions, you will get even this particular matrix. Now remaining procedure remains the same.

Student: What will happen in step thirteen and fourteen?

Thirteen fourteen these packets will go out; that is it, it will remain here. So, thirteen to you will come to eight.

Student: Directly?

Yeah; there is no other option. If you are in n minus first stage, these both will be read out; this packet cannot move here. So, you will come up with eight. If you are in fourteen, you will come to nine. So, I think that gives more or less the idea of that how even this simulation is done when t select is zero. So, after the midsem break again, we will continue with and I will start do some fresh topics. So, this buffered delta finishes off at this point.