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VLSI Design, Verification & Test

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Module X: sequential Circuit Testing And Scan Chains

Lecture III: Scan Chain based sequential Circuit Testing – 2

So welcome to lecture number 3, of module number 10. In which case we are discussing about scan chain based sequential circuit testing II. So in the last lecturer the one lecturer before that followed that testing sequential circuit as these are flip flop so which actually making difficult to controlled secondary primary input and secondary primary output difficult to observe so because of this reason we found out the sequential circuit testing or ATPG is more difficult than combinational circuit.

For the combination circuit are single times better can be determined which can detect false. So that is why scan chain propagation justifying approach. Now if u going to sequential circuit which is already seen in last two lecture which are the if you want take sequential circuit the what you have to do if to first go for the time from expansion method that is you have to slowly controlled the virtual primary input and secondary input, which are the output of the flip flop so that cannot be directly controlled.

So what we have to do so have the use time from expansion or that is mean by serious of sequences every controlled this virtual input then you can apply the test based primary input and you can test the circuit. And follow that the process is complex process because you have to controlled this flip flop output which are the secondary input which are the serious of factor

required to do and you can find out the last stage it can be a conflict which can need to the restart of the whole producer so leading in lot of wastage of the compaction time. So when we find out the when we discuss the last lecture that to avoid this complex business we said directly controlled flip flops. By using this scan chain so these are the good physical approach and we so it can be easily daring in two dimensional pattern we can easily takes that circuit in which case in first pattern set and reset the flip flop is required.

And then apply the primary input is second pattern and do the testing. But only found out the n variable in flip flop the is required a two n number pins in this circuit in do that, Which are extremely complex procedure because it means the circuit has around 10 to 20 thousand of flip flop an having 20 to 40 thousand extra pins is not a very physical approach. Listen because the packages is more than one thousand pins we have been the limitation of the 102 packages, I mean generally have in the market so going beyond that is very expensive and having about 10 thousand pins in physical situation. So while the idea was good which convert the sequential circuit to virtual primary circuit is testing for the huge number of pins out actually creates the mass record.

Then what we have done, and then you have to say now the letters called controlled set z input like flip flop by a primary input making this much primary inputs. Then it is using a shift register and load the shift register in a sequential fashion and output of the shift register will be connected to the set and reset lines. So what we have to set and reset lines to be controlled what you can do you can as required, you can scanning the values or shift in this values in the shift register and do that. Then found out the good approach because that the two things are the pins out are not increment because you required pins out for the putting the values in the shift register you need the different talk with the shift register and extra output for the shift register.

And three more pins you can do the testing that you can control z the z is individually using this testing. But now here the problem is it have n flip flop then you required two n number of extra flip flop in the shift register making this area are variable. Also secondly meant to controlled the flip flop now required 2 n number of clock pulses because shift in the values of 0s and 1s for the set and rest lines. These are the n flip flops we saw that 2 n lines are set and reset lines and then

we are shifting 2 n numbers of patterns or pins in this case top control the set and reset lines. So that is a comparison process. Then it found out the real great VLSI design testing that is scan chain we solved most of the problems.

So what the present state, if you already have shift register, if you already have a series of a flip flops circuit why not used them a scan register or why not used a shift register, so easier that I will not use any extra shift register to control the flip flops either I used my circuit in two modes and the one modes is normal mode when the out of the national function block go to the flip flops and another mode what I will do I will connect all the flip flops in the shift register mode and the output of the flip flops will be connect to scanning pins also output of the previous D flip flops. Already we have seen that the architecture how was can work and it is now the test mode you can shift in values in scan chain whatever you required to conflict the flip flops.

And if there n flip flops you required n patterns to control the flip flops. So you have saved in n number patterns compare to a shift register approach. And also we have seen that you no required any extra kind of shift registers. So no required extra flip flop do this in register based testing. All are the extra requirement is mask which are the very simple because you do not required set reset arrangement in the flip flops. So this set reset arrangement in extra area you can incorporate in the any have multiplex so all the problems are almost for a sequential circuit solved by the scan chain problem, or scan chain design. The only issues that remain are to set the flip flops you require n flip flops in the circuit.

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You require n bits or n clock pulses to control them. So only those parts remain, all other things are solve using the scan chain based. Today what will see? Will see it is about the scan chain how that designs? And how can optimize of the number n flip flops you require, n number of bits to control the flip flops. If we see can decrees the remaining other things will try seen about the scan chain.

Today, so first will start with the example, so you remember this are the old circuit. We are considering every day so in a lecture we can start a 0 for in a two register. If you recall you take a stake 0 first you require a 1 variant so D is propagated and you require a 0 variant so you require a 1 variant, you require a 1 variant, so you require a 1 variant so you require a 1 variant. So we know that this is one output of the one flip flop and the other output of the flip flop.

Which has to be controlled by any means we can saw that how by controlling it by a set rest lines. Also controlling by shift register variant so 4 flip flops now will see how it can be done by using the scan chain. So this is 1:1 and 1:1 done. So already discuss what will do in first step will make n=1 that is remove the next state function block from the n flip flop are connected in a chain. So already said if you make n=1 and the test mode=1 if you do and what is happened the

series of flip flops is decoupled from the circuit. That is next state function block is decoupled from previous connection in a chain mode.

Then in this case you require a 1 over here and a 1 over here, so you require 1 in a clock pulse and 1 in a clock pulse. So two 1 with 2 clock pulse will get the flip flop set 1. We just look at the architecture of the details, so what happened so you can make n=1 so this is the normal input from the n set block so which is got we considering the output is no way which is cut flip flop similarly the output of the n set block going to the flip flop number 2. That is also cut by the making n=1. So what happened this scanning to the external pins that to the flip flop. Output of the first flip flop is connected to the input of the second flip flop and the final output is scan out. So now it becomes a shift register chain.

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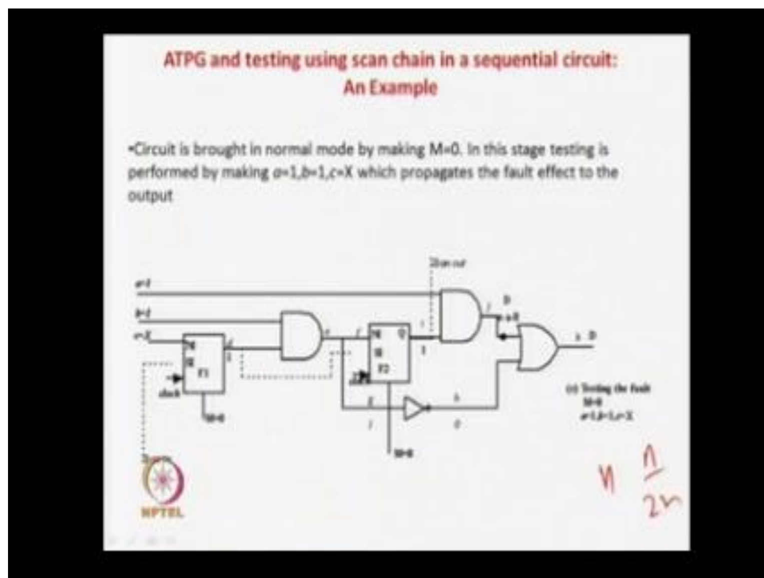

So now you apply 1, 1 on the rate of 2 clock pulses then what will have you have a 1 variant and 1 variant. So this is actually set the flip flops. So you can understand what will have to achieve so in the previous require using a shift register can do this so you require 1 0 and 1 0 because set equal to 1 and reset equal to 0 so pattern of 10, 10 shifted kind of things to make a set register only a require a pattern 1, 1 control the registers flip flops. So the n flip flops so you require only

n patterns register of scan chain based testing and 2n in case of shift register based testing. So not only it is scan chain solve the problem of extra number of flip flop in this series what you called in register but also the solve the problem of reduce the number of time required to moving the values to require the control the flip flops. So in this case the flip flops maximum n patterns are required to shift.

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Now what happened, now you get this one is 1 and you get this one 1 it is done. Now we go to apply 1 and 1 is known to get the flip flop at the false tested. So now what you have to do you have make n=0. So already discussed when n=0, then the scan input at the scan chain has decoupled from the circuit and the normal n is a block is connected to the circuit. So this is done whatever seen the normal operation of this circuit so what will get so you are having a 1 and you can apply 1, 1 here, so you get a D variant and get a 1 variant and the you get a 0 variant then you get the output and reduce tested. So this is two patterns required testing so it should not called two patterns it should called this is a final pattern. We are actually apply the primary output to the test n to bits shift required 1 in a clock pulse and 1 in a clock pulse to this kind of flip flops.

So you require n. that it is n+1 number of patterns. So in case of shift register which is 2n+1 and in case of set reset line testing circuit in test pattern. We require the entire two patterns. One pattern directly required to set and reset to this two flip flops and one pattern was to do the testing. But in that case the extra numbers of pins are become so high actually all that solved. Therefore we are go to this scan chain based and everything is solved. So all the disadvantage in this case we found out require two patterns and n number of patterns to the shift this circuit. So 10 thousand flip flops see for an example in this circuit, in the problem is to have to have 10 thousand clock pulses.

To set the flip flop first or reset the flip flop first then you can apply the final pattern. That is only a problem that is remaining with this scan chain all other problems can be solved because no extra area for the shift register and you consider as put some multiplexes and what is the consequent put in the multiplexes does not have any much consequent. But you have to understand because already told that when you are having this scan register you can see would not have a set or reset lines are not gate.

So whatever area by say putting this considering eliminating line is set and reset line now you can be considered we got some advantage by whatever set by removing this set reset lines part of the circuit I can add for the multiplexer. Exactly saving amount of circuit you are saving is used by multiplexer. But what some areas we have save because of using the set reset lines. And we can do it in this way.

So this way you can understand basically you considered broad required scan chain which is not absolute terms you think. But you think of in this way. Now we are trying to solve other problem. The main problem is n number of pattern to set. So now let as see other advantage. That actually how to solve this problems will get another by production some times and by producing see get as see here advantage of scan chain will see.

So one advantage will be n will be reduce and second will be getting another advantage will be come out. What happened if you are using this scan chain till now what about we discussed ,

shift register mode, set reset mode so what we have to do. First it was remove flip flop that was the first step, and second step D algorithm.

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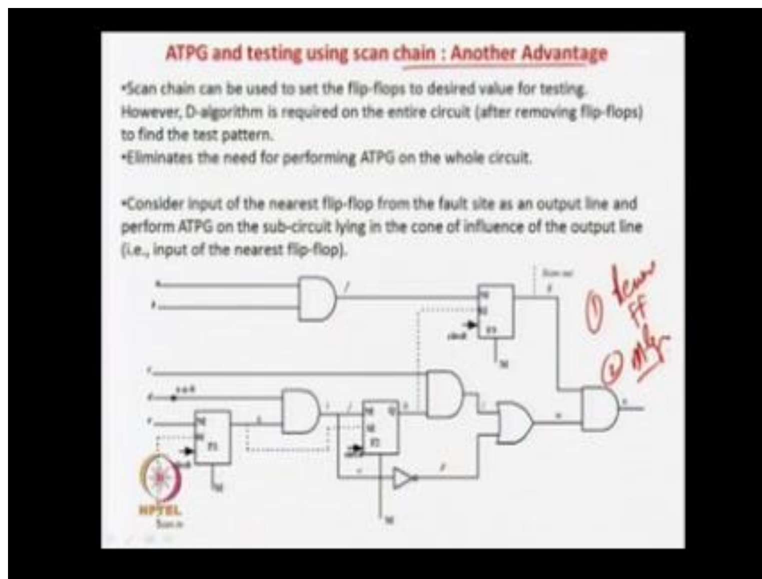

So remove all the flip flops in the circuit and this performs a D algorithm. These are the two basic steps. Remove the flip flops and remove all the flip flop and to the D algorithm. So whole circuit apply D algorithm, but now we will see that the scan chain you did not to do D algorithm of the whole circuit. And you can only take partial circuit to this. So let as see the new circuit we added this part of the circuit to restrict the concept. So let as take a stake 0 to 5 variant. Now if see the I want the standard what will do will remove this flip flop and remove the flip flop connectivity and remove the flip flop connectivity and do an ATPG in whole circuit.

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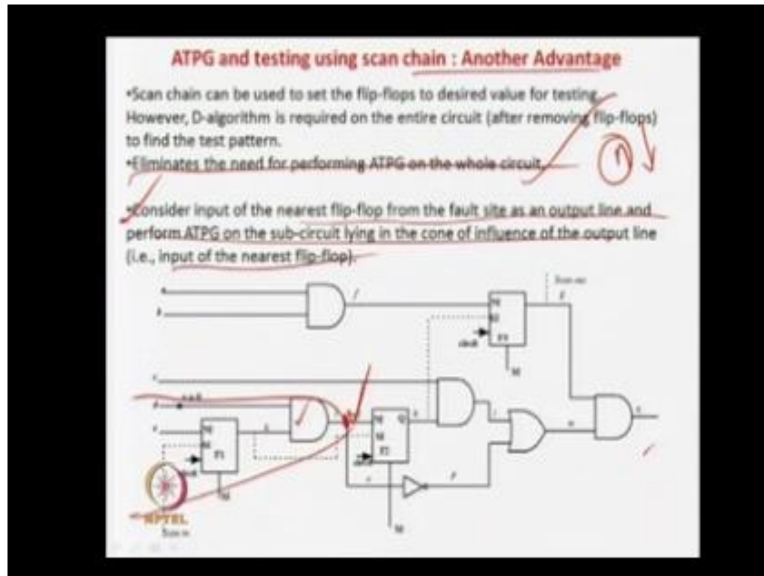

But so it takes some time completion. But now we see that if you want to do another advantage it will see in scan chain do not considering the whole circuit for the ATPG. What will see? First you have to find out entire circuit you eliminating ATPG in circuit. It is new advantage is eliminating ATPG for the whole circuit as well as n pattern also comes down. So we have to find out what you to considering the input of the nearest flip flop from the fault site as an output lines and perform ATPG on the sub circuit lying in the cone of influence of the output line. So what we have to do basically we have to find out flip flop actually which is nearest to the fault side.

So in this case you can think that so this is my nearest flip flop input okay, because this is output is quiet for input of this flip flop input do not come influence of the fault site. So you can think that this is the nearest input of the flip flop which is nearest of the fault site. So just considering the nearest input and then make a cone of influence. That means is nothing but in these gates is output gates actually A and B that means the output is depended on inputs. Is a very simple definition, so in this case this point so which gates are influent in this one so this gate is involved in this D and E are involved of the flip flop. Only this circuit is involved this point. So the cone of influence only about this very small circuit part of the circuit.

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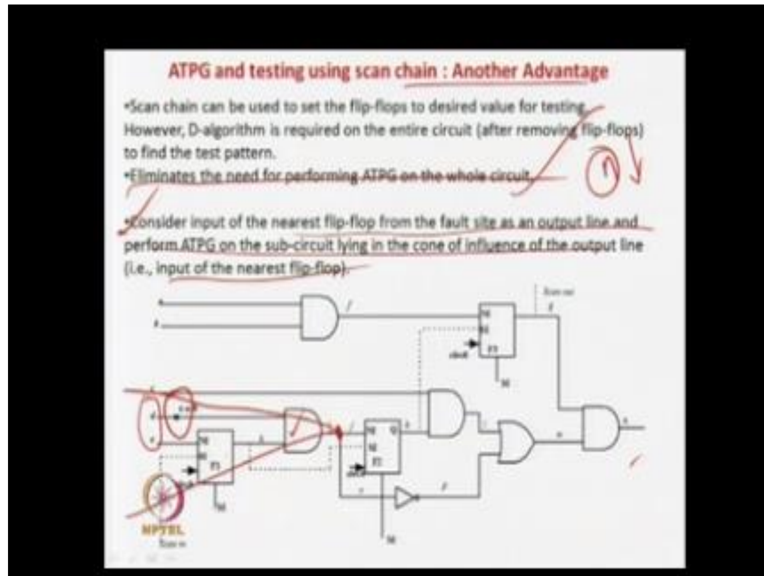

So what you have to consider only this much smaller circuit, because it was find out the nearest flip flop and do that. So the level what we have to done so just remove the flip flop and all the flip flops are remove now do not considering any thing as. The advantage in steps, the small part of the circuit variant ATPG and solved the problem. But yow will take normal approach removing all the flip flops and ATPG on those things we will take a round step.

Now let as considering the parts. Another advantage is scan chain advantages it is a traditional advantages. Let us see that this is the whole circuit of the flip flops been removed now let us consider the paths, this one is the path so we take approach another advantage because we show the real advantage and scan chain. Then you have to compare the approach that is conditional approach and scan chain approach in the conditional scheme okay.

Let us consider the whole circuit and do that so that you can see exactly what is the advantage which will come out so you want to apply the approach then that is the newer approach and that will not give much high value right let us say the path. So what is the path so let us the path is D then I this is the fault path you are taking I, the you are seeing O then it is P, N and then P for the fault propagation. But this has not been selected because from here there are two different

frontiers from this there are two frontiers one is this gate and one is frontier over here and another frontier to the down way. So any one could have been taken but the person has selected this one let us go above it.

So the stake is 0 fault take 1 would a D prime here you require 1 over here and flip flops variant it is so you can do by scan chain you to be 1. D variant is you get an OR gate, D over required a 0 over and finally we get the D output. That requires a 1 over here so the flip flop by scan chain you control the output 1 so these about the traditional ATPG or sequential circuit using scan chain. So you require 1101x do not care and set to 1 and final flip flop is set to 1, f3 flip flop is set to 1 and another flip flop is x do not care in x over here and then you can test stakes okay.

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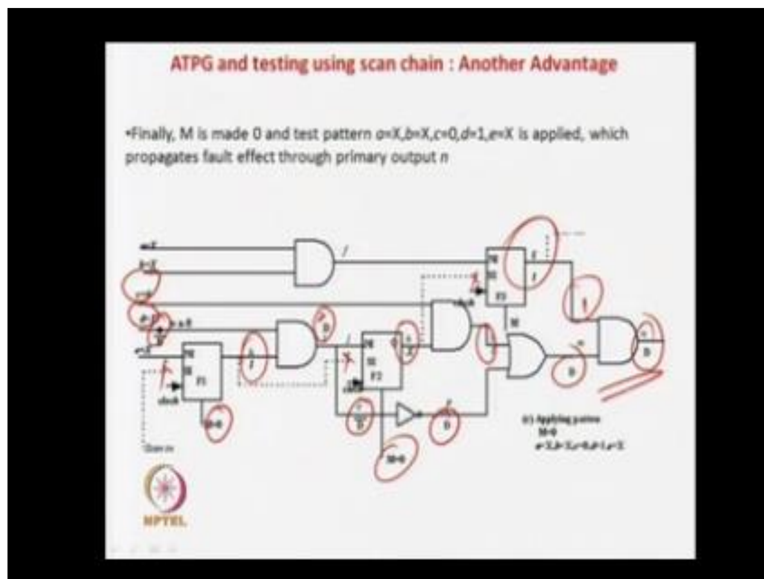

Now let us see what happens so first we know that you have to set this flip flops. That means n=1 this scan chain is connected to the decoupled circuit. Apply 1x1 3 clock pulses flip flops have to be 1. So you required 3 clock pulses require n flip flops so n bit was transfer. Further a=x, b=x, c=0, d=1, e=x would apply the pattern to sensate and propagate the fault effect. Finally m is made 0 and test pattern a=x b=x c=0 e=x is applied, which propagates fault effect through primary output n. One the part is done the flip flop is decoupled from the circuit; normal n block

output is connected so you considered 1. One variant this is not required anymore. So now make apply d=1 what will get is stake and prime over here. D prime and 1 over here by scan chain control the flip flop so get a d prime over here. D over here get a 0 over here by apply =0 because this flip flop is controlled by the scan chain and you get the advantage and fully your circuit is tested.

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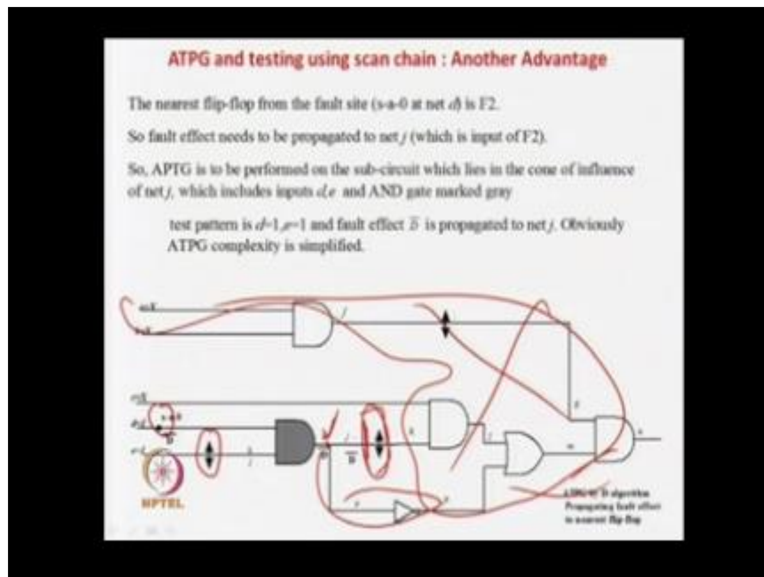

So in this case we required 3 patterns. So that is 1x1 is applied 3 clock pulses and finally we apply the pattern c=0 and d=1 these 4 patterns are using testing in scan chain. Now the other advantage the circuit considering the whole ATPG in the one problem and the n number of patterns are required to set the flip flops because in this case 3 flip flops we required 3 patterns do that. Now again what we are saying that now we will take the new approach which is this flip flop was here and stakes for here and another flip flop was here so this is the nearest input for flip flop. So that is nearest from the fault site, this is nearest flip flop will be the fault site.

Whole circuit can eliminate only the circuit will considered input that is cone of influence, so the sub circuit going to considered. Going to consider the flip flop all the circuit in only influence cone of by the flip flop, it is all the small sub set will come in to picture this gate will come in to

the picture these two flip flops are come in to picture and this two input will come in to picture. Nothing else so only do ATPG on this it the big advantage you are going to see on this now what we are going to do so we are applying this is a stake at 0 now you have to apply 1 you get d prime over here now you require 1 over here because our fault d prime propagate.

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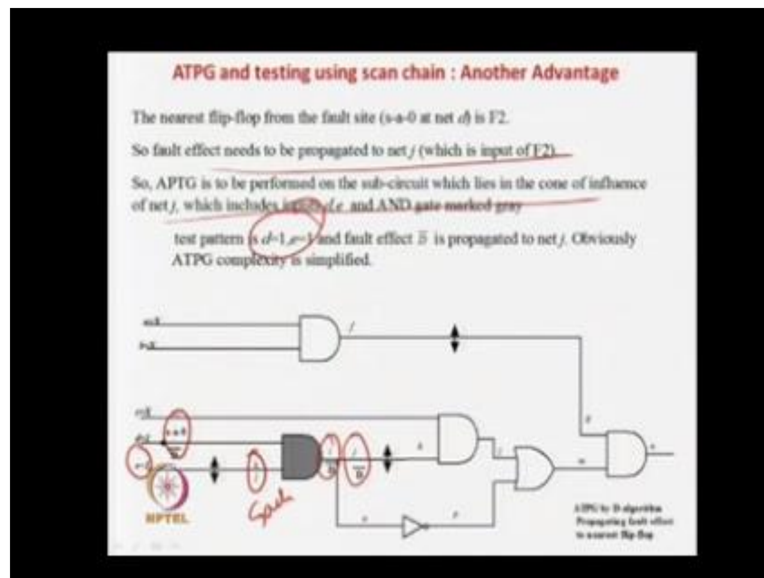

So we get a d prime correct over here for that =1 this are flip flop these are scan chain. So we can set it and this is the case and so the fault is here and this is the input of the nearest flip flop of the fault site you job is done. We do not require any other part of the circuit ATPG d algorithm is very simple over here so you consider the small circuit and your job is done. So what is this fault effect needs to net J which is to be propagating to set in flip flop. ATPG is to be performed on the circuit which lies in the cone of influence of set. It is small part. Test pattern d=1 and fault effect is propagate to set and the job is very simple approach. So the combinational circuit is reducing greatly.

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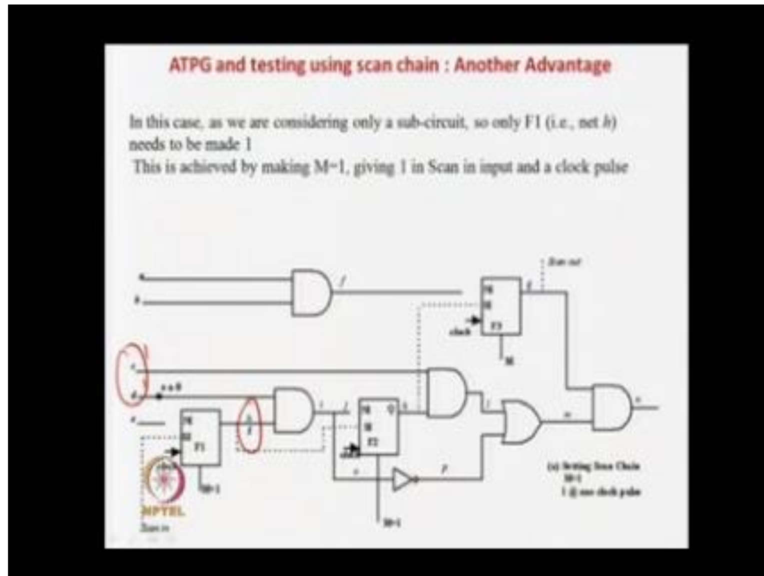

So now what we do so now in that is what is done so you only know that this is equal to 1 and this equal to 1. So for the testing for you so for that only one requirement was that so this flip flop has to be set to 1 by the scan chain. So what you can say you can say that again you save greatly do not control the two flip flop. And other advantages is we are not required to save this two flip flop previous case required to 3 flip flop now you don’t required this because the only smart part is considering the portion of the circuit.

So 1 flip flop and 1 clock pulses in scan chain is there but we do not bother much we get n=1 is set pulse. So you can also think that there is a fault here where that you can say in this case it will be nearest space so in this case to set the flop flop then you have to apply see what you can call this flip flop to set it is far away from carrying. In this case you require n flip flops and require n patterns to set or reset the flip flop. But the entire flip flop is not from the fault side as we are considering only a sub circuit, so only F1 needs to be made 1.

This is achieved by making m-1; giving 1 in scan is input a clock pulse. In that case we are going to take n flip flops and patterns set or reset the flip flops. But all the flip flops are not bordering from the fault site. Half of the flip flop almost nearest from the fault site, every time will going to

average case find the fault is nearest to the flip flops. So the great deal of saving look at the average case. In this case first flip flop will be conscience only one clock pulse is set the flip flop as required. Second flip flop is 2, so the average cases lot of saving in the number of patterns required setting or resetting the flip flop. You make n=0.

Obviously the circuit start in normal way, applied d=1 over here, so it is d prime. So the propagate the fault value to the input of flip flop. Another mode cannot use scan chain mode. in the previous what we do we set a flip flop you give the primary output that is propagation and sent the primary output and your job is done. But here the disadvantage is here part of the circuit in ATPG is an propagating in fault effecting nearest flip flop so again this steps what we do again this got over here, this is the pattern will apply. Now what you do so there is,

One more steps you have to picture is very important, initially last two steps set and reset the flip flop get the fault values propagate the primary output. Other steps involved in this case n=0 applied the clock pulse, then the d prime is fault effect is input get to the nearest flip flop be selected. What are the other steps will go for n=0 and give a clock pulse so the d prime is recorded the one of the flip flops. We have added four steps. In forth step what we have to put X in this scanning do not bothered keep some clock pulses, so this fault effect gets out through your scan output, there is two more see what I have done in the first case previous approach so you gave a scan chain set this scan chain apply the pattern and get in to the fault affect in to the primary scan chain your job is done.

But here you have to consider all the faults set the false found the false pattern there as well as you have to do ATPGs for the whole circuit that was the big problem then how we solve this in the second approach consider only a partial circuit which false in to cone of influence of what which false of the influence and the nearest to the false side. So one that is done what you will do you will do ATPGs in the small part of the circuit that is very less chances of pollution and all so your job is done so it will save lot of time and complete ATPG. Now what we have to do next necessaries than next we said the influx only whatever require we said only whatever require we said then using your what you call scan registers once is done propertied to the flip flops selected.

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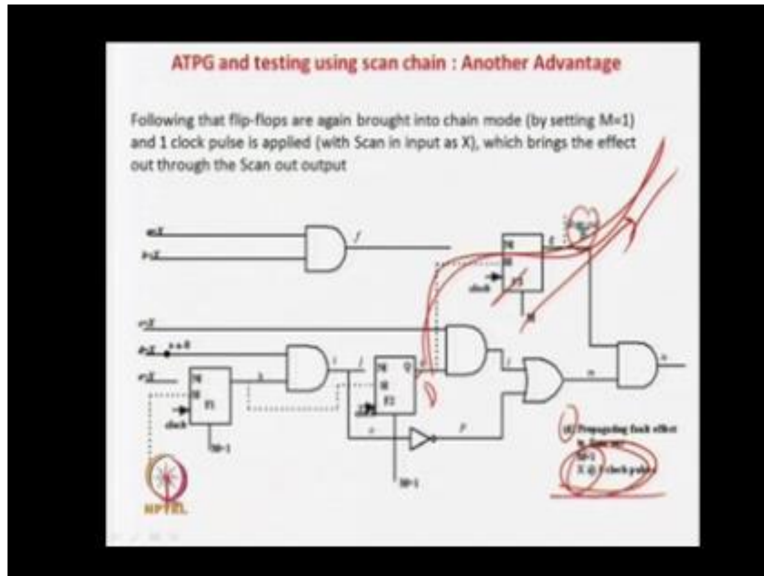

Then there are two more steps to be done now you go to the m0 is that to the formal mode then apply a clock pall so your fault affect the recorded that to the output of the flip flops which was the nearest the selected. Now that was done so your flip flop it was selected over here, now what you have to do, now we are not consider propertied the flip flop fault to the output of the primary output. So what you will do? You will use this scan register of the scan output propertied of this value. So we have to again apply the output of the scan chain okay whatever was the nearest I mean there is one more flip-flops has to be past to be of the scan register, so you just apply 1X you do not need to set a flip-flops which is near to butter of the pulling out the value.

So we are given one clock pulls value in the past output flip-flop, so here are the understand that you are not much said about the clock pulses because on pulls is required to set this flip-flop one pulls to the record to the value and one pulls was there to take out the value, so in this previous case require three clock pulls set the flip-flop one pulls to the record to the value and one pulls was there to take out the value. So they are so not much saving that but what we save greatly is it performs ATPGS small part of the circuit.

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If you do that they will be very, very less chances of collusion and you will be always getting successful result so this is another very big advantage of combinational scan based things you can perfume ATPG very small part of circuit and that will great reduce your chances of collusion and almost all the false you can take very easily you can go for ATPG. So that is what while we seeing. That is what we are going to see another advantage.

So in case of ATPG using a scan chain what we have to do ATPG is part of the circuit. And secondly sometimes we will be saving number of clock pulls to set the flip-flops okay. That is the 2 advantages of the scan chain. So what people will do people generally do not go full circuit ATPG in case of scan chain ATPG the cone of influence will be partial circuit then the bring out fault effect to the scan chain rather than bringing out what you call the primary inputs okay.

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ATPG and testing using partial scan chain in a sequential circuit

- A circuit with sequential dept d_{seq} needs d_{seq} clock pulses and patterns to set the flip-flops (to required values) when testing is done using time frame expansion approach.
- In case of scan chain if there are n_{ff} flip-flops, then n_{ff} clock pulses are required to set/reset the flip-flops.
- As $n_{ff} > d_{seq}$, test time is higher for scan chain based testing compared to time frame expansion method. Also, multiplexers are required in case of scan chains while no extra circuitry is required for time frame expansion method. Only ATPG complexity is lower in case of scan based testing. It may be noted that ATPG is off line exercise and test time is very expensive as patterns are applied by an automatic test equipment.
- However, scan based testing is still the most widely accepted technology. Time frame expansion scheme cannot set/reset flip-flops which are cyclic (i.e. whose input is dependent on its own output). So scan based scheme or set/reset with shift register scheme is required for cyclic circuits.

So now, now what we have seen we have solved the problem got one advantage ATPGs done on the smaller part of the circuit. But one disadvantage still lie is that one that n facts the in circuit require n fact either to control the part of the value not yet solved. So we try to solve in a different way is actually call the partial scan chain in a sequential circuit so we will look in to the partial can chain. So just am recall early we have discussed the last to last lesion in sequential circuit using time from expansible plan so what we said that?

To set a circuit all the flip-flop is do not necessaries of scan chain to set all the flip-flop is the flip-flop in the circuit using time from expansion method we require at most d sequential number of clock pulses, because we have assume that all the flip-flop are connected in to the fashion in the circuit that is last flip-flop connected in to the previous flip-flop depended on so far the sequential circuit maximum in this case so it require n if the N number of flip-flops so sequential step max can be n.

And what is the number of clock pulls testing as the asset or dissect case of the time is metal sequential expense but that will be old case when all your flip-flop connected in to a chain fashion. But generally that n flip-flops in the circuit. D sequential not be old case is equal to d

sequence number of equal sequence is everything can be achieve. In also there will be cases when or general number of cases of the much, much larger in D sequence. So if you are considering what I have said using of time from expansion method then you have require d number of sequential best set of flip-flops d number of patters set as the flip-flops.

But in case of scan chain you always require n. N is number of flip-flops require n is number of patter is number of bring out the values. So one advantage we could see is the previous approach of time from sequential method that number of patter is set of set flip-flops is d sequence or in old case that can be a higher than f, f but always this is not in be case but always will be n equal to number of flip-flop. So partial scan chain can be part of your scan chain approach and your time from expansion method advantages also it will take, this sequel number is less than number of flip-flops. Then you can use less number of patterns to set the dissenting flip-flops. But actually if you remembering the scan chain discussing single based to set a flip-flop,

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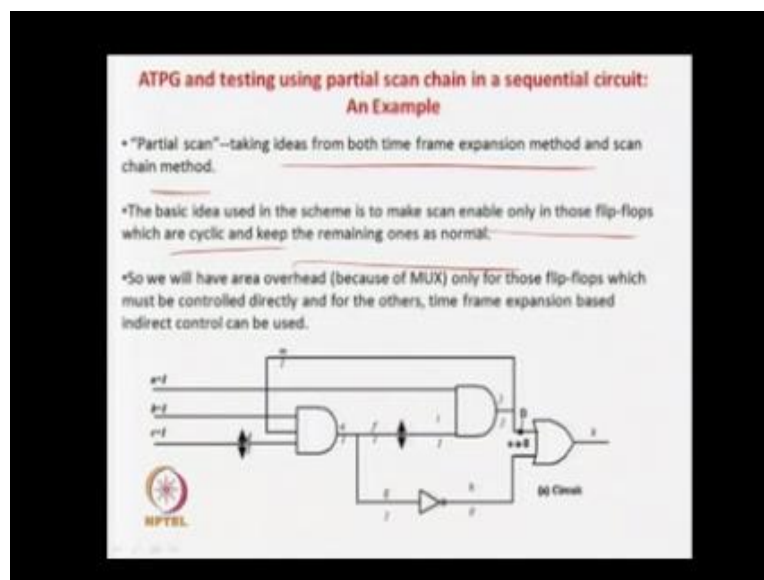

In case of time from expansion method beads it is not patterns sate of especial it is compensational very expensive so we will take a advantage of both of them and see what we can do so again elated by examples. So partial scan taking ideas from both time frame expansion

method and scan chain method the basic idea used in the scheme is to make scan enable only in those flip-flops which are cyclic and keep the remaining ones as normal. So what is the idea? The idea is we have already seen the example of the extra gate, extra gate what we have seen if your extra gate is cackling your extra gate so the extra gate can be control and fall cannot be tested. For that case it is mandatory is that to be have a scan to direct to the set of flip-flop.

But for other cases you may not have a scan chain, it can be control in to time from expansion method. Because the time from expansion method the offline complexity is high there can be clashes all those things are there. When you computing what patterns equal to complex the time from expansion method offline compression approach but we said that the computation is very, very high, why it is very, very high because that can be classes that to be vitiate.

But once somehow you found out the pattern in the number of pattern is use to control the flip-flops it will be must less n. But in flip-flop you may not control the flip-flops for that you require bits. So you will find clashes are 0. But if n flip-flops you have to use n patter to do this it will be control. In real time testing in chips are there so you require n number of pattern to set it.

But in case of partial scan or dynamic expansive method you require only d sequences number of pattern to do this. So primary expensive method you do lot of in the offline but when you are going for online testing for that you are chip is best when you do institute testing you save less time which is more important of introduction class. So people decided that taking advantage of both.

So we will give chance to those flip-flops where is very difficult to more cycling flip-flops control you cannot check all the circuit all those important steps are there, there you have to mandatory put this flip-flops because you directly to control these people, but for other cases if you remember where you can control by timer in expensive method you better use that because offline compensate is there condoling flip-flop beets do by pattern in terms of time line expenses but still number of expansion pattern is less. What is the basic idea n based by the example,

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ATPG and testing using partial scan chain in a sequential circuit: An Example

- Two flip-flops are to be controlled to 1; net d is to be made 1 and net l is to be made 1. Making net d=1 is simple and can be achieved by applying c=1 and a clock pulse.
- Control of net d via F1 is by time frame expansion method; as d_{seq} =1 for F1, so one clock pulse and one pattern is enough to control it.

So let us look at this circuit there is two flip-flops are here so somehow I have removed has been done. So now you can say that so what we require 1 over here d over here it will be 0 over here you require 1 here that is the well-known fair 1 require over here but big problem is to get 1 now this is the cycle bees. If you want m=1 you need j=1, more over there if you want m=1 defiantly j=1 needed and to get j=1 you need m=1 so this is the line a cycle.

So want you have to do is you have to do partial scan chain, what is partial scan chain that is you have to somehow get this value to be =1. So if there is that you have to use the time frame expansion. So let us see how we can do this. First what we do first make a scan chain, this is your scan frame this is your non scan frame that is also we called as a partial scan chain this is your partial scan what we do you need to make m=1 and we apply an m1 in a clock pull what it will do you will get a I=1 surely you will get.

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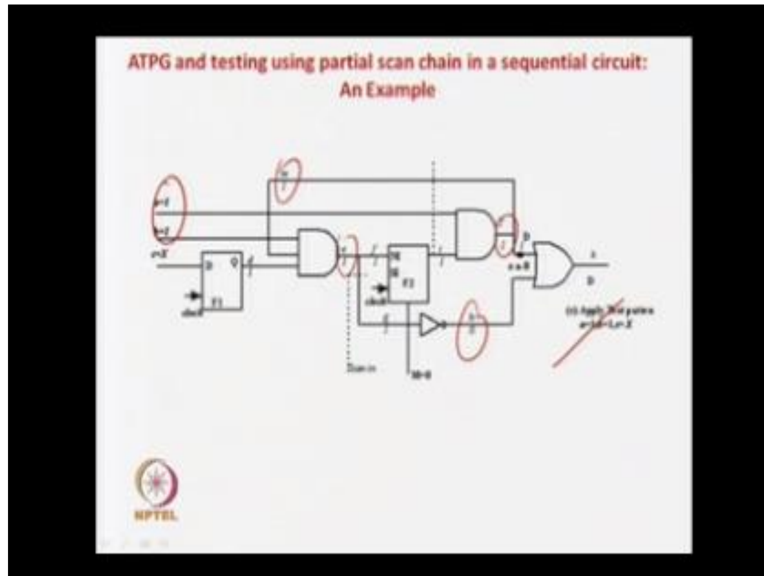

Next what you do that has what has been done to make M=1 apply a clock pulse to get a 1 over here that is what has been done over this case correct this is what I was saying that. This we control by time frame this is controlled by scan frame. Now what you will do m=0 normal fashion now what you will do 1 over here for that there is no scan chain that already said using time frame expansion method. So in this case c=1 and apply the clock pulls what is going to get a 1 over here that is very obvious but now her you get a 1 over here you get a 1 over her and then you apply a 1 over here and 1 over here so if you apply 1 over here you will get a 1 over here and then you get a 1 over here if you apply this you will get a 1 over here so this is a 1. So finally this will also be 1 this will be a 0 and your circuit is going to be tested.

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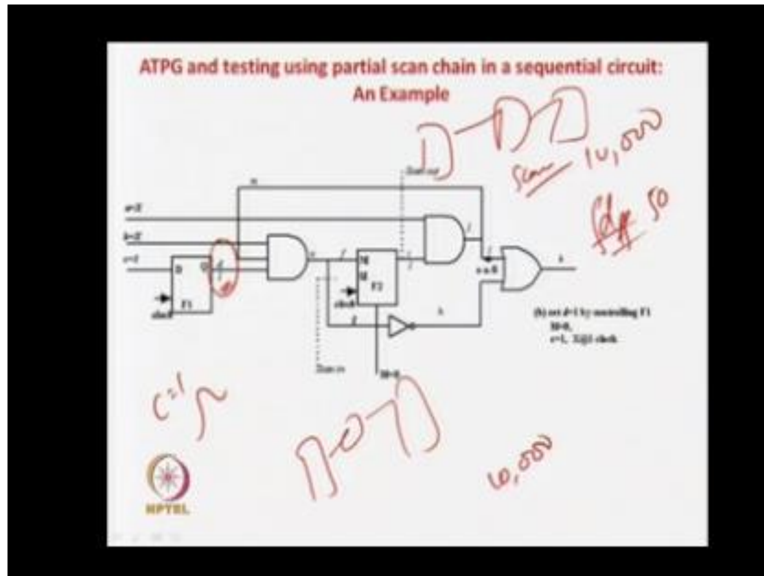

So essentially what we have done so in this case you do not see much advantage of you this is direst primary input flip flop. So you do not get directly get the advantage of what you can see or what I am saying to highlight. What is the basic concept which in was going to discuss on the partial scanning you have to see a bit more carefully so what is idea we have seen, that if there are say if, if you use a direct scan chain approval so what would have been there would have been 10 flip flop.

Something like that so all have been connected there are 10000 flip flops interchanging so what you have to do. So you require 10000 clock pulls as required correct? But let us assume that the sequential dept that is DFF the sequential depth okay. You say for this you save 500 so what do you mean by that all the flip-flops are not compassion by the circuit this is the scan what you have to do you have to connect all the flip-flops.

You remember all the flip-flops connected in a chain so if there is n flip-flops you need to do n pattern of two sets. If there is one flip-flops here you need to do one pattern flops if there is another 10000 flip-flops are there you need another 10000 flip-flops okay. This particular circuit less than that normal apology you consider not be deepened on others like 10000 flip-flop not

depended on the 9999 flip-flop similarly 9998 will not depended on the others that is not in this case. So what will happen some of the other flip-flop depended on the others so in the average case you have to take10000 or 1000 or 800 something less than that that last flip-flops depended on the others. There are some say 500 flip flops that are common circuit. So this 5000 flip flop are dependent on the previous and so forth.

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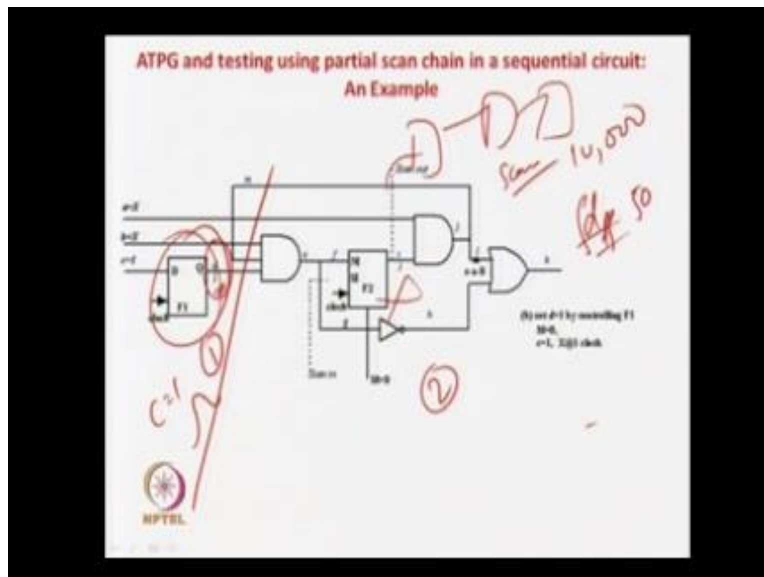

Another separate single chain is like this so the sequential depth will be deferent or the maximum sequential depth will be most less than that, so what you can do is that all those flip-flops did not directly controlled by the flip-flops we keep then in the time frame expansion method, this case you consider this is dangerous flip-flops is sequential flip-flop depth is 2. Because this is outwardly depended on x1 here the depth is 1 all sequential circuit depth only 1. So what you have to do you require one pattern to test it. So there have been for example let us take a example so at just 10 at this is OR gate with,

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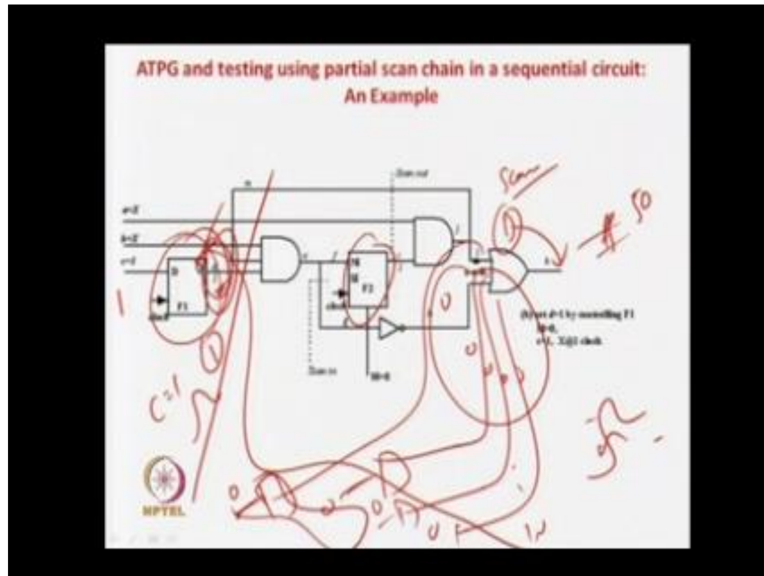

Other flip flops so other 10 flip flops are there. Let us consider this okay so other 10 flip flops are there say 10 flip flops others are connected so this one all other flip flops are there. So I have 10 flip flops are there, and there are connected to the primary input. So what is the sequential depth is 2 for this one because this a dangerous flip flop kind of a thing because it is a dangerous set of the circuit so it has feedback. So it is controlled by scan no option about it so done. Now what we are considering this and all this 10 flip flops what is the sequential depth is again 1. You know this flip flop id dependent on primary input this is primary input and so forth.

So if you require a scan chain to set all because this is a OR gate to propagate the value do D over here so all this output should be a 0. So in a scan chain then what I have to do you have to make a scan chain from this entire flip flop. So then we will be level flip flop in series so you require clock pluses to control this one. Because all the flip flops here are dependent on the primary inputs. So what you have to do you have to apply in this case in this a 1 is required, so you apply a 1 over here or 00 you apply. And we apply a single clock pulse so this is for time expansion method that means 1000 10 0. So once you do that you will get the output of 0 over here and 1 over here and your testing is done.

So have you been using a scan chain so you have to control in this way but if you are directly using what you call a time frame expansion method then only one sequential depth is one so you will do one pattern to it. But here it is simple that all the output or the inputs of the flip flop are primary inputs the controllability was easy. So you can have a common circuit and you have to do some more computation to do it. So what are the advantages of the partial scan we have got.

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The partial scan chain advantage what we got is that you may not require n number of patterns to control the flip flops. So that point is also solved so what we are doing again it is not you are not being able to solve all the problems. So what is going to be the ideal situation the ideal situated that we have totally time frame expansion method we could have already have taken scan chain best approach and then we could have solved that we do not require n number of patterns to set the flip flops.

But that will not do because if you want to use a scan chain approach then, then the advantage is that you do not require doing the ATPG on the circuit. If you want to use scan chain totally the scan chain get advantage is that don’t get the advantage of scan chain you can take depth of the nearest flip-flop and then you can apply your test pattern do your ATPGs for small circuit and

take out the scan flip-flops and then it is done but again setting the flip-flop recording the value out of some flip-flop and again brining to the scan chain you require number of flip-flops.

So this one we have been now there will be a lot of trade of so you can think that I will keep only few parts of some because if once the scan chain goes very, very long then you can have some problems. So you can think of again for hibernate that some of the circuits some of its flip flop is even if there are I mean the non cyclic I can go for a scan business because time span expansion methods many be too high in complexity. But so much we see but we just see the question and answer session.

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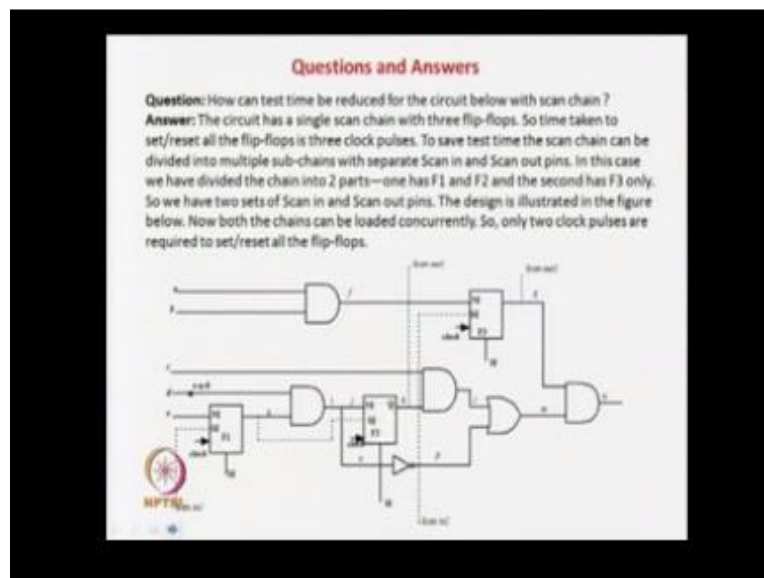

After these questions so two approaches one approach is full scan based technique and another one is partial scan approach and what do we call partial and sequential problem. So there can be third approach we will see so how can test time be reduced for the circuit sown below? Everything will be scan based so how can you reduce the test type? If there is flip-flop you need 3 clocks pulses set to the flip-flops. So there can be other flip-flops. How can you reduce it? You can say that reducing this business what we can do?

We can go for a time frame expansion. So time frame expansion method what is the depth of the sequential circuit for this is 2 this is depended on the flip-flop here the sequential depth is 1 and clock sequential depth also 1 because this directly controlled by this 1. So you requires to pattern to set of patterns are require.

But for that you can tell that because this some because in that case we go for time frame expansion method then the controllability will not be just by 0 and 1. It will be patterns they will be equal to control in the offline complexity. But still you require only 2 patterns to set the flip flop. Then people have gone for third approach in which they call it multiple scan chain in what case is multiple scan chain, do not make a very long chain why we require 3 pulses is to control it? Because they are 3 in chain, you can ask why you are making so long scan chain. Because directly avoid time frame chain because of the meth medical complex chain.

So what we can do is make multiple scan chain, so what is guy is done he make one scan chain over here another scan chain over here. In this case what we do there is two scan chains parallel over there. So in this case there are 2 patterns 1 here and 1 clock pulse we load here second pulse we load here and parallely with this we load this. So it is under flip flop over here 2 can be loaded here. So if you make 10000 chains so you will have 1000 flip flop chains in one go we require patterns to flip flops all we require.

So we do not require 10000 patterns to the flip flop only for 1000 because we are loading in parallel. So there is one thing that is greater than one we have that approach which is now widely accepted people generally do not go for what you call this time scan expansion method and partial scan. What people do that the go for multi scan chain because when in time scan expansion method is very difficult to do that two offline with clashes and you do not require patterns you do not require patterns to control them and so forth.

So what people will do is we go for multiple scan chain so the break long chains into partial scan chains and you load them. But there is a problem so if I say that you make 10 chains then you require 1000 patterns to bits to control them so let us say I make 1000 such chains so this 10000 will bring 10000 flops were there so I bring 1000 chains so you require 10 flip flops per chain.

So you are very happy so you require only there are each, each of these chains are these are 10000 flops. You check 1000 chains so if I made 1000 chains then what is going to happen if you make 1000 chains. If you make 1000 chains say 1, 2, dot, dot, dot. So take 1000 chains you make so each one will have 10 flip flop so only 10 patterns are required so your job is done.

But again we are having a big problem that is pin out problem is coming for each scan you have one scanning pin and one scan out pin so you can assume that but for again for each scan chain you require 2 pin out extra. So if you have 1000 scan chain you need 2000 pin hours extra. This is very difficult, and always shades of so you can think that I will make say around 50 scan chain. So there will be 100 pins so in a very, very complex chip you can say 100 testability may be okay. but this for higher rates so it will be 10000 by 50 if you go so you get it around you will get it around 200 clock pulses to maintain that always there is a question about what you will gain and what you will achieve so either you can go for totally time frame method if there is no high flap method it means you are the best.

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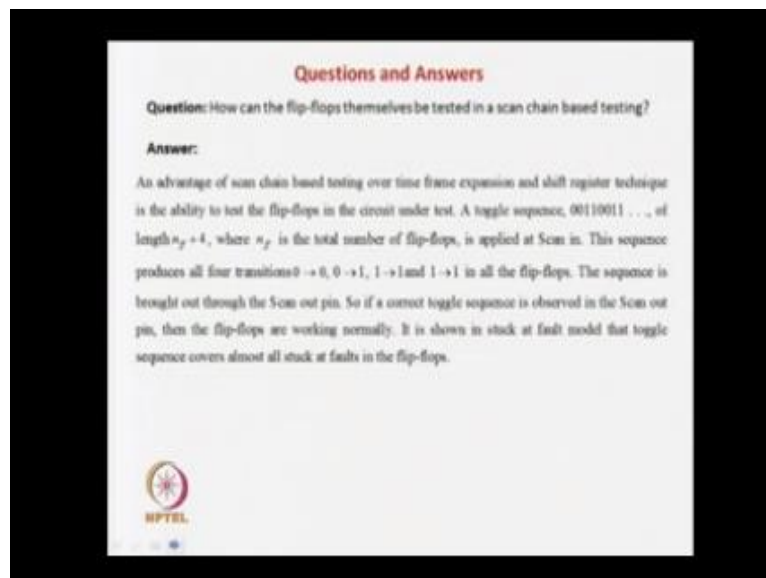

Now non extra circuit less number of circuit test patterns to over this again offline complexity is very, very high and you require patterns to do them. And then you are going for full scan chain

method then you have to go for single scan chain method requires n number of pattern is to set the flip-flops. So more test time is there but here the chances of collision is almost 0. Because we will take small steps of the circuit part of this scan chains inter stability and small circuit and then you require n number patterns to do that. Then you can go for this partial scan what you can call scan chain.

So there are here again it is of scan chain and what you call time scan expansion method complexity is there. But you can go for simple approach you can go for n take up the long scan chain to take part. It is a very good method foe two small scan size of the more number of scan chains you are bringing out by breaking the larger into very, very small number of there is large number of scan chains and the poi out we have.

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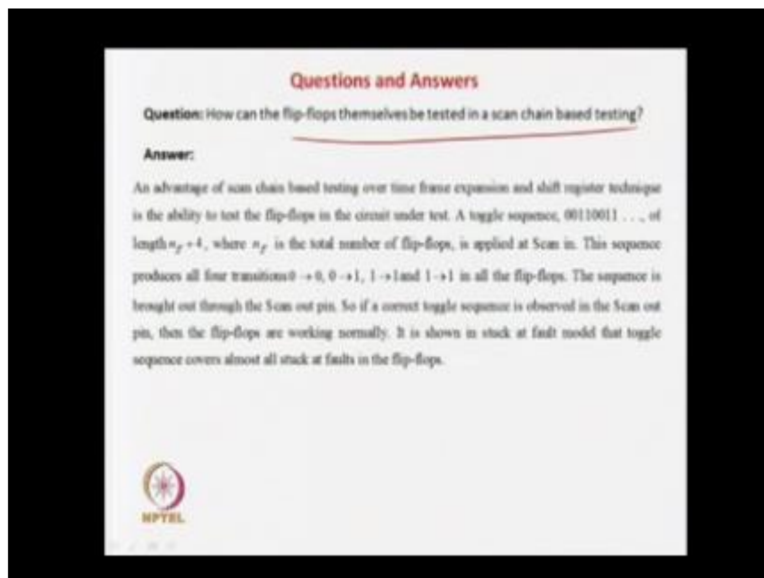

And you have to select and worst out of it which you have feel pest of this that you have to decide. Next question is the how can the flip-flops themselves be tested in a scan chain based testing? There for remember all the chain based resting over time frame expansion and shift register. So that we assume that there is no fails in the flip-flops, but still you have to test the flip-flops how can you do that? Scan chain easily do that still if you want to test go to scan mode

if you want your test flip lop only then you just go for the scan mode make m=1 do not think about the m=0. Do not do that make it only scan chain, then pass these kinds of sequences 00110011 are all alternative sequence. So there is 00s 11s 10 01,

These type of sequences you give then you can get these type of transitions 0-0 0-1 1-1 and 1-0 if you get it then your flip-flops you get them correct you know that you are flip flops are fine the flip flops are tested. So scan chain in the end and the data advantage of scan chain is that you can test the flip-flop. So again there is very good design one of the best designs that had been developed. So I will say that it is scan chain because it is solved most of the problems. That is related to your sequential circuit testing harmonically chain

So with this we have come in to end of the model and this lecture in the next module and the next module are reaming and testing what we will see that so next we have seen that offline testing scan chain testing or whatever discussed. So patterns are tested and once you have tested the design so it is fabricated it is replaced on the tester your tester will apply that patterns which you have determined for the lectures we have discussed.

So paths and patterns are decided so those patterns are applied on the automatic testing you get the response and you say whether the circuit is normal or faulty if it is normal it is shifted to the customer otherwise it is thrown out. But now say for example you have send you chips now it is put in laptops or put in the video camera or put in the pc what you are using again it may go back, because all the chips suffocated happen during operation it may have some failures.

Now how to test them there is something called build in self tester so whenever your circuit starts operation so it will be testing itself right so that is one important value of testing so that is one part which we are going to see and also there is one thing which are not considered that is the memory. We have considered sequential circuit we have considered commotional circuit we have considered but we have not considered, third very important in our circuits which is in the memory so in the next few lectures we will be looking at build in self test and memory testing which will be complete our course on this testing so, thank you.

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