INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

NPTEL
NPTEL ONLINE CERTIFICATION COURSE
An Initiative of MHRD

VLSI Design, Verification & Test

Dr. Santosh Biswas
Department of CSE
IIT Guwahati

Module X: sequential Circuit Testing

And Scan Chains

: Scan Chain based sequent Circuit

Testing – 1

So welcome to module 10 lectures 2 and 3.

Design Verification and Test of

Digital VLSI Circuits

NPTEL Video Course

Module – X

Lecture – II and III

Scan Chain based Sequential

circuit Testing

So this is on Scan Chain based sequential circuit testing so if you remember in the last lecture 10 of module 10 so what we have discussed we discussed that that sequential test and circuit test as compared a combination circuit testing using the D algorithm since they propagate and justify approach. So what we are seen that in case of combinational circuit you sensitizes comprise and propagate and justify so one pattern is enough to detect a fault but in case of sequential circuits, what we are seen that the basic architectural of sequential circuit you have some primary in puts.

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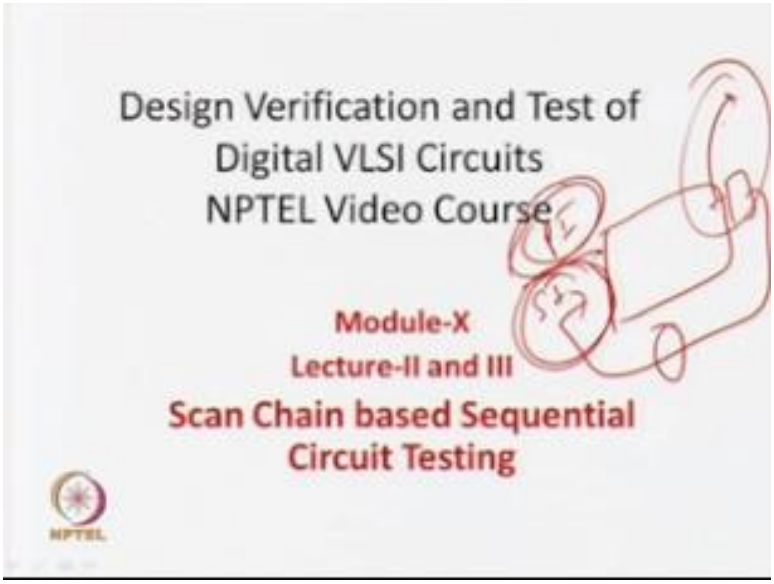

And there is a state register and there is some feedback from that and actually this is called as secondary inputs or virtual primary inputs so as this set of inputs are non-directly controllable. Because the output of registers so you cannot have a single test pattern test the circuit because you require a multiple number of test patterns to precise if the sequential depth of the number of flip-flops in the circuit is sequence, then you require a D sequence of test pattern, to control worst case to control all the secondary inputs.

Now once they are controllable then you can apply the primary inputs and test your circuit similarly the output is also not directly observable, so to make it observable directly so you have to again propagate some values through some of the flip flops you take another set of time so single test pattern we already seen is not enough to test a sequential circuit by sensei propagate and justify approach.

First you have to use the sequence level of number of test pattern to control the sequence secondary inputs then apply the primary inputs so this sequential number of patterns plus one pattern then again also the output the propagate the value of these out puts to observe them. So more than one number that is de sequence plus one or some plus km number of test patterns are

required to test the sequential circuit and also you know that, we are going for this ATPGS test with sensei propagate and justify test and many times you lag to in consistency so again you have to back track you can assume that sequential circuit testing is order of complex city of combination circuit testing into number of test patterns to be applies you also discussed in the time flies method.

Then you required minus de sequence to zero level of time frame that is de sequence number plus 1 time frames are required to do this you can understand that in last time frame average type are successful but in the last time frame it will inconstancy then the whole work is gone then again to start with refresh so because of this inconsistency today we will see what we can do so that this over all complexity of more than 1 number of test pattern can be avoided or can be minimized in sequential circuit testing so effectively what you have to do some how you to directly or indirectly control and observe this secondary inputs and secondary out puts respectively. If you can do that there are problems is solved. So let us see what we will do, so as in introduction we are discussing.

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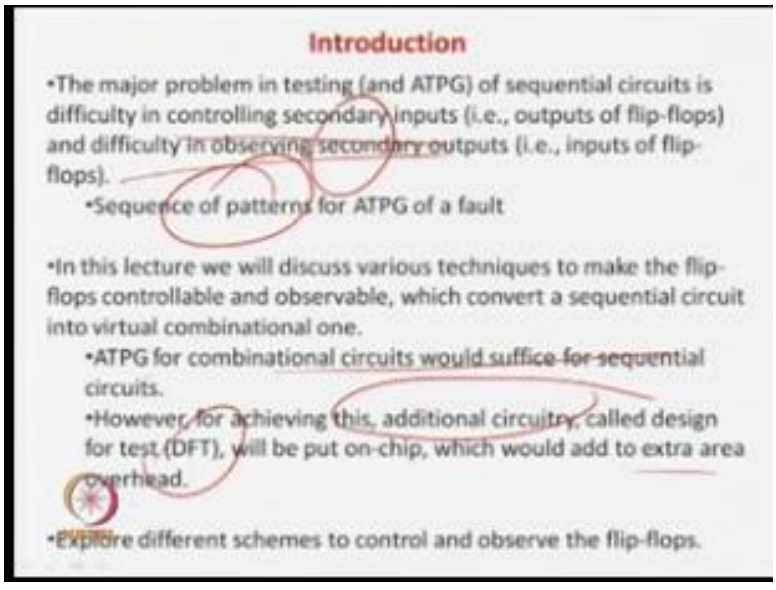

The major problem of testing of sequential circuit is difficult in controlling in secondary inputs and observing in secondary out puts, so somehow you have to do that design for testable or some other arrangements you have to do so that why you requires a sequence of test patterns for ATPG of sequential test, which you want to make one kind of thing. So in this lecture what we will do what we do in this circuit level so ATPG for combinational circuit is for sequential circuit that is somehow you have to use ATPG algorithm and D algorism for combination circuit and do that an s say that it is done for sequential circuit and the parts which you have control.

Indirectly will use some other technique which is actually called scan chain used as we say to control the indirectly okay and this is one example of scan chain design were coal on coat simple designs are great. So if we are doing a complex design with lot of flip flops and with lot of gates are there are very chance for the designs are in proper or in efficient but good designs are always simple that is coat on coat thumb moving VLSI if you design is very simple and you solve the problem the you are a greatest engineer so great designs are always simple so you find out that how nigh mare problem of testing one fault you require D sequence of number of patterns to test a sequential circuit was solved by a person who develop scan chain and his design was extremely simple.

This is one proof you can do very elegant proof simply so converting all the sequential circuit into combinational circuit and combination circuit ATPG algorithm applies for everything and the so solve it we can do it this sequential this pattern generation we type frames and all so they loss their importance and combination ATGP with design for this ability is modifying the circuit so that you can directly control the secondary inputs and secondary outputs observe ability indirectly using some kind of extra circuit then came in to picture.

So but for that to achieve that you have to put some extra circuit on the chip which is called DFT that will be extra over it but anyway that extra over it problem is not much.

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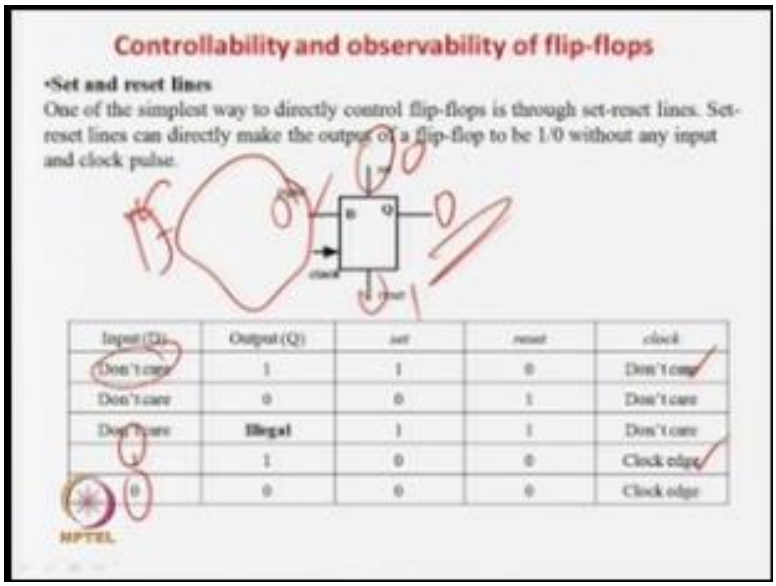

As we will see than compare do off line head ache for one fall generating this sequence number of test package so how do that so one major problem we have seen in the last lecture was to control the output of the flip flops which are nothing but a secondary inputs so how can you do that so one very simple way of as you already discussed at in our lectures we are using this Flip flops.

As they are standard user all dslr circuits so one way indirectly that is directly or indirectly without using except test pattern directly you have to get the access to this flip flops somehow and you have to control them so if you want to indirectly control them you can apply de sequence of test pattern and go for time frame and you can do it but here what we are saying that this indirect control we have to do somehow directly you have to access all the flip flop and you have to do it and you can understand that if you get some of gate hold of that set and reset the pins of flip flops then you can always what you can called take control of flip flop we see the example if you can directly some of get access to the set and reset input of the flip flops then you can directly connect them over 0 or 1 As required for secondary input so if that time you did not go for this de sequence number of test patterns to make this secondary inputs controllable indirectly.

So we can use that so what is the true with this of the flip flops you can say so if I make reset = 0 if you say a set =1 you say then you are going to set your flip flops so what is the idea input you do not care at the time because you are directly controlling the flip flop set and reset and clock is also you will not require you will directly get the output qs 1then if you make reset as 1v and set as 0 then what will happen you directly get the output of the flip flop as 0. You did not apply clock and all those things.

So somehow if you set and reset lines externally then you can directly set this secondary in puts as you required and 1 and 1 for the set and reset is not allowed because it is a illegal condition but now if you have to operate normal in your flip flops then you set reset =0 if you apply a one you apply a clock age in next stage you will get a 1to this flip flop you apply a 1then you apply a clock age your set and reset should be 0 in next clock age you, will get 1b and 0 for the same case if the input is 0 then output is 0 this is normal operation of flip flops.

But if you to clock pulse to control this flip flops then inputs will have lot of combinational clouds so you require sequence number of test pattern to set this inputs so you get desired output as 1 so if you have to get a 0 over here indirectly you have to set a 0 over here for this you have control flip flops and so for so for which you require D sequence number of patterns okay now you can somehow control this and this then directly you can reset and set =1 output as 0 which is required.

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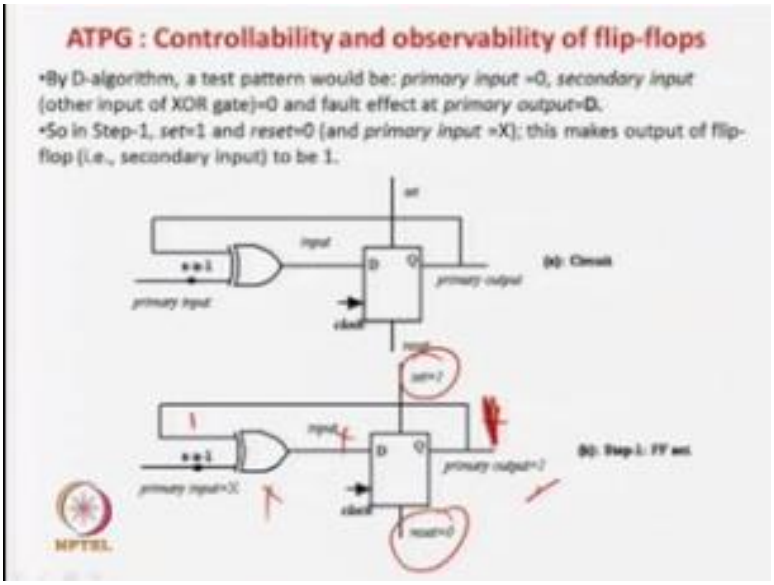

So let us what you gain by this you can directly do this so if you remember the in last lecture we said that this was a circuit and you can think that set and reset lines were not there so the idea was that we asking can you test this fault then you find out that if the set and reset line is not there it was in the question of the last section then this part cannot be tested because you know that the this input and this output is X for this. Kind of a thing and for this stacked one you have to apply a 0.

And if you that is 0/1 and in the case of XOR gate output will be a X or X' because a x 0 = 100 get the output is the output is whatever is input or output and if we apply a one over this for the s of fault this x will become x' so it will be x and x' so never you can get any complete value and you cannot ever test your circuit so that was the case. Now we can see that use of this set and reset line if you have then what can you do so for example we know that all the lines x for the time being so this is X and x and so for so what do you do so I can do is that

Now we can show u makes it set equal to 1 and reset equal to zero Set equal to zero so what you want to do that so without applying the clock also you this output in one output is 1 and the output is 1 because you have set the flip flop directly, okay using set and reset okay now stacked

one so what you can do is that so you have a one over here never one over here so and now this is just what you have done first if you apply set =1 and reset = 0 so you get 1 over here you get a one over here.

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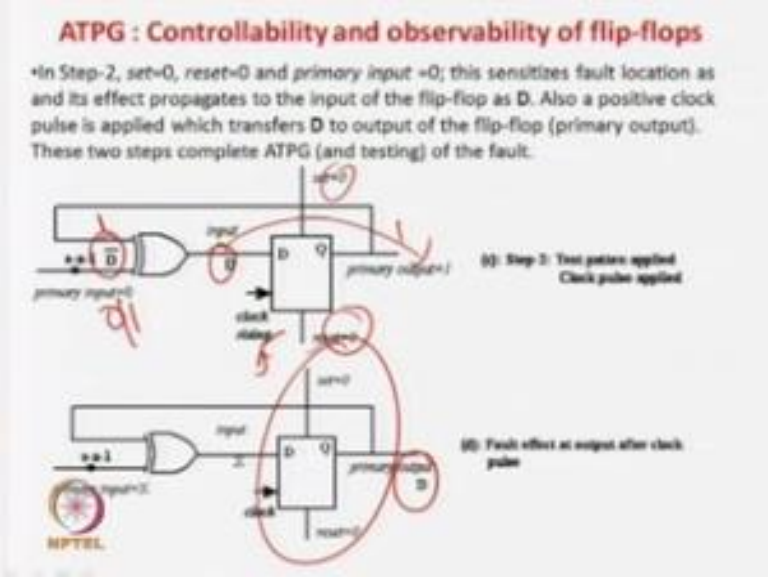

Now what you do you make set and reset =0 now so what will happen now this de flip flop will be operating in the normal clock mode so 1 over here so what you have to do you can apply primary input 0 so normal case 0 fault case one because of the stacked fault so here is a d' over there and you know that in case of XOR gate if the other input is 1 and second input is prime is inverted so you get a D over here now what you have to do so this set and reset you made 0 now you apply a clock pulse over here so this output will come over here as primary output which will get here and the fault is tested in the primary output.

So what we have seen that the fault which is not testable in the first go without the set and reset lines now become testable when you are using a set and reset line so this deal the great problem some of the faults which are untestable. If you consider you circuits without the flip flop without set and reset lines now become testable secondly one more thing is that that we see in the other example.

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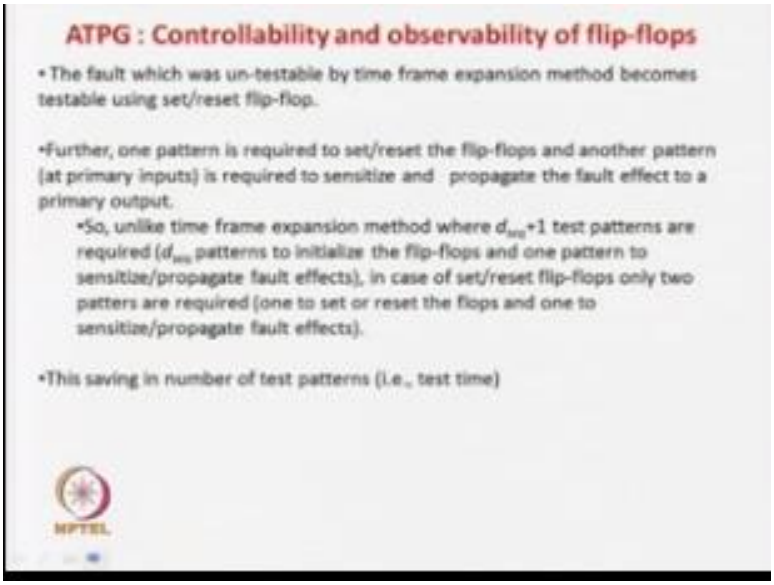

So what are advantage of controllability and observe ability of flip flops with reset lines of all is untestable in time frame expansion method in last lecture is now becoming testable using set secondly so what we have seen that only one pattern we will see only one pattern is required set and reset the flip flops and propagate the output so the idea is that if you look at it so only one pattern that actually you can call that set =1 and reset = 0 that is one pattern which will set the flip flops because there is more number of flip flops set and reset is required and there only one pattern will drive your answer to this one.

So indirectly what you are going to have if your set and reset like in your flip flops one pattern will be required to set and the re set of the flip flop as required for your secondary inputs and secondary output kind of a thing secondary input control ability you can directly get wise setting and resetting flip flops directly with that pins and now one pattern is required to apply which will sensitize se the fall and propagate the output some flip flop kind of a thing so instead of D sequence pattern initialize the flip flops so unlike time from expansion where you required these sequence one pattern to what you call sensitize and justify.

So in this case only one pattern is solving the problem or you can call to only two basically one to set the reset of the flip flops and one to actually sensitize the fault level that is by the combinational test man algorithm.

That is this pattern actually this is your applying a one 0 over here so this pattern is by combination ATPG and the other set reset you are doing by this one sorry this set you are making as one and two this is the other test pattern, so two patters are required to solve your problem so this actually says the number of test pattern and also the test time.

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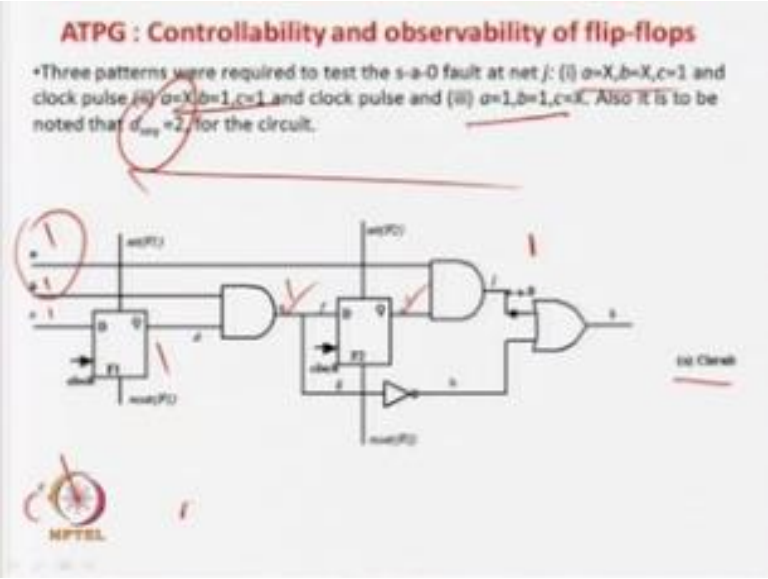

So what we have done by the using the set and reset lines we have solve one night mare problem we are actually going towards combinational algorithm to test sequential circuit so now instead using d sequential order or d sequence of test pattern to set the secondary inputs and then what you are doing g then again we come back to apply this D algorithm final pattern to do it so now you are controlling what we are doing now we are directly controlling the flip flop out puts that is in secondary output.

By directly setting the set and resting of flip flops now you can directly give the patter required to testing so we rustically changing the order to 2 from order d sequence plus 1 to order of 2 so this is a very great help and slowly we are moving to our aim we are converting sequential circuiting to virtual combination form of circuiting for testing and apply combinational test pattern like D algorithm and solving the problem now simple and last example so now go back to the big example which considered in the last lecture.

So if you remember this was our circuit this was our faulty and there were two flip flops so if you remember when you have done the D algorithm so we require a 1 over here also 1 over here to test the fault we require a 1 over here also 1 over here so if you apply 1 here so you get a 0 over here so effect is D over here and this effect d over here we require a 1 over here also 1 over here some like this was a scenario if we look back last lecture you will understand.

Now the main issue was here that how we can this was the secondary input as well as this was actually a another secondary inputs okay so because this is the output of the flip flops so somehow how can we indirectly control this so in this case in the last lecture we have seen that t we apply 1 applied a clock pulse and the value came over here after that we applied 1 over here and this one already there we applied another clock pulse this 1 was retained so this 1 again to be transferred.

So all this discussed but we require two patterns two set and to get 1 and 1 over here we require 2 test patterns c=1 was here if you see c=1 was required and a clock pulse then b = 1 and c=1 we require to set this output and then finally a = 1 and d= 1 we apply to test this pattern so 3 patterns were required to this pattern to test the fault that already we have seen.

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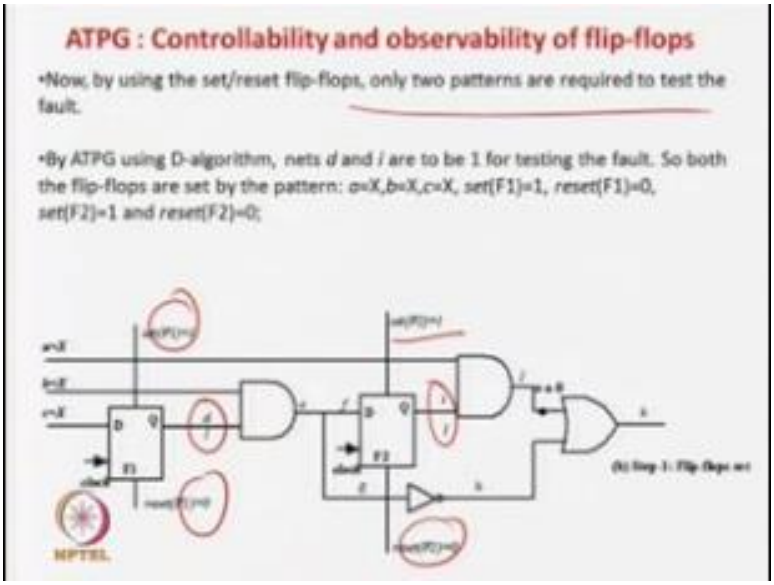

Now let us see how can you reduce this using set and reset lines of flip flops now you know that we require 1 over here we require 1over here so instead going for a time frame and actually time clock pulse what we will do will make this one as 1and this as 0 immediately you do that to get the output as well because to set the flip flop for the other flip flop also you make set = 1 and reset =0 immediately you an 1 so now your job is done so what we are doing only two patterns are required to do this one pattern to set the flip-flops and another one to test it so you make this and this so this output and this are set.

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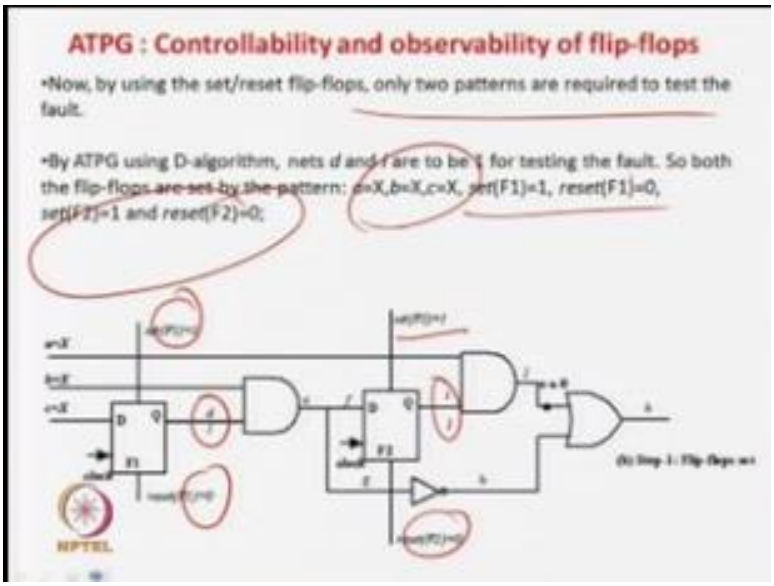

Now what you do you gate a 1 and 1 by resetting this now you have to go for the normal operation of the flip flops so you make the 0 that is the normal operation is done now you make a=1 b=1 if you do that so you will get 1 over here and 0 over here this will 0 this will be 1 is a 1 over here also 1 over here. For the NAND gate you get a 1 to give d as shown as 0 and your job is done so you require two test pattern one is to set the flip flops this guys a, b, c so you to set the flip flops.

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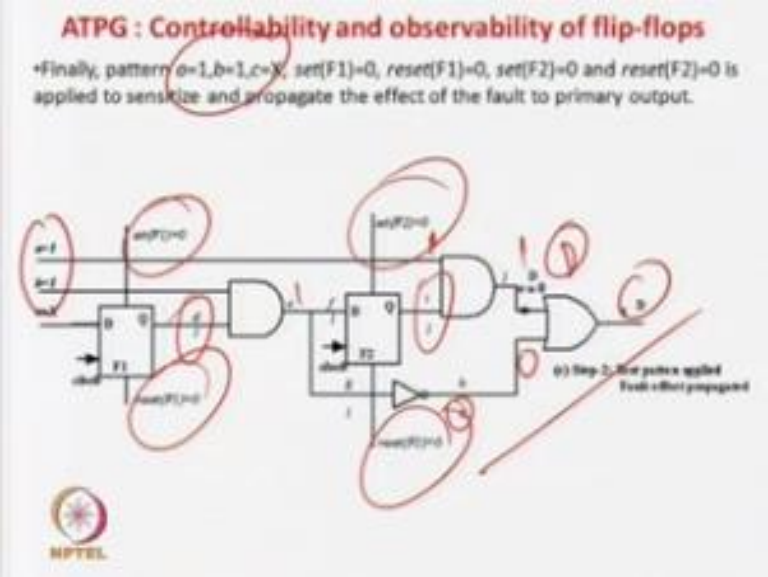

Then the next pattern you keep you just apply this pattern and your job is done you have to remember if you 10,000 flip flops only two patterns are required to solve the problem.

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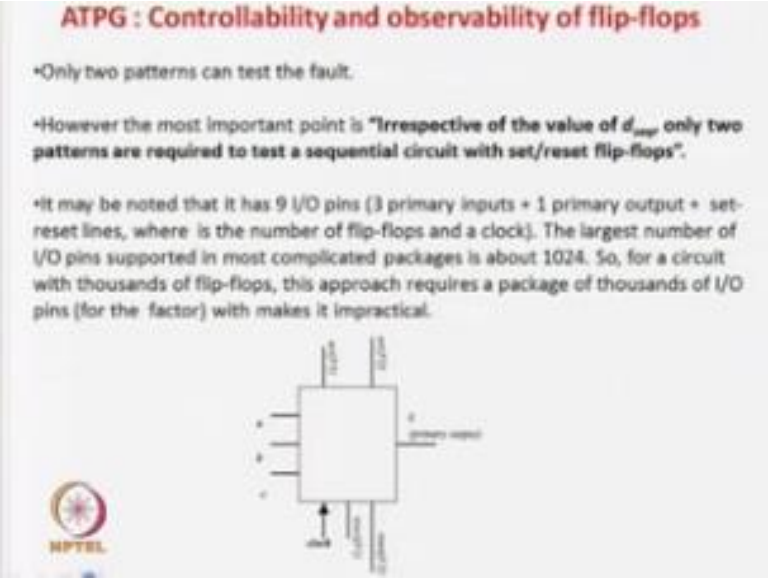

One pattern will be to set and reset the flip flops the other pattern will be for what the other pattern will be just you can see.

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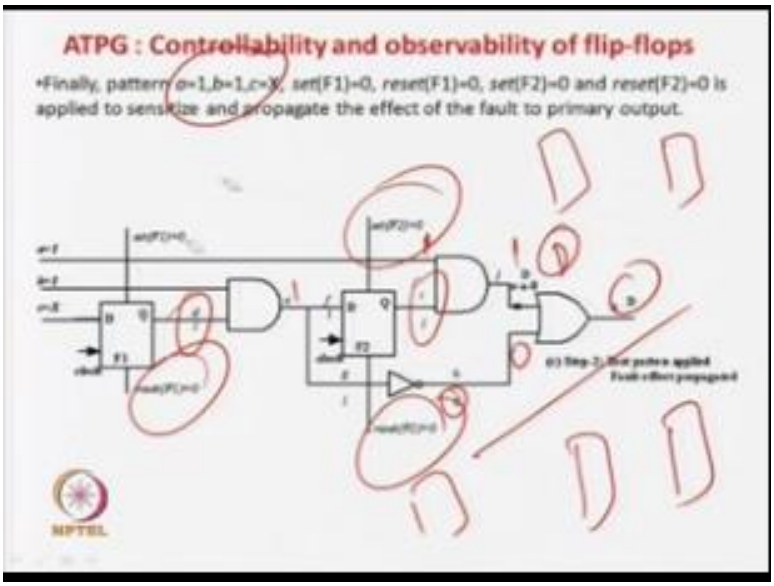

Even if you have another ten flip flops is there then also you did not worry why you did not worry because in case of time frame expansion method what was happening let us see back what you are doing so you can think 2 flip flops over here and two patterns and idea is not that the idea is if it is 10,000 flip flops again 2 patterns is required to solve the problem say for example you have some 10,000 flip flops some other stuff is there so for.

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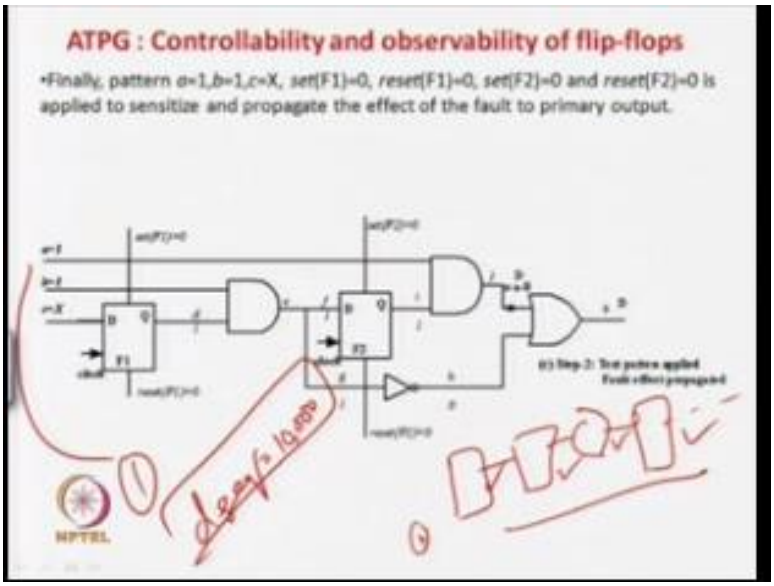

So in your time frame expansion method then one pattern will be required to set this so 10,000 flip flop this so your d sequence is equal to 10,000 then you are in a big problem if you have a 10,000 flip flop in these sequence you require 10,000 pattern to solve the problem set the primary output of the flip flops primary output of the flip flops are nothing but there are you secondary input so you have to do that and the one pattern will be applied here to test the circuit.

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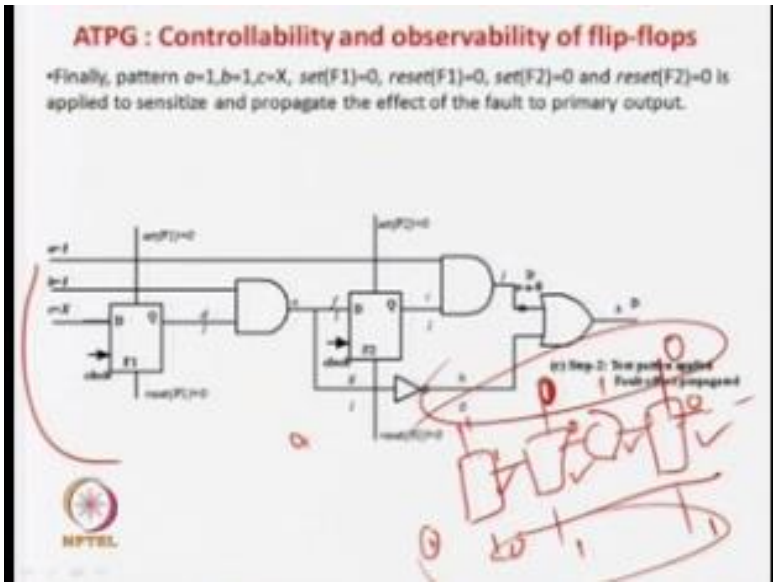

But now if you are having a direct access to the set and reset lines then what you can do to get 1 over here make set =1 and reset = 0 if you to get 0 over here make set =0 and reset =1 and similarly if you want to again get a 0 over here make reset sorry set is = 0 and reset is equal 0 and all this things you can apply parallel these all the flip flop will be individual control level you have to assume and then your problem is solved. So two patterns are done for this one.

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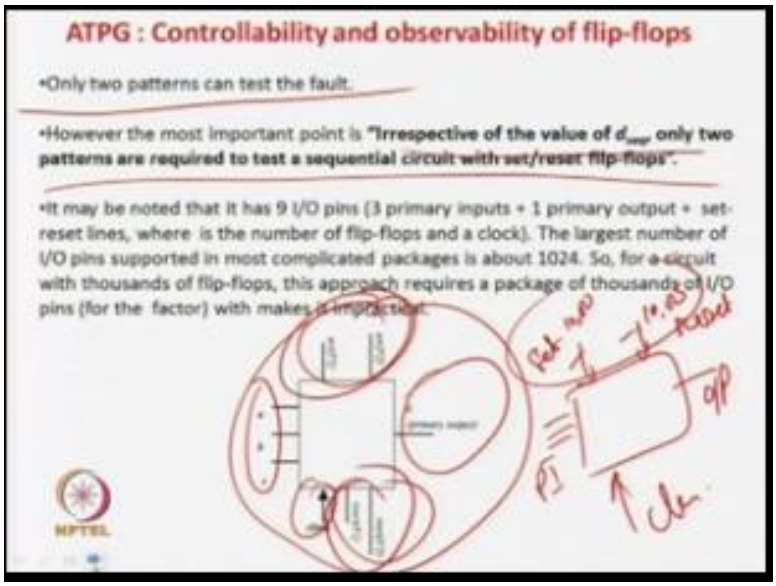

Now you see what you gain and what you lose so gain is only two patterns to test if n number of flip flops are there what may be the sequential depth no need not to worry you job is done only two patterns are required for that but most important point is irrespective of the value d sequence Most important point is irrespective of the value of the sequence only two patterns are equal to the tested sequence .The greatest boon is that if you converted a circuit from a sequential circuit of archival component circuit and you are solving your problem. D Algorithm is doing everything for you need not go for the triangular expansion and all these.

But if you look at the block diagram of this circuit this so we just getting the block diagram so these are A,B and C were the primary inputs and primary output is there. And two set lines for two flip-flops and two reset lines for necklines. If you think that I have ten thousand flip-flops, so that it will be the primary input and this will be your clock. And there will be ten thousand set lines for ten thousand flip-flops and ten thousand reset lines for the ten thousand flip-flops. So now you can see the complexity.

So ten thousand set lines and ten thousand reset lines are there to do the problem .And you can understand that maximum number of output of primary input and output can be maximum 1024

or 512. They are very expensive to get a package like that where you can have 512 to 1024 inputs. Now, if you have 20,000 inputs such packages are not available and you cannot do a circuit like this. So we have gone one step that we have converted a circuit to a virtual combination of circuit and solve the problem.

Now the night may having in a started that this set and rest lines are too many in number so how can you do that.

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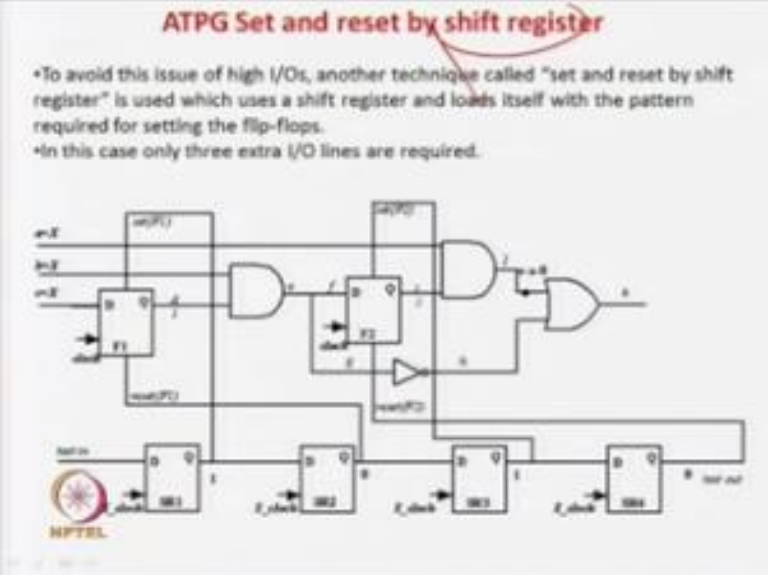

Then the engineer started to solve the problem. Then we cannot have we did not use concept of set lines and reset lines and we will control them but how can you control them by bringing the so many pin outs .So bringing so many pin outs is not feasible because you do not have package. Packages are in IC's where black packages are there. This is called DIP (Dwell in Line Packages). So there are silver pins and all, so many you have seen we have seen around 14, 24 may be some 30 or 40 you might have seen for micro point circuit and all but 10000 to 20000 pin outs almost impossible and not durable at all. And also we require a ATE .We have also discussed about ATE in the very first lecture of this testing module .We require 10000 to 20000

pin outs of the ATE, which is also very expensive equipment .Then the number of probes to give inputs to the 20000 pins is also not feasible and this idea is dropped .

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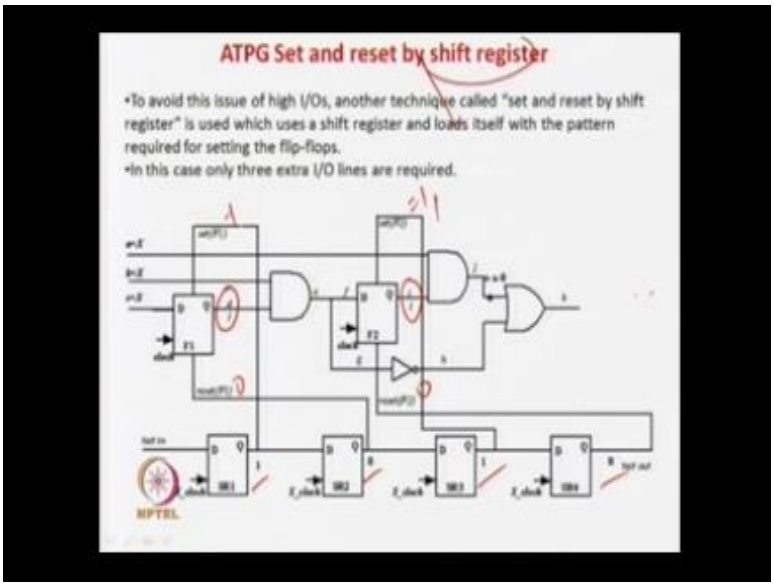

So now the problem they have found out was the same example we are going to check. We require a one over here and one over here. That was the requirement .For that we have to make Z=1, Z=0, Z=1 and Z=0 that was the requirement. Now what problem we have the problem is that if you want to bring this four pins .So 10000 to 20000 pin outs will be there. But people have said we cannot have that many pin out. Some people give the idea that you use what is called a e Shift Register Brass Technique. Now what is a Shift register technique so in case we just want to minimize the pin outs. So you will have a set of what you call and the Shift registers and have a set of registers and a set of flip-flops which is connected in a Shift Register kind of thing.

So 1, 2, 3, 4, there are 4 pin outs and we require 2n number of scan or Shift register. So this is the idea for so you are ready for either flip flop so there are 16 in this case. That will be the idea now what you do so that is our problem you are having. So now instead of being this pin outs, it will be connected to the output of each pin of a shift registers. So now you see there are two flip-flops and a shift register of four flip flops. If there are four flip-flops in the main circuit, we will have

eight. Now the first output of the flip-flop for this shift register will be connected to the set lines. The second flip-flop output will be connected to the reset lines.

Similarly, the third output of the Shift Register will be connected to the set lines of the second flip-flop and last flip-flop output will connected to the reset input of the second flip-flop .Now the required connection is done. Now we require 1 over here and a 0 over here. A 1 over here and 0 over here. And now what we have to do you can say that is you require 1 at the output here one 0 here 1 here 0 here, because now this input and the state you are not driving externally from anything okay. So we are not driving by pins.

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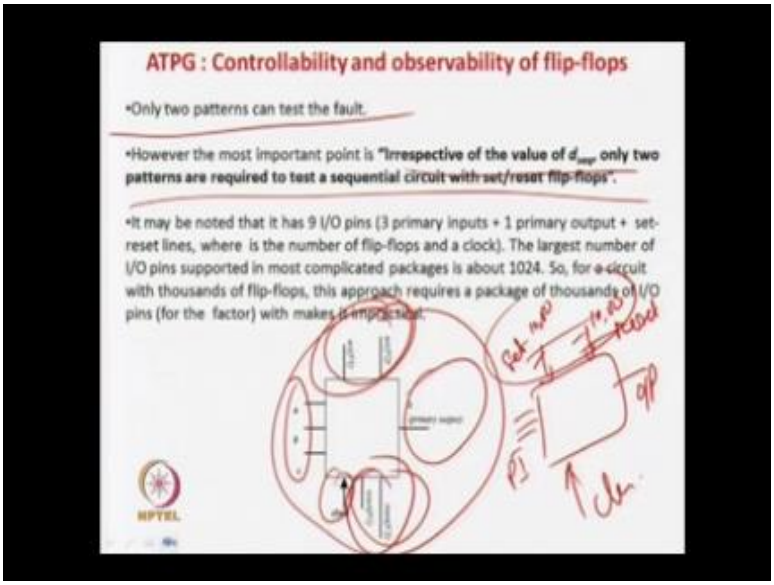

So if you at the last line of the lecture, there were external pins and you could apply them parallel. That is one go you could apply all this flip-flops but for that what you require you require a circuit or the chip designed for 20000 flip flops so that is the input 20000 say extrametrical problem. But in one go you have controlled all the flip-flops outputs directly. In Shift register in one go you cannot have 1,0,1,0 directly. In one shot you cannot have. So we have to apply 1 then clockwise 0 then apply the clock wise then how it happens. So we require four iterations to do this. So first you apply 0 over here, this is the requirement so do not go

about this is the requirement so first you apply a 0 to your clockwise now this 0 will come over here correct.

Now you apply a one over here okay a one over here and now you apply your one over here and you have to rename that all these clocks are same and these entire clock are different. It is very important to know this is a circuit level and this is clock. So two clocks are now coming into this. Now you give another 0 over here and give a clock pulse. So now this 0 will be coming over here and we will get a 0 over here and 1 will be here so now you get a 1 over here and a 0 over here these are actually do not care now we do not know what is value it is. Now you can add a 0 over here and you give a clock pulse, what is going to happen is this 0 will be here and this 1 will come over here this is the case.

And now, in the end you apply a 1 here and give clock pulse. So, once you do that its 0 will come here, this1 will be coming here, this 0 will be coming over here and this 1 will be coming over here. Now we have 1,0,1,0 which was equal. So we require 1 clock pulse, 0 clock pulse, 1 clock pulse and 0 clock pulse. So four clock pulses are required in this case to shift your value required to control the input of the pin. Now, if you have 10000 flip-flops now what is the case you require 20000 clock pulses to control this answer is correct that you have to do. And also we have seen that the ATE is very expensive you cannot have a you cannot take the 20000 input time you cannot have or it is very redistrict to do. But this problem they have found out that is still remaining if you look at sequential circuit testing.

To minimize these number of clock patterns to test the fault. Somehow they are using fault collapsing because you have already seen that fault collapsing algorithm to minimize the number, number of faults only those things they will be doing to minimize the number of faults but filling or shift register. We will see the scan chain is the motivated version of this will be seeing in next lecture .But anyways this 20000 number of pattern in, in this manner cannot be done .So this number of clock pulse will be required to shift the pattern here which can indirectly access to set and reset lines and conclude the output of the flip-flops.

But now there is advantage in solving the problem. This is clock for this circuit and s clock is clock for this shift register. Now these two clocks are cape different .The idea here is that if you look at this clock pulse it is driving one AND gate and again the output is driving a invertors. So, whenever you get the data, it will take some time for the value to be propagated over here .So, you cannot have a very fast clock towards this one .Because whenever you apply the clock pulse the data will come here and to get the data here may be we can assume an another flip-flop over here to then this change in data should be arriving over here .And another clock is used to trigger this flip-flop. So it is a long part so this output will be there this is and gate is there then the inverter is there and the or gate and then the data will come. And there is some delay of the data travelling from here to another flip flop.

So this clock period has a limitation in aped you cannot go for a very, very high speed clock over here and so allow but if you use the shift register so this output is connected here this output is connected to the input and so on. So there is no devote is once the clock come around here immediately the data gets transferred this input of this flip flops there is all lot of combinational cloud over here the you have to wait for the data to be coming from here to here then only you can apply now this is not the case here the output is directly connected from this to this the output is connected from this to this so your problem is solved. So you can apply a fast clock over here compared to this clock so this filling up can be done in a fast rate even for 10,000 flip flops even if you 20,000 pattern to set or reset again your problem is not high.

So in 10 Mg Hz clock you can use 500 Mg Hz clock or something like that generally you can also use giga Hz clock over here and very quickly shift the data but this will be slow there is lot of combinational varies here. So the number of test patterns is 2 one is to set and reset all the flip flops apply the pattern and done it the set reset lines has to fill up in the sequential manner so number of test pattern required is 0 1 clock 00 clock 1 clock that will take around 20,000 cycles if there is 10,000 flip flop but that can be done in a very fast rate and one more point you have to remember over that. So you may ask the question that so 20,000 patterns are required to shift the data here.

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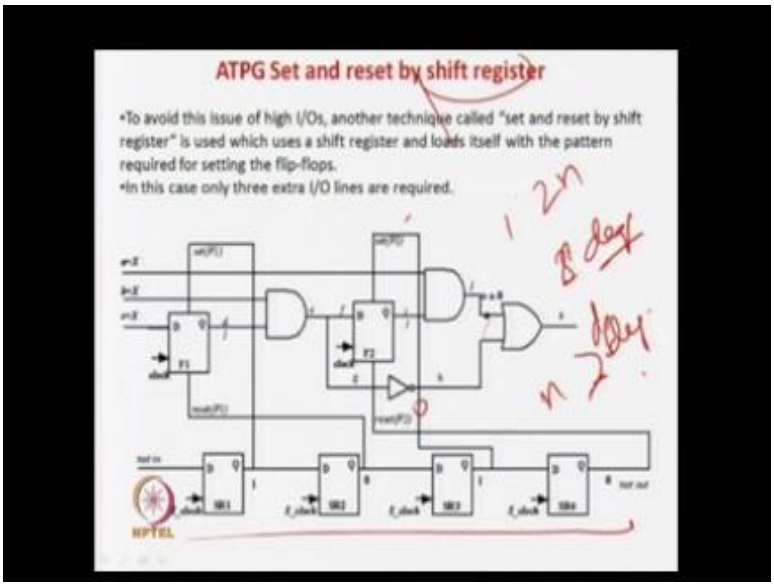

So you can say that there in flip flop and 2 n patterns are required to control this set and reset. So you can also say that from time frame expansion method also we are having the same thing if there is sequence of flip flops then what you have to do you have to apply in d sequence time frame method all the flip flops are set and you apply this and you know that if there is N flip flops so here 2 N pattern I mean 2 N series are required but in case time frame expansion method only d sequence series number of patterns are require you know that the D sequence is less then equal to N because if all the flip flops are tied in to one chain over here D sequence will be 4 but sometimes it may happen that there are minimum numbers that is not all the flip flop depend on the previous one.

So your D sequence is maximum days of flip flop that is equal to or less than so you can say that what you call these time expansion method in this time you control some of the flip flop outputs so it may not be 2n. 2n is actually double the number of flip flops so it is required in the case of Why are you going for this one why we are not going for this you can call sequential time expansion? The answer to this sequential time space, thus is a very complex stuff so why may happen is that in one time frame –DC because you said some of the flip flops. In time frame this

sequence 1+1 is you say some of the sequence but you are not using this so what are you going to apply hoe you are setting up setting the flip flop in case of time expansion method.

So we are using primary inputs only to do that so primary input means you have to get access to flip flops you have to cover some of the combination circuit like for example you are saying that is the flip flop because there is lot of control and lot of communication circuit here. So you have you control this inputs in time scale approach to get a access to this one okay. And in case of this you can get directly access to this flip flop so what may happen is even setting up this shift register take 2n number of times. And which is the D sequence in case of time span expansion method so number of clock period may be very less or less compared to this one in case of primary expansion method but you have to remember that in time span expansion method we get access to flip flop through common circuit. That is primary input output.

So it may happen that after 3 or 4 times you may reduce in case where you may have inconsistency because whenever you want sate of flip flop direct to the state there is no question comes in consistency. You are somehow get to solve by flip flop scan chain or direct out but what you are gaining direct control to the flip flops and there is never any question of consistency that is never you can come to a case that you cannot control the output of this case if you remember this,

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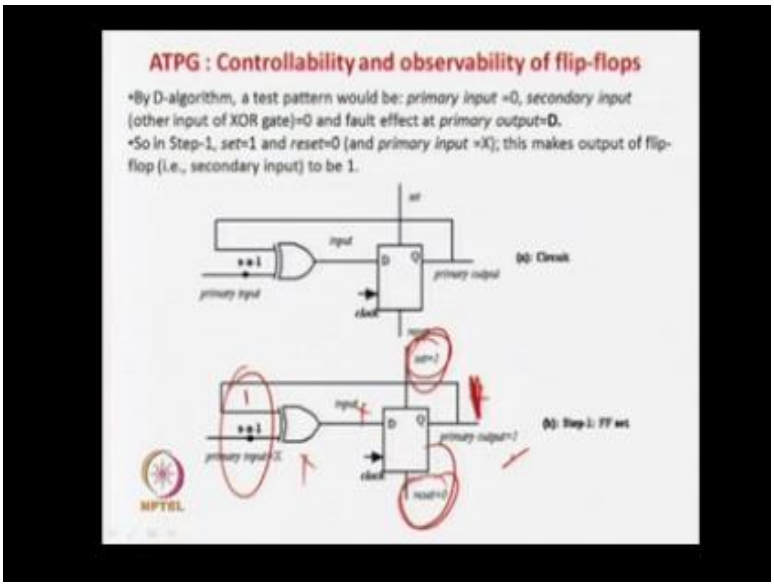

This example like in this example you say that by using time expansion method you cannot change the circuit because using the primary input output you cannot control the primary output but by this register you can direct have this control this in other words this method this is direct access to the set and so if you are using so what advantage you are gaining is there is no question of any inconsistency always you can control the flip flop even if applying 2n number of patterns to set but you will never going to have a inconsistency. So just apply the algorithm get the patterns control the virtual input and you are done.

But say there is very complex in nature that you may have what is the case that you can land up in the problem and that in last time before the success you get some inconsistency and again you have to redo that often come with the so high that the we have moving towards this time span expansion so we are forgetting and going for this now we will see.

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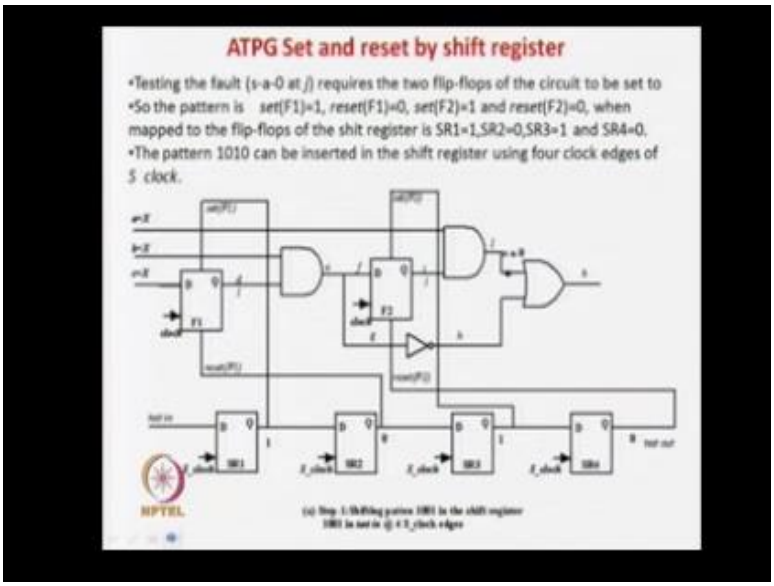

What you call 2n number of patterns to be applied to that so basically we need to add this extra set of flip fop so there 10000 and 20000 we have to put in making a this shift register. So this design is not a very efficient one you have you put double n number of flip flop to test. That was also not very high widely accepted technique so you can see that the this is what I was discussing and how you can test this circuit so this people have 1010 done and applied the pattern like 1010 so this is how you do the testing and the clock you set it and then apply this 11 so in four places. Let us look at this steps so how you do that so this circuit you require a four clock shift 1010 and then you all the set are done.

Now you apply 2n patterns of obviously this clock will be very much faster than this clock now what you have to do the another problem over there more complexity you add so now all the lines has to be 0 because now you want to operate this circuit normally so again this 4 you have to apply by four clock so nor only 2n +2n number clock period are required to set this flip flop required and then again you have to make everything You want to apply one to become zero over here, what we have to apply is zero not only 2n,2n plus number of broad equate, to set the module to equate and again we can make everything normal.

And then we can apply so the huge number of controlling want to become zero, and then actually what we can done is main achievement are the testing we called the most important in case of testing I will say this a concern, then the concern came into the picture and solve the problem forever so and people are following the partially solved problem, that then only two pins set in and set out there is only pin in set in whereas only three pins required but now we can have 2n and plus 2n number of clock to set in extra to set and these extra.

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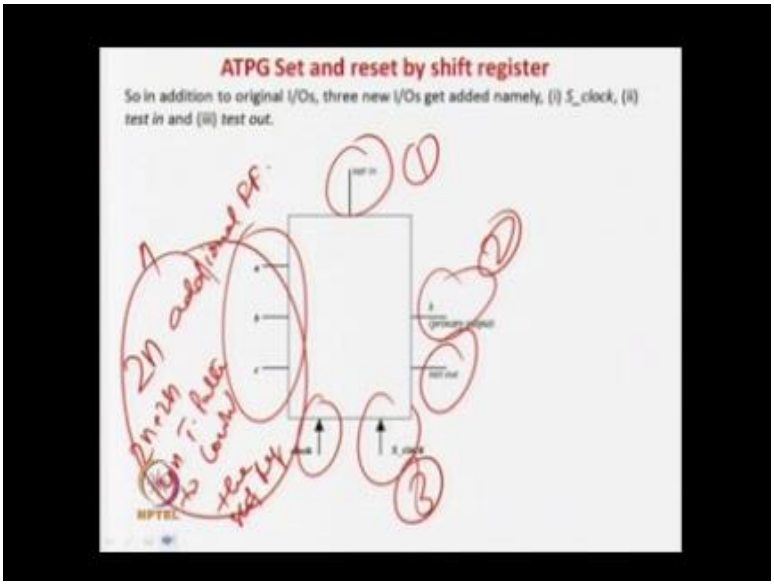

And this shift register has been able to conquering the set and the set lines to get back, but now this actually taking the if there are 10000 to 13000 flip clock so you are having 10 flip clock then we are saying if there n flip clock then 2n number of extra flip clock you have to add and 2n plus 2n extra clock periods are required to control this to this, that is the big problem which is came into this, then so this the block diagram I will say and the testing in and this to test out to extra that the shift register input shift register output and primary output to clock, and additional pin is one is one two and three and in 2n shift clock and additional shift cock you add and you require is 2n plus 2n is 4n test pattern to control the shift register.

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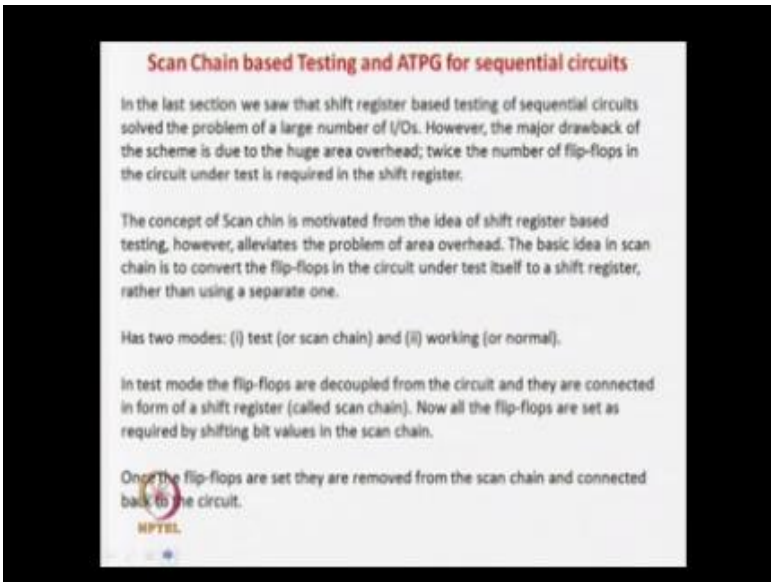

So this is the panel we have to add and actually this was solved by a personal which was a test engineer and can change which we actually can make it solve the problem forever, and which actually call it into condition circuit to a sequential circuit and solve most of this legacy problem whereas pin in and pin out has for set in and set lines and n number of shift clocks for reason so the last problem what will see is potential circuit is huge number of using the diet control, and the last major drawback was to produce flip flop which was want additionally to do that, and also Fourier number of pattern to do that so the concept of scan chain can came so it mediated from the shift register in the Albion register.

So this one actually scan chain main idea came from this circuit only, just have a look at it and then I just see that how scan chain was invented and utilize the official scan chain good design are always simple. So what was this idea the persons idea was you are making an scan chain and chain with some chain but he fail that why are you making an additional chain here we already having two flip-flop are available why we cannot make a chain in this that is the question we have and you have to tell that because you are an engineer and always ask an very simple question to that because we always having an real he sate design paradigm as students so as an engineer's we are and what is our main idea should be that we always ask very simple questions

and always we try to solve the problem in an simple way then we are making it very complex and trying to solve it using an very roundabout way thinking.

We are genius so there is some of different when you are solving an methodical problem and solving an realistic problem these are some coat and uncoated problem if you can solve a problem in an simple way because you require less number of gate less number of power less number of test engineers and we have to solve it in very complex way then it will look very nice design but it will take more power more area and more designer that is not appreciable incase of ASLR. So in this it is a very simple question if I shift register is over here and you are making an register over here why I cannot able to make an shift register using an same flip flop we are already having an flip flop.

In the circuit if I can able to make an chain over here in this circuit then go will be an extra that was the simple question he asked and then he says can I solve and it was solved. And he say that I was using the same number 0f flip flops are already available in this circuits to design the change that shift register chain and there will be two module in the circuit one more will be test mole where in this case all the became the chain that is this mole will be chain shifting this one to control it so if say that in my case this one became the shift register and circuit will be operate already and in the second phase all of you making zero so then this flip flop will not be in an chain and chain will not be there,

And it will start operating in an same way that was the idea can we do that so he actually solve the problem in an simple way as we see, so in test mode what is the idea when shift register are there it will be connected in the shift register that is called the scan chain okay, and when the circuit giving normally the shift circuit are normally and removed from the chain and connected back to the circuit there is two way in one way your flip flop will be change the commercial part of the didapper and all the circuit in normal mode this chain will didapper and circuit will given a normal mode different type let see how is done.

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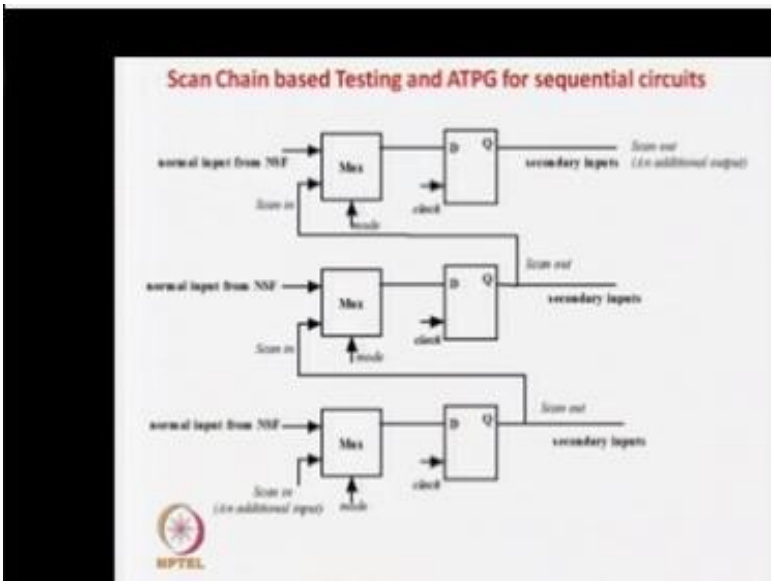

Anything is doable then the problem is solved so what is said is that so we consider that I will have an very special kind of a flip flop same flip flop but instate we will put an multiplexer in policy only that is the only thing he required to make this whole problem solved so with each flip flop now is adding a simple multiplexer ,so in the multiplexer he is saying that let us say that this is the circuit okay, so you can thing that these are normal input from the extra function block so you can have this idea is that so there are some there flip flop and have some input you can also thing this is another hand gate.

These are connected and so forth okay, here you can say that the inverter like this is a b c and d these some of the inputs he is saying okay, this is all outputs you can say okay, you can also say that this is also same input and this is actually a feedback here that is also you can assume you can assume anything, okay these are the connections now what we are say is that now just before if you just forget about the multiplexer the correction will be something like this because how then make the function block means there will be some conventional circuit primary input will be there they will be connecting inputs of the flip flops.

Now what is said that instead of doing this what he has done he just moved one multiplexer he has didapper this the output from this commercial cloud is not connected multiplexer are connected to the system now you say that this have more one and more ones are common and what was the input of the multiplexer one input is normal which is coming from the combination of the part of simpler and the other input is the first one is the additional input that is scan it which is the input is coming from the scan chain normal mode and other is the input of the last flip flop in the chain similarly for the chain in this what we have to do one input is directly coming from the block whereas the combined circuit and other input is coming from the output of the second last flip flop kind.

Of now what we are doing this was the arrangement now what is doing when you are saying that this is the arrangement of the circuit was have ok and we say that this solve it so it is solving that problem is this is actually explaining the scan chain so what additionally he has taken a flip flop so this was the d and q this are the correction so he say that just eliminating for the time so what for the coming you just same thing just put a multiplexer over here you said that in case of zero this will be the connection but in other case of one .

I will have my own input and this is the control line , if the control is zero the normally input was go is fine but if it is one ,then I will send my input the fast taker In case of second flip flop it will this output ,this one is the output if you not we make more zero then is normal connection. Whatever in this side but if I make it mode one Then I will take control of this stay, then let us see how it has done so this is the additional thing I was talking about so this is your the flip flop before that he has put one multiplexer this control for this flop and normal output for this one and it this flip flop.

So this is actually called this a block diagram as scan chain so now we can say as scan flip flop here we have normal input this is scan in that is specially input this scan out block and mode . So if the mode is equal to zero the normally input will be showing if you have mode is equal to1 scanning will be feeding and that are two cases so hours can change normal inputs can input and output is common .

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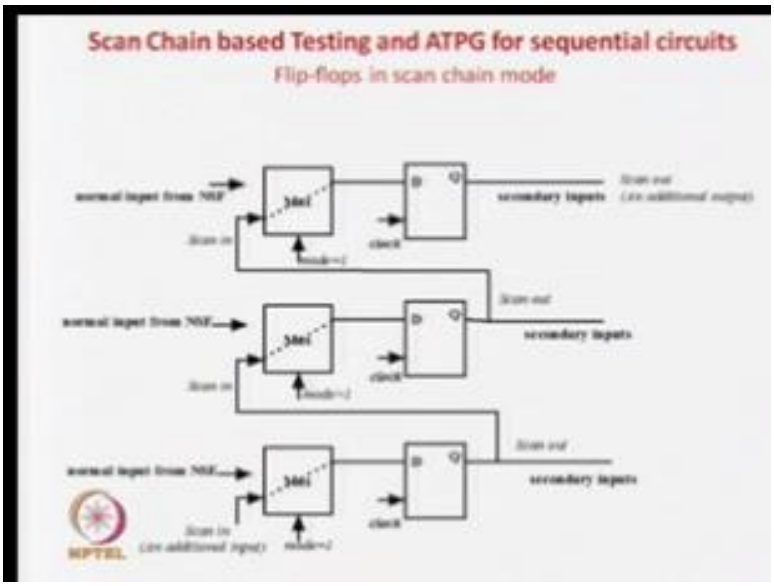

This is the block diagram of this one now we can see what he has done now we say that I want to take control of the whole flip flop okay, I have told you, may have some input like this that is inverter member and variable this one was our inverter so there was some angles over here this is also some angles over here. so short this was seen now he says that for some testing assume that for some testing also this c has to be one to be one and some fault to required that one to be one that is input is c is back over here you required.

This to be a one for some lesson you are okay, other thing distinguish A, distinguish B C and this is D you can called that this D is also connected to this one and you said them I required this to be zero for some fault testing how do you do so what do you require in the scan chain is flip flop is the output you don't required see you required to be one because virtual primary input or secondary input thus to be made one so if the quant ability of this and this also you want to make it to be a zero ok, because this is connected to be pin which is to be zero, solved to do that that so if you do that get the old story that is control reset we said so we have to do you have to make this z=0 and z=1 and z will be zero and z will be 1 and z is don't care. On about it once it is done you will get 0 1 and required that you will have circuit z=0 z==0z=0 then the circuit is normal mode then you can do it so that part is if there 6 flops so what is required is shift flip flop

either three flip flop either you required is 6 pin outs, so you requires neither 1,2,3,4,5 6 extra 6 pin out you required or whether you have to use the shift register.

Which is having 6 flip flops and that line makes neither life very well extra number of pins are extra number of what you call pastry what is the person has done is he puts an extra multiplexer circuits, now we are seeing all three flip flop are barring my circuit then why do want to additional incorporate another flip flop chain to do that we say that when you have to get the value of one over here and one here that required so was these over here so he was wrote here why you should have another extra chain so he said that I will make my mode equal to 1.

So when mode equal to 1 so this input get connected to here .Because this input connected to hear these output this normal output from the outer block is now cut because all the modes are in the flip flop. So, this is connected to this one. So now you see automatically a chain has been developed using this is very important observed that our chain has been developed non buying using any extra flip-flops?

Again I repeat not but using any extra flip flop it has been obtained by using the flip-flop which are developed in the circuit additionally adding some extra marks that So now you make mode is equal to 1 so you get the chain connected. Now we have to apply 0,1,x.z so you apply 0,1,x and you have to apply classes so that why I told you that there not x solved very natural way then how can you mean reduce the number of clock periods to be testing so in this casing c plus control so you can apply 01 x and apply three clock faults so initially zero will be here x and then and we apply one so you will get one over here and x and x over here when you have to get clock also here then will apply anything so change can be on patterns.

So three pulses also applied now what you do this is one and this is x and what you do you know what you do so know again you that some and gate is there and know we have to paste your circuit by applying some patterns now what you have to do so now again make a circuit in an normal way so the state circuit is made for just to make mode equal to zero so once mode is equal to zero will be there in normal circuit input will be going to the output of the input. Of the equal to one the normal connection is there. so here what we achieved in an block diagram.

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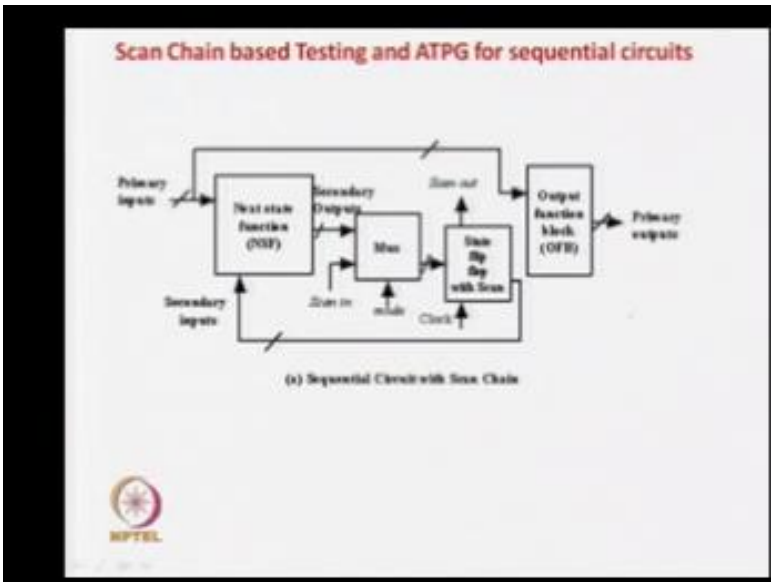

We see this is what required and you see that secondary outputs this is secondary inputs this we have to virtually control so this person has done is mode is equal to zero if mode is equal to zero this secondary inputs are directly coming to the circuits in this case the circuit is operating on normal case now in see what you are doing in this case more you make as one then what happen you can directly control of the flip flops you can control them whatever the value required is one and then you come back and mode is equal to zero.

There will be no chain and normal circuit will be there. You can apply test pattern and the test testing, okay so this was about the lecture of the scan chain and next lecture give about the elaborate examples and advantages and disadvantages of the and so for before closing. one thing have to see is what is the gain we are achieving the gain achieving is now if there would not require n number flip flops and would not require 4n number of clocks and patterns so what we require if we have n number of flip flops then n number and if the size is on is much less than the flops so you just require the n number of and n patterns to set the flip flop so last case we require 4n now we require only n and instead of 2n flip flop we require just n number of flops so we have reduce the problem of delay.

That actually been the path of the sequential circuit what is the base design for the opinion to possible I will be seeing as scan chain so now so it has lot of important problem to solve like timeframe expansion collision or inconsistency and all secondly what it has solved about extra flip flop. so required n marks that is 2:1 which size is much lower than flip flops second you don't require 4n number of long periods to settle down the you just required n number of patterns to reset the flip flop and also you have to observe one thing here flip flop does not require set and are not required over here you are doing.

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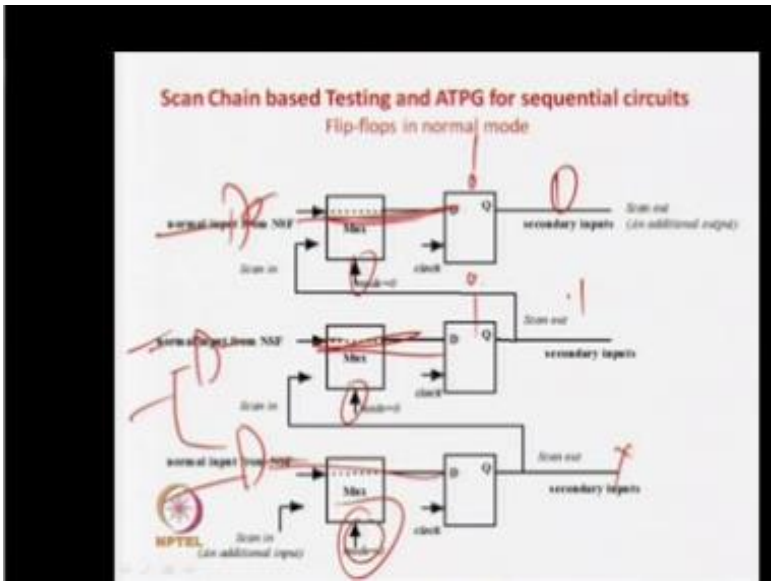

It in normal way so flip flop size can also be smaller than the set reset flip flops so that you can in operate this one inside that. Is you can say that flip flop is set and reset signals then it may area will be larger than a circuit than the flip flop doesn't have a set and reset line then, you can say that mark area flip flop will say is almost equivalent so infect this additional marks is not at all problem you also saying an set reset flip flops so again. we have a great boon we are getting correct and only thing is that n number of patterns will be required to do this so n number of one only problem remains and will not be solved as of now and one more thing is that in case of scan chain this same flip flop we can see same clock here but the clock is operating in two different mode that you have to know which complex is concept. when the flop is activating in normal

mode that is this mode is there then the output of the flip flop will go for an combination clouds will there and its bit case is lower in this case when you are working in the
Problem like time frame expansion collision or inconsistency secondly. what it as solved it solved that you don't need extra flip flop just you require n marks multiplexers 2:1 whose size is much lower than flip flops second you don't require four number clock period to set this which is required N number of patterns to set or reset the flip flops and also you have to observe one thing that here flip flops do not require set and reset line is not required over here we are doing it in the normal way.

So flip flop size also can be made smaller than set reset flip flops so that you can incorporate this one inside if flip flops set and reset signals the it don't have set and reset line then you can think that the marks area you say flip flop line is almost equivalent to flip flop is marks. so in fact these additional marks is not at all a problem so additional marks we are adding that N marks area you are also saving by not using any kind of a set rest flip flop so that is again great boom we are getting correct and only thing is that N number of patterns. To be required to do this that is only problem in the field remains that cannot be solved as of now we have see one more thing is that in case of scan chain.

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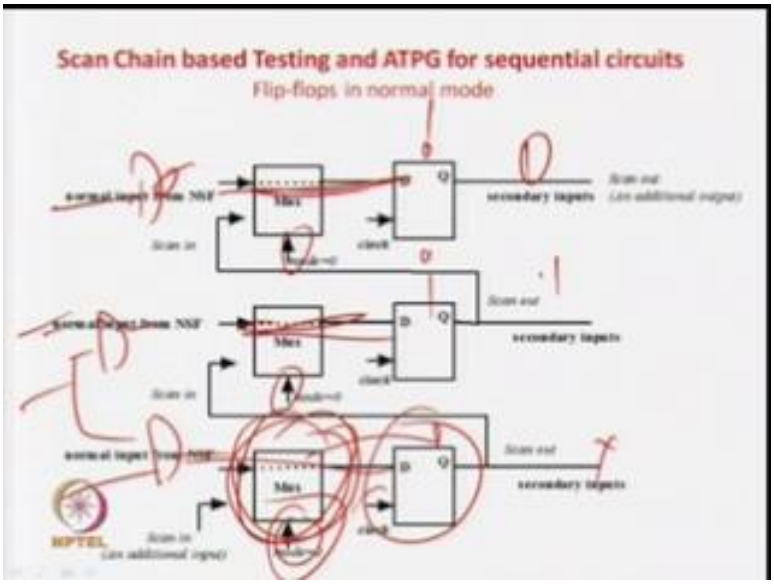

In same flip flop you can see that is chain clock is there but. Now the clock is operating in two different mode that you have to know this bit confuse concept that when the circuit is operating in the normal mode that is in this s mode.

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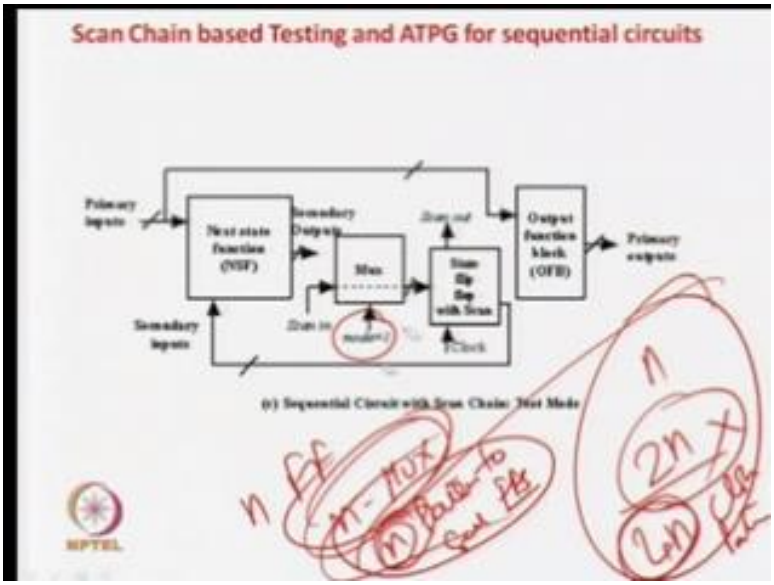

If you can see the circuit is operating in the normal mode if normal mode is here then the output of the flip flop. This lot of combinational clouds will be there and then you can get the output so there is a delay but your clock as to be bit lower in this case but when you are working scan mode then. What is happening this output will no longer there so you're only in this mode so there is no combinational sequence so you can use this clock in a very fast rate? so when you are scanning in the data to set the values in the flip flops you can do it in a very fast rate because there is no combinational delay that much when you are operating circuit in normal mode so you have to do it in a bit slower mode so that combination delay are matched so almost all the problems are solved by this scan chain but only one problem that remains is that N number of flip flops.

In the worst-case N number of patterns are required and number of bits 0 and 1 required to control the flip flop to 0 and 1 that is only problem remains to solve so in the next lecture on this

what we are going to see we are going to see how to handle this N clock period business how can you reduce it this is one mode and second we can see that what are the other variations or other advantage we get in scan chain okay with that we close for this. Thank you.

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