INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

NPTEL
NPTEL ONLINE CERTIFICATION COURSE
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VLSI Design, Verification & Test

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Design Verification and Test of
Digital VLSI Circuits
NPTEL Video Course

Module-VII
Lecture-III
Fault Equivalence

So Welcome to III lecture on the testing part on fault equivalence. so in the last lecture what we had discussed was that for testing a circuit be functional of structural .

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The idea is that we have given a circuit and then it there any input kind of thing so we have to apply some test patterns and you have to find out where is output response matches with the golden response, then or idea was that we have seen that if we go for a full functional testing then number of inputs was 2^n which was quite high and is almost that impossible to apply to the high expensive test equipment's if you have to apply around 2^n patterns.

Then we said that we can go for a Structural testing so in structural testing what was idea was then the bigger circuit of say which had any inputs to break it half into small units which have say some 2 inputs 3 inputs and this have 5 inputs… are some number of inputs and then you test this functional you test this functional as individually functional and that it would be functional test at structural level.

That is your testing this guy for this one and module functionally but you are not taking whether with this interface is proper or not, so this is kind of structural testing at the module level that the module is a small blocks of circuits now the question also we asked in the end of the last lecture has it is modules are quite large in number then less number of interconnect has to be checked like for example if you consider the case where this your whole block which have some in inputs then you break it half into two models which is n/2 and n/2 so then less number of Interconnect has to be test this has to be verified on Idea is that you have to test this one individually.

And this one functional individually and then the structural party is block its then what happens it less number of Interconnect, and also last lecture we have seen what do you call this in Structural testing it is interval for intermediate modules you try to control or you have to absorb, so if you have to control, then you have to put some 2:1 multiplexer or you have to put 2:2 observed in out, so if number of Intermediate lines are less so the number of extra circuitry is less.

But the intermediate lines are small that means modules intermediate modules which you have testing structural level the modules are large in size and the ratio which n decreases may not be large might enough right for example you can have n/2 and n/2 so $2^{n/2}$ is not a small number but on the other hand if you make this elements or what do you call this the elements you have to test

structurally are quite small so you have some two inputs here you have 3 inputs and so on some 5 inputs.

So the whole n inputs you are breaking up into small modules and this one you are testing functionally and this one testing functionally and so for so now lot of intermediate were more so you have to put more number of respirators or more number of 2:1 markers and peanuts to have controllability and observe of the intermediate lines.

But now the modules are what you called structurally or structural blocks and now having less number of peanuts so it is actually $2^3 + 2^2 + 2^5$ …… so the number of test pattern that need to be applied has quite less it is $2^2 + 2^3 + 2^5$ and so on…so number of test patterns are smaller because any numbers broken down into small numbers.

But now the last number of intermediate where some come into pitch it so that is what is the answer to the 1st question of the yesterday's I mean in last lecture in which we have asked the question that if the modules are quite large in number are quite large in size are large means the more number of peanuts then what is the problem so the problem is that you have the n does not reduce to in that amount so you have to apply large number of test patterns. But the interconnections which are less amount what you called this 2:1 multiplexer of resistant is to be applied.

On the other hand if your modules are the modules on which you are going to test functionally are which are the blocks of your structural testing are having very less number of inputs then the number of test patterns to be applied is less but on the other hand you have large number of interconnects in between them again so the now it is more number of 2:1 multiplexer peanuts are registered so it is trade off if you are doing this without a fault model but now the next question was that what is fault model in case of fault model so these are circuit and you have smaller module in between them.

Then would do not is this one structurally, is this Structural test with fault model so previous one we discussed the structural test without a fault model so in fault model what we do we just say

that we do not want to test functionally of this whether we want to find out then this circuit should not have any fault from the faultless so we have seen lot of fault model is most widely accepted one because it is simple to handle as well as it can give you an accuracy or would you call confidential of 99.9% and if you are doing Structural testing at stack at fault in the circuit is not having any defect which is as accurate 99.9%.

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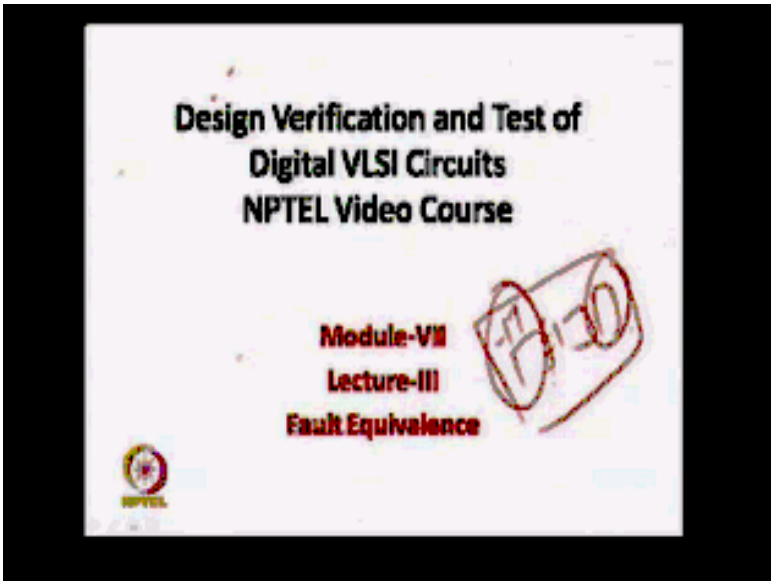

So in this case what happen in this case structural functional Structural testing with fault model if you have bigger circuit modules then you are breaking up into smaller then we can have Interconnect setting of the functional testing then we are not bothered the functional testing of this block or functional testing of this blocked we are hither bothered that this should not have any stack fault similar this stack should not get any stack fault.

And so on and we have also shown that for this it is such a good staff that you need not have a any peanuts extra neither you need to have 2:1 multiplexer neither you haven't any what you called this register extra if you are going to do a structural testing using a fault model so that is why the Second question was thus really a stack model is happen? The answer is no really it may not happening in circuit but what actually happens is the pattern stack at fault is that from 2^n that

is all possibilities you can be applied. We need to apply say that all possible tests factors all the factors you can apply say some K test pattern which is feasible with a tie.

Now the question is which K test patterns you have to apply among this $2^{n.}$ 2^n is the larger set full super set and then among them you have to apply only some K amount of test patterns. Now which K actually stack at fault tells you which k to apply it will say that apply stack at fault for an example we have said that if your given an AND gate something like this then you say that stack at fault here means 2 inputs if you test it 1 1 and you can verified the output to be 1 then answer is 1 is correct else stack at zero fault is there.

So this 1 1 to takes a stack at zero fault is here you have applying 1 and 1 so that means the stack at fault is implying that you have applied this factor so each stack at fault implies one test pattern so if you have n n and n number of pairs then we have seen that utmost you can have 2 n number of stack at faults that means 2 n number of patterns where 2 n is equal to K number of patterns so the stack at fault is giving you very good subsets of 2n which is to apply then you are going to say a 99.9% sure that the circuit do not have any defect.

So stack at fault has such do not appear but they give you a guideline with subsets of test patterns to apply that can give you very high confidence so what will see in today's lecture in today s lecture we will see that if there are n lines then we can assume that we have 2 to the power stack at fault that is one stack at zero and one stack at fault but today we will see the infact much less than 2^n because some faults are equivalent that means more than one stack at fault will be tested that means will require really the number of test patterns require to test stack at fault is much less than 2^n.

So 2n is the extreme fully functional test then 2^n that is equal to the test equivalent to your structural test with fault model 2^n is one line stack zero at one stack two 2n comes to the much lower number so then what happens is the very low number test patterns say p in number have confidence of 2^n test with 99.9% + accuracy. So we will see again the beauty of stocked fault model that not also 2^n it is much less than 2n test pattern has to be applied.

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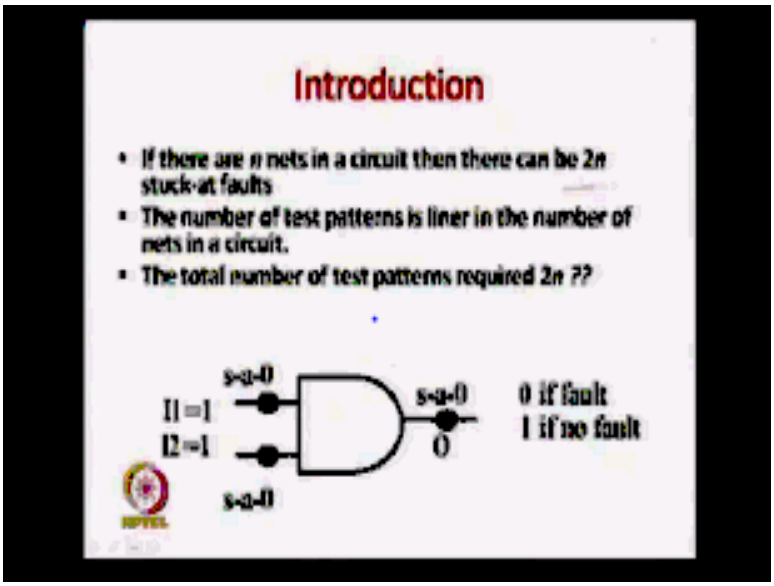

So today we will see how it is possible so whether I told you if a circuit has a 2n bits so there can be 2n stack at faults so it is linear one test pattern for each fault so the number of test patterns is equal to 2n which is much less than 2^n or in other words the number of test patterns request to test all these 2n faults are much less than 2n one pattern will test multiple circuit will be tested by a single pattern.

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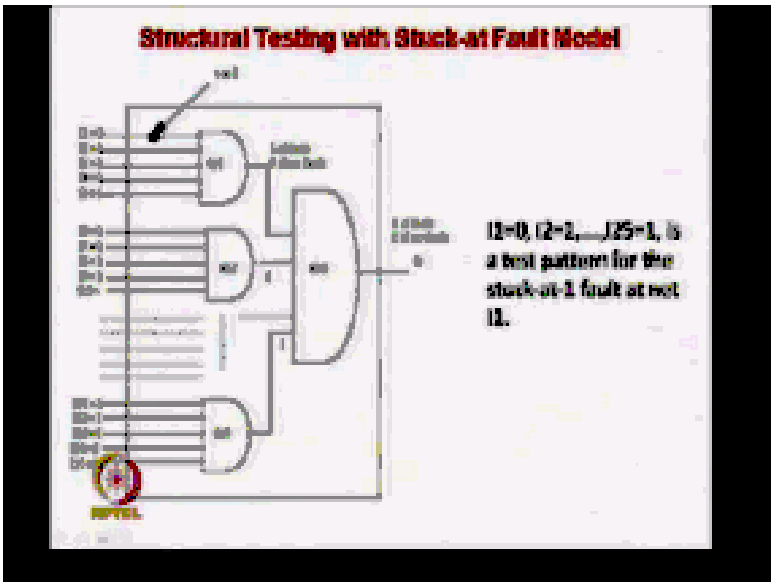

So let us go to the yesterday's all last is example so this is a circuit to let there be a stuck fault here stuck at once fault at the pattern to test the stack one fault is zero are here if fault is sensitized. If no fault is there is net will be zero if fault is there mean it is what it meant is one. Apply to the test pattern at this point here to keep all the lines has been one in the output and similarly in this is propagation output has to be done so you have to apply once said all this.

That whether this circuit is doing this ending of input 1 input or input free correct will do it will Who is that it will find out whether this gate is operating properly or this gate is operating properly and whether this Internet that is correct or not Character to do that with NAND gate is a multiplier absolutely nothing to do with his only verify that individual get an individual Internet or proper or not in that is fine.

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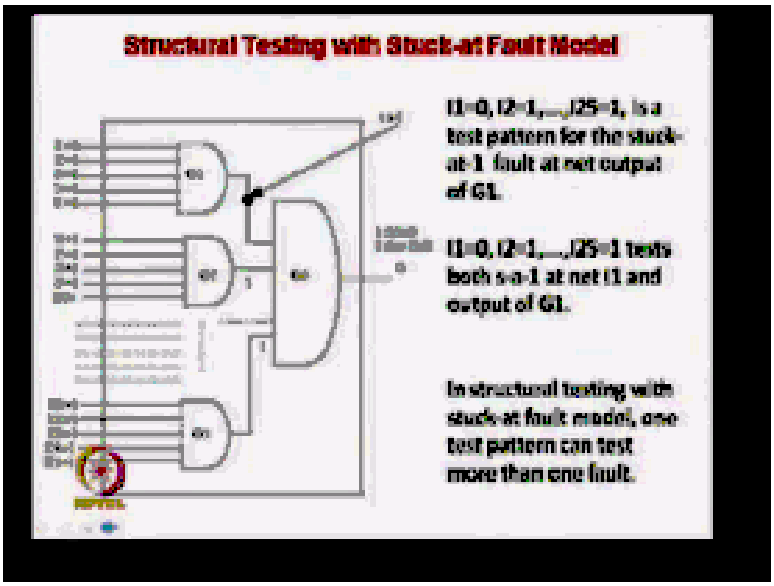

Then they say that it is structural it is tested to be fine It is said to be found at that structural test are very high to equivalent property. About 99.9% law that on Structural testing a really started moving to develop structural testing Structural testing text Mini 4 less time, compared to functional testing at maintain the quality of the solution that is around 99.9% plus quality win then okay.

So I told you the Structural testing does not take the functionality of the entire circuit Structural unit generally in the units of gates in the general level. Regional definition of all as well as the interconnects of the net is fault Some fault ,so you can tell that Structural testing is a functional testing at the GATE level verify whether the gates are functional as the nets are functionally correct And not higher than that explain Structural testing now.

We see what we do in the structure in structural level all the gates this gates are individual element. And we have to find out whether these gates are functionally upper or not and you have to find out the units are correct if you, see that if you test the gates automatically nets are checked so if you want to find out whether these gates are functioning or not what is the pattern you should apply 5 inputs so 2^5 patterns you have to apply.

So what will be there will be 00002 to 5 volts so these are the patterns required to test each NAND gate s this implantation of the 25 leveling ending is done by the 5 NAND gates and there is another NAND gate, which is to find out the next level of this is circuit internship there can be any other implantation of these function so for this gate you have to apply 2^5patterns and these gates you have to apply 2^5 patterns and again for these gates ageing you to apply individually 2^5.

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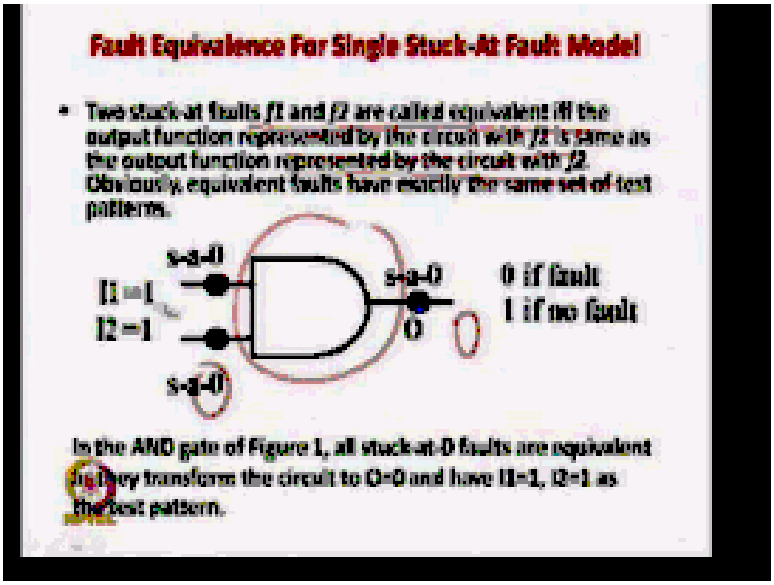

Again so now I am testing each gate individually but i am not testing the entire interconnections or what you called entire circuit. I am testing each gate will individually so number of test pattern equal to test each gate individually these is this one so now you can see how many patterns you requires for the it is very less it is 2^5 into number of gates is 1,2,3,4,5 and 6 so this 6 X 2^5 which is much less than 2^5 so see what you have done if you go for the functional testing of the whole circuit and you have to apply the 2^{25} itself 25 inputs are available.

That is a very high number but now if have to say this i want to test this separately and test this separately and for each gate you should apply 2^5 gate input and number of gates requires isnumber of gate is 6 so 6^{25} is much lesserquantity then 2^{25} p 5 but now i am not done the

integrity test but statistically that if you take this structural testing still the accuracy of a functional testing is as high as 99.9 %.

Now you have to understand one very important thing so what we are doing so if are going for a structural testing, you have to apply the 2^{25}but now if you are applying functional testing then you have to apply 6X 2^5 so the number of vectors applied is a very less number of among. So this called 2^n and thisis actual called k so this case must less than for kl so structural testing is telling you that you have apply some 2 kn input is also told by the structure which will allocate but there is one very important thing you have to note that structural testing is very nice thing.

So you can test each gate individually and you have apply $6X2^5$ test vector which is less than 2^{25} test and the accuracy is 99.9 % plus which has been seen through history and statists but then what you have to pay the thing is not very simple these gate if you want to test if you want to test apply 00000001 and so far this you have to apply but you have to absorb these output this output is connected to this gate and this is a circuit so this line is diagonally fitting this so this thing is not available to the output to be observed so one thing you can do is that you bring this as a separate pin out from the circuit.

Then it is very easy you can apply 5 inputs and you can observe the output s similarly you can observer these gate is directly connected to this NAND gate you can test this circuit fine you can easily apply the test pattern but you cannot observe it directly, so you can bring out the pin outs so that is one thing you have to bring pin outs so now you have decreased the test pattern from 2^{25} to k but which is 6 X 2^5but have to bring lot of pin outs out.

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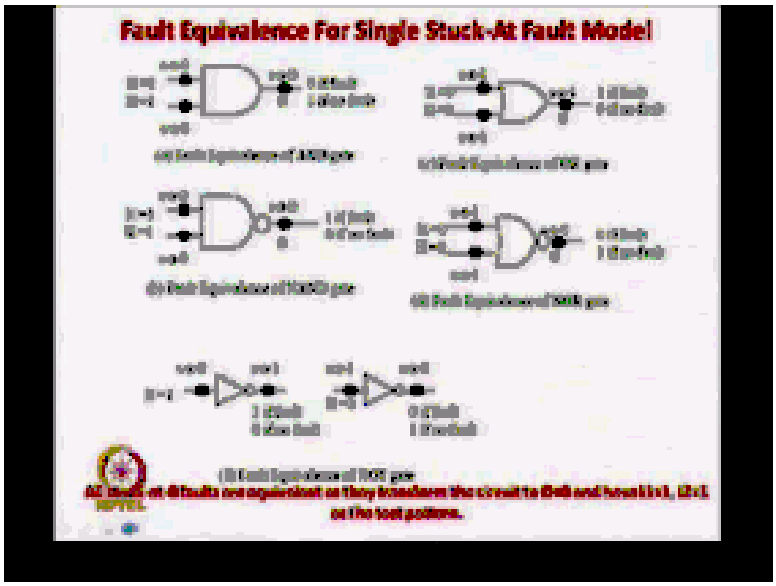

That is actually very difficult situation because you have 1000 nets which you have observe along 1000 extra pins from the circuit, so we see haw to handle this so this the penalty of this structure.Secondly you have to test this gives directly coming out of the circuit input to this NAND gate not directly controllable they are fade by this 5 NAND gate so this directly controllable so for that you have to make a different arrangement.

So you have to brought as separate so there is 1000 nets around then you require 1000 pins extra which is invisible but another more important problem that raised now is that NAND gate is directly connected. Now what as happens this you have to controlthis gates now you cannot observe this so this is not directly controllable now what you do you can observe the value but this gate is driving this NAND gate so i cannot apply any pattern over here directly so there should be some extra arrangement so that i can apply so you cando this because they are some gates you see like.

For example this connected by another gate now you apply some pattern so how can you do that first you have to decuple this case this guy is driving this and then you can apply some pattern, so see what they have done something called a test mode you have to apply when you the test

mode is 1 then what happens the out is directly connected to the NAND gate and the circuit function normally.

But now when i have to do test operation so if you do a test operation you have ensure that this guy is decuple this gate should not able to control this and this gate should not able to control this and put some values here this test is 0 there are, some extra control pins so in this case you can apply 00000001 or whatever so this is gate and this is a line so this internal gate so some other gate which is driving now to apply a test pattern our idea is to test this gates.

Individually then the whole circuit so what you have to do this some other gate is driving this so in test mode you have to make this gate unable to drive this and there, should be some extra pin outs we should now able to drive this gates so that you can apply test pattern as you like so that you can test this gatesindividually so this is possible in this case in all cases by using what you call 2: 1 multiplication.

Basic architecture is something like this in case of 0 and 1 this test mode when the circuit is not in test or normal operation is connected it feeds there but when you make the test mode = 0 then you have to do the testing so this normal cloud and normal combination thing which is feeding this gate is decuple and this separate pin out that is called test pin you can call then this gate connected to this gate which is driving it and you can apply test pattern to test this circuit directly.

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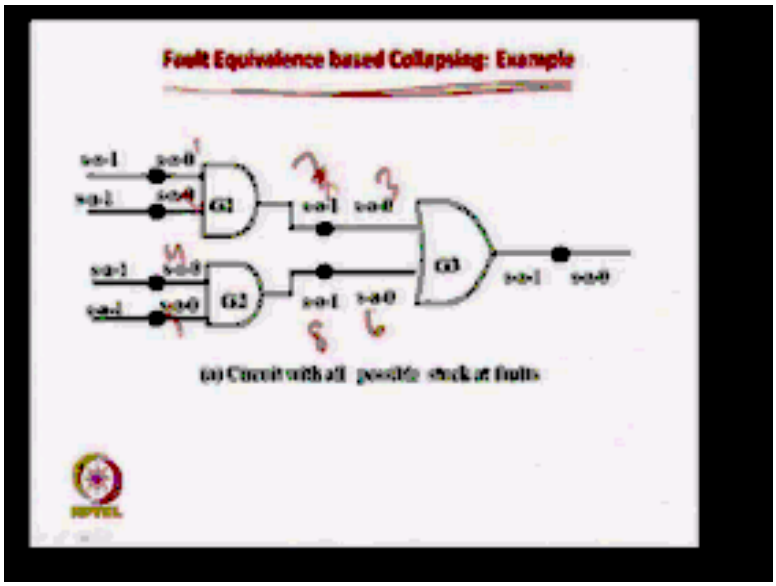

This called controllability so what you have to in case of structural testing there are two things one is observably the output should be observed that is called observability now you have to apply to test this gates because this two pin can work directly because these gates are feeding so what you have to do you have to 3:1 multiplex arrangement so that this lines are become controllable these are call controllable in this structural testing.

What we have done we have brought down from 2^n to some k in this case 6X 2^5but what we have to do we have some extra pins so how many extra pins for this 5 gates you have 5 pins and now for controlling this inputs of these gates you require. How many control pin there are 5 pins for these you require 5 extra pins that is control pins here and as well as we have to put some multiplex so how many multiplex you require in this so this is how very difficult problem.

You have apply some more penalties like structure test is bring down test count but you require extra pinouts and you require extra multiplex so extra pin out is very difficultbecauseyou have 1000 lines you require 2000 extra pins are something so let us see how we can handle this so what we are discussing the number of test patterns require in this case were 6X 2^5which is around 160.

If you are having same test which is 1 mega Hz tester is 0.000016 seconds and for a million sample is 16 seconds so structural testing is what has to be adopted but that is very good but the penalties of extra pins extra marks so how we have to take this thing in to picture.so now we will see how we can handle this the function testing is very good because you did not have extra pins you should not have extra marks but still number of test patterns are very high 2^{25}.

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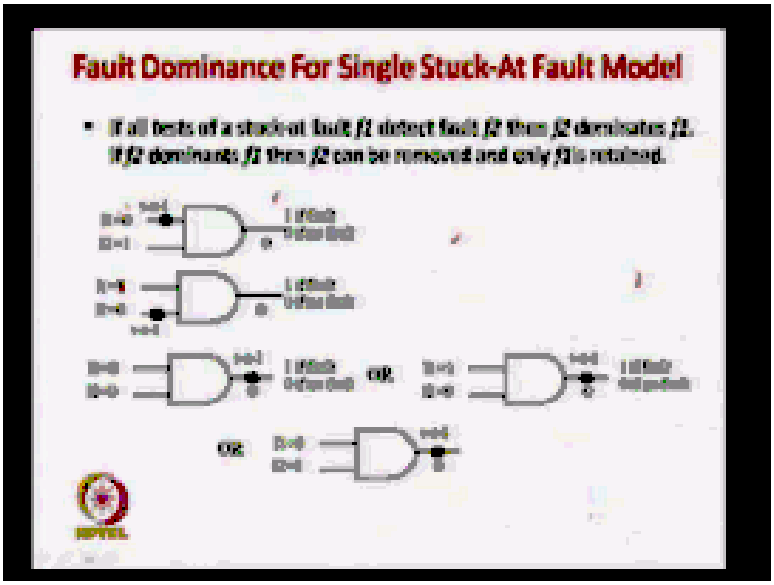

In this case then test time is infeasible but in structural testing you can see that in 16 seconds we can test one million samples but extra pin out sand extra mars are there so research now have been done so which will you study in this course and some in lecture today also and how pins and multiplex are down that is feasible but still taken the test frequency higher and going for functional test is a difficult problem.

So that is structural penalties we have discussed so you require what you called extra pin out sans dome multiplexers so this requirement are infeasible so you cannot have that high requirement so let us see how we can handle the problem of extra pin out and extra multiplexors so we take simple another example with structural testing with internal memory so our main goal is that we cannot have so much amount of pin outs say.

For example I say that i give you 2:1 multiplexer 200, 300, 500, 1000 whatever is possible i will give you because they will only increase my circuit area but if have cheap sixe of this much, so there is fixed number of pins which can be applied on the circuit if this goes to 20,000 or something become infeasible to manufacture 20,000 sample is as larger than you laptop so one chi p size is as large as your laptop you require 20,000 inputs.

But this also not a very good idea but i can still say that I cannot make manufacture cheap with size of a laptop but still I can have a chip and another i can give you area in the chip itself were you can 20,000 marks that is still possible not desirable but still possible so let us see with an example how we can do away this major night mare problem of the pin out first you have to handle the bigger problem, that is the pin out sand then we see the problem of the lesser dimension that is multiplexers.

So this is repel cadre you can see that is 32bit repel carter and 32 bits are the inputs and carry and some you can have this carry so obviously you have to do a structural testing you require 2 p 32 input which is again infeasible in terms of time so how to handle tis so let us do our structural testing so in last structural testing the gate was the unit and we were testing the interconnection now in this case we consider gate as unit level.

We brought bit broader level were full adder is full unit so we consider this as unit will apply the patterns here and we will observe the patterns so there are more gears inside but for this testing this kind of structural testing we are considering this as our unit so structural testing is a functional testing of the unit level so in the general example which we follow through out or in the last example.

The gate was a unit but now for us this full adder is unit so to test it as we know that full adder as 3 inputs this is a b this is carry input then you have to sum then you have to carry out. so now you have apply this 3 inputs that is 2^3 inputs you have to apply per full adder and then we have to see 2 outputs that is the sum out and carry out so now if you look out the structure e in this case it is very simple to apply the input because they are all available in the pin out same we are going to test each individual test.

At a level and also some output is very simple you can easily get some output and also the carry out now the problem is that for a individual that intermediate carry that also to observe this is the intermediate carry is going from here to here so this has to observe as i already told you bringing that pin out is infeasible in terms of number of pins so somehow we have to handle this so how it is handled so in this case people have a applied.

A simple logic so in this case simple chip register so what you do so intermediate carry out of this output of this gate is feeding this forget about the multiplexer is feed to the next level of the adder and also the same time same thing is writing to chip register again there will be another element of the chip register which will again fade y the output of this gate similarly the output of the second last full adder will again go feed the last full adder as well as it will write as 31 chip register.

So we have a 32 bit chip register so now what is happening so whenever we get this output so what we are going to apply. so we are Appling all the patterns for a full adder now you can directly see here and the carry is propagated from this one to this one and so far at the same time instead of driving the pin outs of this carry we are feeding it to a intermediate to a chip register so we are feeding this so when all the testing is done so all the units of this chip register have the values of this 32 bit.

Intermediate carry then you can apply 32 clock pluses so that this data is correct so now in this case you require 32 clock pulses to get the result not bring this output of this carry what we are doing that we are feeding this carry to this unit of chip register so now when the testing has done. Think that is the digital be o'clock for the shift register and at 1 m. to bring it so what we have achieved so if you directly bring out carry out from all these other then you require on 31 or the order of 32 kind in okay and now what is only one and one shift.

What you can call ladies digital least observation public carry 32 Again the food is full error these two are the input A and B can be directly control but there is another full adder here which is directly feeding to this we are going to tell this in the last case example of the year. Philosophy of life we apply or 2 is to 1 multiplexer over here and there is a test control so whenever test

control it’s a zero or whatever so you get in one control this this out of this will feed the author of the season.

So far whenever you are in a test more then what will happen this guy will be this and you can At which carry today what happened this is all of this but now in the last exam Not this happy now actually taking a huge amount of area also .What if I carry values you require at this is this you can shift register story that will take 32 clock pulses because now you cannot feel everything directly to do slowly in 32 clock pulses but now the only other pin out is required output.

In which we required to be brought out in the previous example now at Booty register so this is the only to a stopping that is actually your shifting in p so that you can get the data ready in this in the individual point of first entrance period by reduced in the test I am sorry you are used .used in the number of pin. Whatever I told you anything area in a circuit is feasible but we cannot allowed to increase in this case 64 more pain because he is equal some pin outs for each of the output of the scary class is already there in 31 pin out of the garage and also you require 31 pin to control the individual carry this is not at all possible.

What is actually 62 tester circuit you can order of European Council have a huge number of peace because in the circuit for the package itself will be having so many pins at once it can be as large as you need your laptop by using shift register . Some more area which is one register how can we solve this problem how can I minimize internal register for all number of pins have been shot.

So what is the number of shift registers you can see that is equal to the number of Internet line status is there are 10000 day Internet lives in you require around 20000 pins 20000 likes or 20000 If you require an element of this is register in 6 + 1 Can also handle the issue of large number of in a sorry large number of this internal ok so Structural testing with Fault Models is the answer to the requirement.

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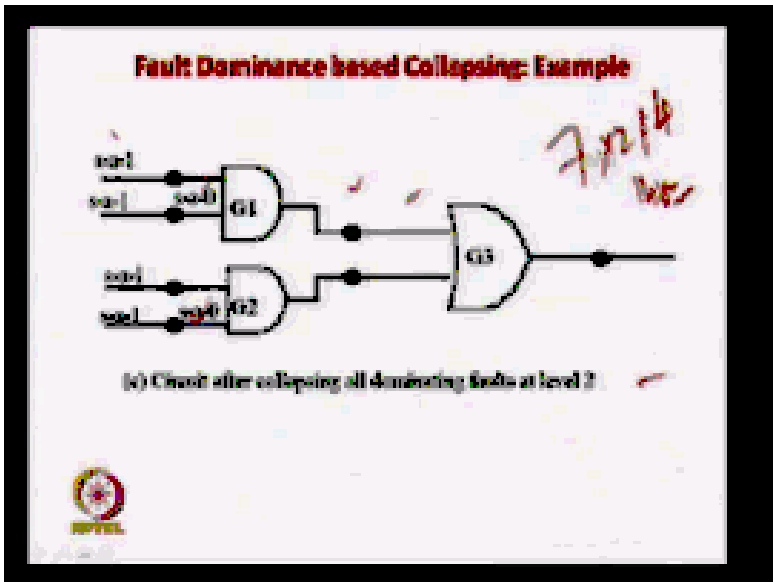

Okay so now we can say that the complete I'm by Structural testing is a functional testing at the lower level then the basic input output function that means what to do functional testing. Call in number of inputs are verified going for Structural testing then you can break up and then we find out whether or not. The game and some days you can even more of a bit higher like in the regions example our unit was a full adder we were not bothered to go inside the other and we will find that structurally fine and our case.

We were functional function it is full and not going and start some interesting that is east full address function proper or not and the full 32 bit adder in other words or Unit on the function as circuit that was it functional element and the block levels with full adder and we're testing this way as they but in the exam example before that our was 25 with Input and or individual block was so in this thing or what you called you need it so we do not need an abstract level like adder Landing Unity structural unit work again any 34 bit adder full adder unit ok so in digital circuits.

Considered as Structural testing terminology example Diesel only for the example to illustrate that what is the Structural testing The essential number of test patterns and Structural testing is

beneficial because it can give you a very less number of test pattern as well as you can have what do you can called we can have a number of pins on number of test items.

Which is much less than 2 to the power number of test, what we have problem the problem is huge number of penis and also there can be large number of internal to is to 1 multiplexer cell when you call register using register we can still say what amount of the PIN number of registers was a problem solving Notes in Structural testing so initially what you are functional then that is 2 to the power to use structural then we brought into k then we have large then this user register so now you are in a position to see how we can.

Register in and also 2 is to 1 multiplexer in Structural testing so again what came into the solution is Structural testing again the last example Shooting with fault model will forget that is a n a full adder is a what is verified and assume that you do not have any fall from the fall so we'll see in this is not the end as a fully functional what is a model Solution is Structural testing with bottle so now I have seen in the last example that we have a Structural testing.

That is a n a full adder so what will verify assume that you do not have any fall from the fall so we'll see now that we not think that Completely forget about the functionality of the unit what is a model with you ask me some model is the reason of the circle. We have to bring down this number that is order of 2 to the power n where n is the number of import the order is equal to a functional testing this week and bring down the number of test speed.

All the properties of alkali as am on the property which is required for the particular application in question for example now or problem is to test that is verified with correct or not so for that Weather in having in indicates or not on the surface so that we can find out any fault model which need not be functionality of the purpose of testing We conquer city of Representation what are the same time you understand that it represents does your job for the job or specification for that particular contact in this case which is a Computer and.

So we have already NAND gate and gate seen that and it is on and it is so composite as a transistor level it can be for layout level in Falls waterfall can be open What do you call me that

that the layout is not proper this layout to be like this is a very thin has become very thin so that can be saying that somebody line is that Should be worn in the normal kiss but in the fall in the area season 02 actually represent now I can say fault.

So I will just say in other words if you want to do a Structural testing of the gates to find out that you apply 00000 to all 1 and then you to find out whether output is zero and Testing is at the GATE level is functional testing of the registers and what is that that you said that if this line is open that is I am not interested Use of circuit is not to guarantee or not to ensure that it is functionally proper that I want to do it I want to find out that there is no.

What I can see that if I say that this line is stuck at zero and the thing is stuck at zero in this case because in this case is anything else This line is not sec 80 stuck at work design is not forget 0:31 similarly for this case and then I can say that and it is not having any kind of stuck at zero on stuck at 1Can be done so now you see how we can all MBBS lecture on human lectures will see how this target structural model helps to reduce the problem of register for the different models what is life can be started so they can be formed at what is the normal amount of time to rise from zero to one in a dinner for the delay will be higher civilized in the fall so they will be here about.

I told you that if all traffic is effect that I put all 11 11 is normal one will actually, propagate this fault effect to the output what is the effect it is what if there is a stuck at 1:40 and the answer is zero in on you can we fall so this is not this an with fall model is a really a very helpful in the sense that we do not require any extra been out as well as you not require any multiplexes or what do you call the register but I will find out to apply.

Similarly not at all and repeat it for all the night here all the later on all the message actually gone test pattern generation with you what are the problems with who do not wear any extra Latest I will be lower because in one is that and you can test multiple target for that is coming to pick and what is the what is the disadvantage function it is no longer and you are not there tour later today so we will go for the question and answer the questions today and in the next lecture maybe or just before we go to the motivation.

What you have finished today will go for the answers of the question what is the question the question answer is that what are the problems of Structural testing without fault Testing without fault model will happen if you need that gets, as well as a larger one thing you can say about this flip flop Second question is that we found on Structural testing with all model is very good then but really happens that really get started 01 Functionality is tested specialist.

Thank you and we come to the end of the lecture so from next lectures onwards we will see how to generate test patterns automatically even the faults, thank you.

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