INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

NPTEL
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VLSI Design, Verification & Test

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Design Verification and Test of
Digital VLSI Circuits
NPTEL Video Course

Module-VII
Lecture-II
Functional and Structural Testing

Okay, so welcome to lecture II on functional and structural testing. In the last lecture in the introduction to digital testing of VLISI so what we have seen is that in case of circuits testing occupies an important paradigm, because in case of circuits the technology being adapted is so new and it is currently changing in such a rapid way that most of chips, sorry you can say a high percentage of the chips may have failure so defects.

That is the yield is sometimes as go as 50-60%, so that is why we have to find out that which of the chips are functionally correct and which of the chips are fault and then we have to bring them appropriately and then we have to separate that before we send them to the market. So that is why testing in circuits is such an important domain, that we have already seen in the last lecture.

Then we have seen that function that comes our testing of circuits or any system maybe in the last lecture we have taken the example of an NAND fate so we have seen that testing can be as simple as just checking the functional properties l.ike for two input NAND fate it was for all inputs that is 000, 110 and 11 and we just said whether it is functionally proper.

Then it can be as exhaustive or as complex as finding out whether the layout from with the cheapest or AND has been designed is proper like the metal deposition should be proper, the thickness between two nets which is being laid out for the NAND gate has to be proper distance of say some X micron which is as part of the design rule checks and so forth.

Then there can be delay fault, then there can be so called the transistor level defects and test, so we have seen that starting from the simple functional testing of the truth table it can be as complex as checking the layout. But now the problem is that as we have to test millions of circuits for a sample run and the number of gates in a circuit can be as large as millions. So to test a circuit in full depth that is maybe to the layout level or the transistor level it may take decades or years.

So that is why we cannot go to that level of exhaustive testing. So at best what is visible, because our idea is that as we discussed in the last class our motivation was that we have to apply as minimum test patterns as possible that is as low test time as possible, but at the same time we have to have a very good what you call confidence or you can say that the accuracy of the test.

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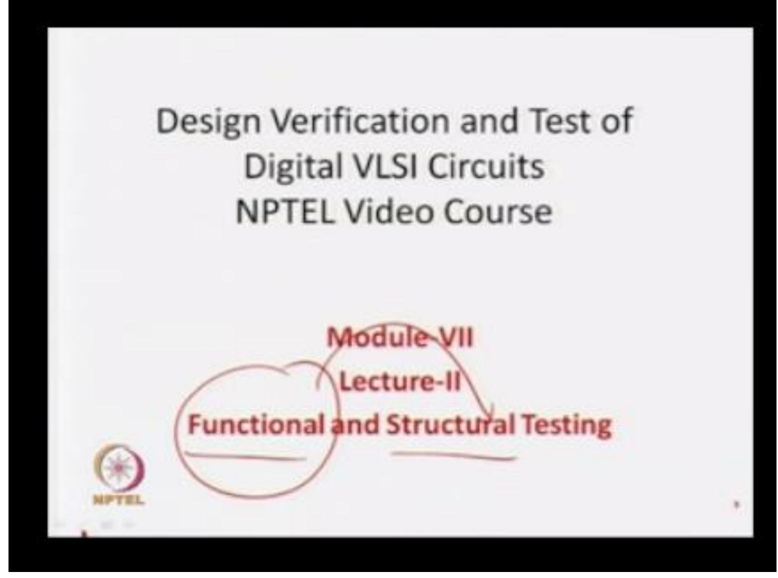

So that is why today we will see what is actually called structural testing. And why we have to move away from functional testing to structural testing that is the main motivation of today's lecture that functional testing that is in terms of the truth table that is how was the simplest testing in the last class. After that there was transistor level testing, then was delay testing and so forth.

And even we will see today that functional testing that is simple the truth table testing is also takes a very long time and is not feasible to apply in a real circuit where the number of samples are in millions. So that we have to move to structural testing, so that is what will be our focus today.

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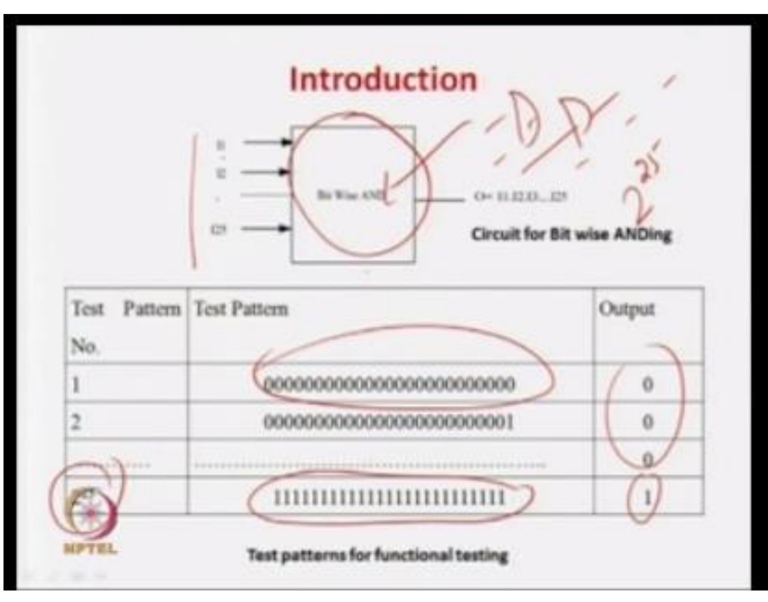

So let us start with an example, so you can see that this is a 25 input NAND gates, AND gate circuit so it actually it is a dot product in 25 inputs (I1 to I25) and inside this there you can have a series of what you call AND gates logic, I mean logic circuits this is not shown because it is quite large circuit. So now you can understand that if we have to do functional testing for this one also we have to apply patterns which starts from all 0s that is I1 to I25 all 0s okay and we have to go for all 1s.

So we require 2^{25} test patterns to test the circuit, which starts from all 0s and we end will all 1s. and what are the expected output for accepting the last thing it is AND for all the inputs that is I1.I2…I25 so for all cases the answer should be 0 except in the last case the answer the answer is 1. So for exhaustive testing you require to apply order of 2^{25} input patterns which is very, very large if you think that if I can even apply a test pattern in the nanosecond range, but if the number of this circuit is in millions you will take days to do the testing, so which is not actually visible.

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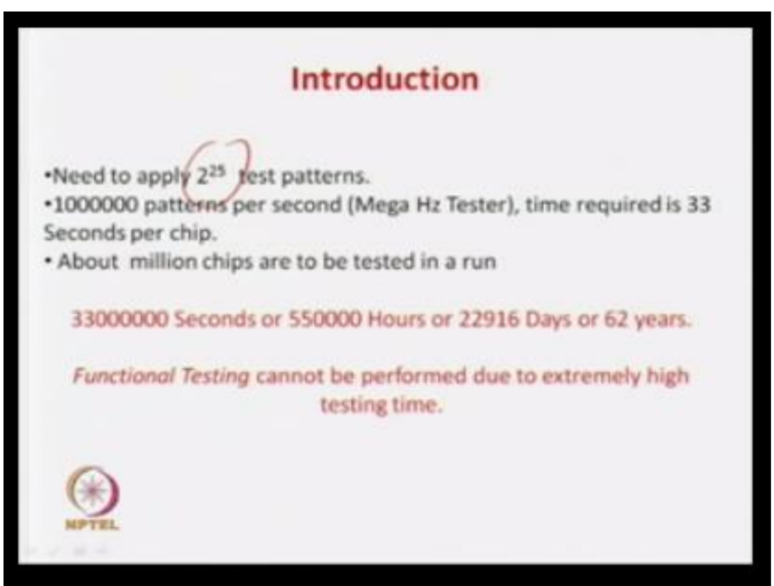

So we will progress and we will understand more into this one. So you can see, we require to apply 2^{25} test pattern so take the fault. And we remember that we are not doing a delay testing in this case, if you have done a delay testing in this case then you have to apply this pattern followed by this pattern.

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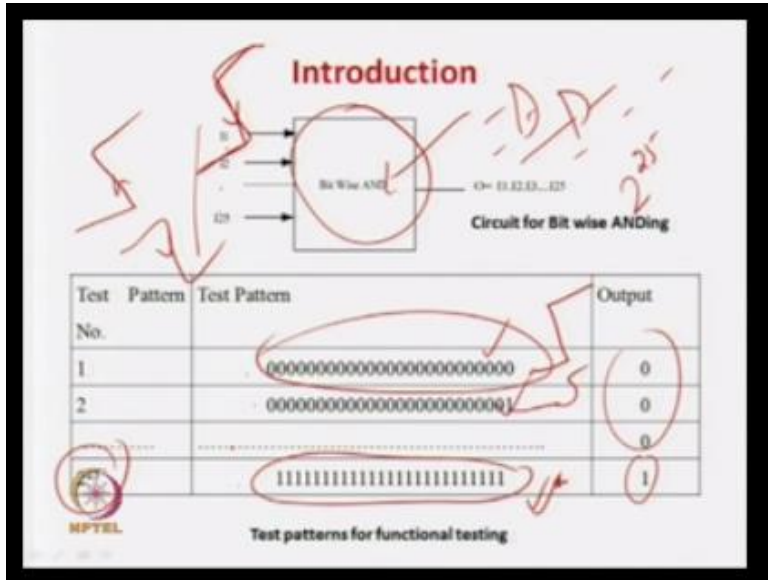

Then you have to apply this pattern followed by this pattern. So you can understand that we have to apply more than double the 2^{25} kind of our faults, because on 2^{25} we just do a functional test. Now if you have to do a delay test that is delay test is 1 is the rise delay and 1 is the fault delay which you have seen in the last class. So for rise delay we have to apply this pattern followed by this pattern then this pattern followed by this pattern and so on till this pattern and this pattern.

Then if you want to go for this sorry the fault test that is from 1 to 0 if this pattern has to be tested that speed then you have to first apply this pattern followed by this pattern, then again this pattern followed by this pattern and so on. So you can easily find out how complex the testing will become even for a simple circuit which is having and which does AND of 25 inputs. So that is why if this is not at all possible.

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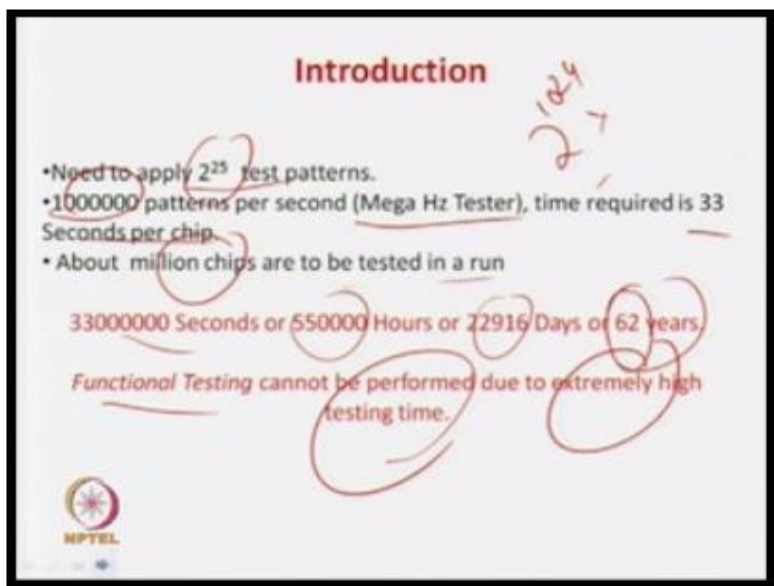

So even if the normal functional test with 25 inputs no consideration for delay and all, you require 25 test patterns. For delay it becomes more complex, and if you assume that we have mega hertz tester that is it apply so many test patterns in a seconds, we require 33 seconds per chip to test the circuit. And remember the only symbol functional test and in generally we have our 1 million chips per run.

That is once we go for fabrication we do not develop or fabricate 1 or 2 chips in a single run we have around millions of circuits. So millions of chips has to be tested in a run, so you can find out if you do the calculation you will require this many seconds or this many hours, this many days or some huge number of years to do the functional testing for a simple circuit having 25 inputs.

So for functional testing cannot be performed due to extremely large number of testing that is what is the idea. Now you can think about this is only a circuit having 25 inputs and the rate circuit has simple as 25 doing an ending of 25 units. Now you can think of a circuit like a Pentium chip which is in our processor or you can think of a graphical processor circuit which can have 500, 12 inputs or 1024 inputs.

Then the number of inputs required will be 1024 and then you can understand instead of this 62 years it can be 62 decades or it can even be something which our testing we will start in our lifetime and we will be not the life to see what is the output I mean what are the data's of the test, that if we never be feasible in our lifetime. So you can understand it is practically infeasible to apply functional testing.

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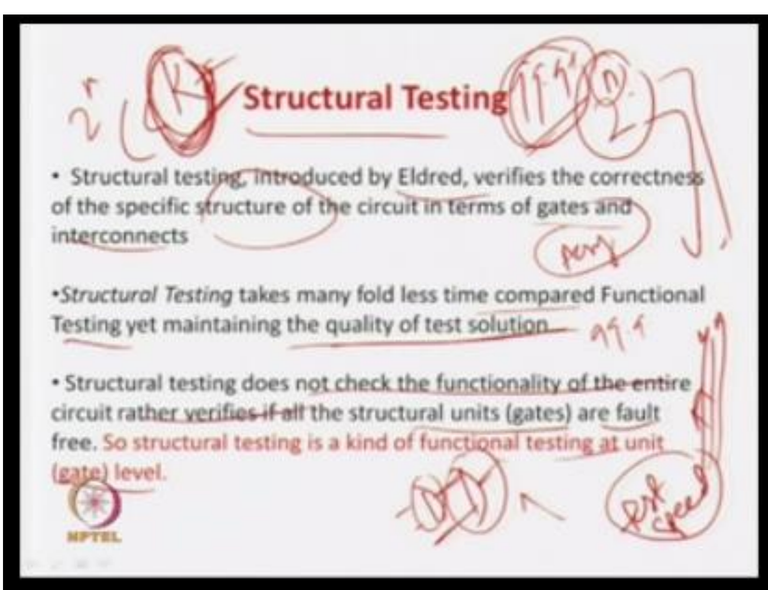

Now you see so what is the solution, the solution is that we have to bring down this number that is order of 2^n where N is the number of inputs. This order is required to do a functional testing, this we can bring down the number of test patterns you can bring down or we can move up the test speed, this we can move up. But moving test speed fine, you can go up to megahertz, you can go up to gigahertz, but going to terahertz or even higher than that will require a test or which will be so expensive that you can never make up a profit by selling the chips.

We can make profit by selling the chips if the yield is low, that is if the chip effects of the circuits are defective, so you can throw out 50% of the chips and other current 50% you can sell in the market and you can make a profit that is absolutely fine. But you can understand, I mean

you have to get the idea that if you have to test a chip in the terahertz they are even higher, the test equipment will be so high that you can never make a profit our of I mean using the test and testing the chip and making a profit out of it.

So AT equipment which we have shown in the last class is a very, very expensive equipment and that is the main reason that why we have to, we cannot concentrate or we cannot do that, we can take the test speed to gigahertz or terahertz or anything in all level. So what is, that is research is still going on to find out that if you can have a cheaper testers which can apply test in a fast rate, but this phase is a very difficult phase to go on.

But so what people have researched on and what people have found out that if we can do somehow bring out this2^n if this number can be brought down that the number of test patterns which has to be applied can be brought down, but still if you can have a good accuracy then it can be a very good paradigm of test, testing or you can say that it is a very good achievement which you have made.

And this is absolutely what people have discovered by statistics, by statistics means of statistical results or history have a very important role in testing. So in testing what you do, you apply a fatten kind of test strategy. And you see what is the outcome for I would say 2 to 3 years in different manufacturing industry. For example, some let us assume that somebody has found out a technique in which you can apply only K pattern to test a circuit, where K this is very, very less than 2^n.

Then we go on using these number of test patterns and then we keep on testing the circuit and then we keep on finding out that keep on doing the pin that this is a normal circuit, this is a defective circuit, but we do not apply 2^n, we apply only K number of these patterns. Now you have to find out the accuracy that what wrong you have done, that is if there are any case, where they have shift fault circuit telling that it is a normal.

So if that is called in accuracy in testing, but history if I look at history people have found out that there can be very good strategies of determining this K number of transitions where the

accuracy is very, very high even it is as high as 99.9%. So that was a very surprising or what you call very nice invention or discovery you can say in which people have found that you can found out there are exists strategies in which you can find out the k number of test patterns where k is much less than 2^n and still you are confidence or your accuracy in testing is as high 99.9%.

So therefore people research actually started taking more in this direction or reducing the test pattern rather than making the test pattern application faster by expensive equipments so this bring down this test patterns to k number of 2^n can be possible to structural testing so we will see what is structural testing if the genital man who introduced structural testing and he say that is very the correct measure and specification of the structure of a circuit in term of gates and interconnects like in a very simple way you say that I have this my circuit say okay.

So what does the circuit does is actually makes an and of input 1 input 2 and input 3 this is actually a functional test but for structural test what we will do is that we will never verify that weather this circuit is doing this ending of input 1 inoput2 or input 3 correctly rather what it will do is that it will find out whether this gate is operating properly and weather this interconnects that is west and correct or not either nothing to do that weather it is a AND gate or whether it is a OR gate or is multiplier it as nothing to absolutely nothing to do with this it is only verify that individual gates and individual internets are proper or not if that is fine.

Then we say that the gate is structurally tested to the fid and you cloud have found that if you can do a proper structural testing then it is equivalent or as accurate as a functional testing to a very high degree say about 99.9% flux so the main area that or the structural testing it the testing area the research mainly started moving to developing good strategy for structural testing.

Takes may 4 less time compared to functional testing yet maintain the quality of test solution that is around 99.9 plus quality risk maintain okay so as I told you the structural testing does not check the functionality of the entire circuit either nothing to do whether a circuit is adder or a substrate or a multiple or that is complete the process it only cheek weather the structural units generally in the units are gate in the general level which are definition or fault free as well as in the interconnects of the nets or fault free.

So start you can tell that structural testing is a functional testing at the gate level you just verify whether the gates are functionally correct as well as the nest are functionally correct so that is a generally we say that structural testing we do we are doing functional testing but only at the gate level and not higher than that so let us try to explain a structural testing was the example which we are considering in the first slide.

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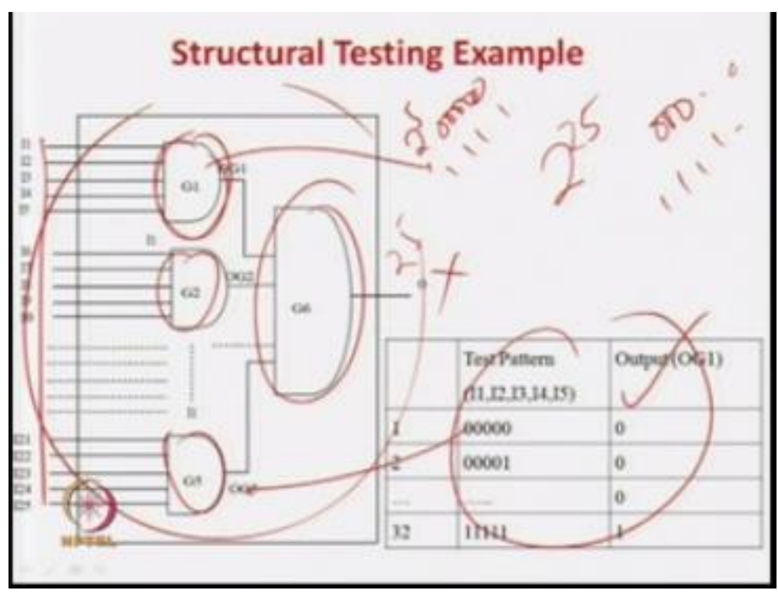

So this again as the same circuit which actually does a ending of 25 inputs now structural functional testing we saw that we require 2^{25} inputs where you state from all 0's to all 1's now we will see what we are, do in the structural level in structural level all the gates these gates are individual elements and we have to find out whether these gates are functionally proper or not and we have to find out whether the nets are corrects so even we see that if you test the gates automatically nets are checked so if you want to find out whether this gate is properly functioning or then what is the patterns you have to apply 5 inputs.

So 2^5 pattern you have to apply so what will be there will 0000 to 11111 so these are the patterns required to test each AND gate okay so this implementation of the 25 leveling handing is done

by 5 AND gates and there is another AND gate which is actually doing the find the next level of this thing this is the circuit implements and there can be any other implementation of this function so for this for this gate you have to apply 2^5 patterns and this gate you have to apply 2^5 patterns.

And again for this gate individually you have to apply 2^5 pattern so each gate now I am testing individually but I am testing the entire interconnection what you call the entire circuit entirely and not testing and testing each gate individually so number of test pattern equal to test case individually is one that is 2^5 .

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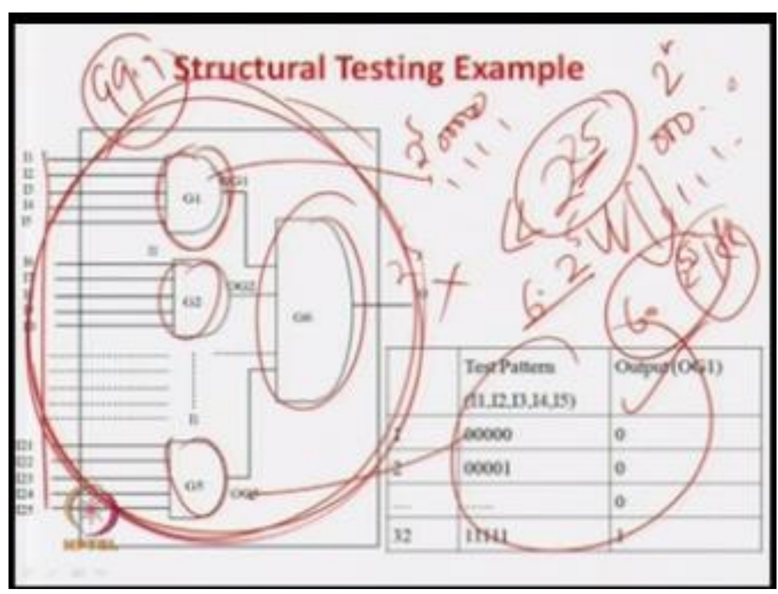

So now you can see what how many patters you require for this is very less it is 2^5 into number of gates is 12345 and 6 so this is 6 x 2^5 which is much less that 2^{25} so see what we have done if you go for the functional testing of the whole circuit then you have to apply 2^{25} inputs are viable that is a very high number but now if I want to say that I want to test this separately I want to test this separately and so forth then for each gate you required 2^5 inputs and number of gate required is 6 so 6x 2^5 25 is a much layer quantity.

Then 2 but now what have I not done I have not done the integrity testing but people have shown statically that if you take this structural testing still the accuracy of a functional testing is as a high as 99.9 % now you have to understand one very important things so what we are doing here so if you are going structural testing you have to apply 2^{25} vectors but now if you are applying functional testing then you're applying 6 x 2^5 test factors so the number of vectors being applied is a very les number of vectors.

So you can call this 2^n and this is actually called k whish is as for our last discussion so this k is much less than 2^n so structural testing is telling you that you have to apply some 2^k inputs now least 2^k inputs is also being told by the structural test which will elaborate.

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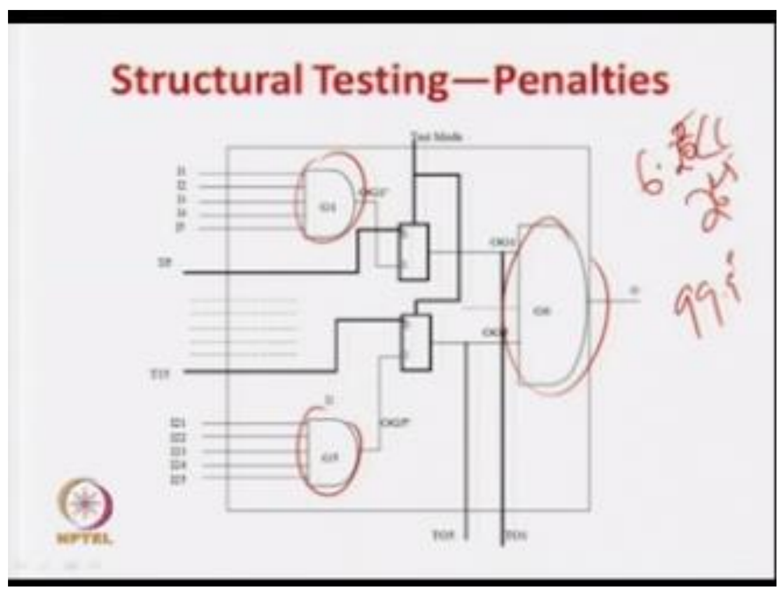

Later but day is one very important thing you have to note that we say that structural testing is very nice thing okay so you can test each gate individual okay and we have to apply only 6 x 2^{25} sorry 6 x 2^5 test vectors which is much less than 16 2^{25} test vectors and the accuracy is 99.9% + which has been seen through history and statistics but then what we have to have pay see then thing is not very simple.

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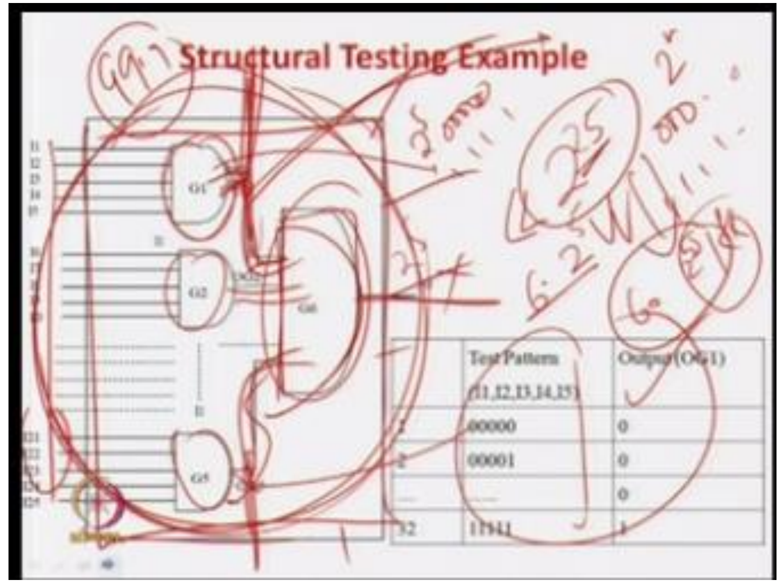

This gate if you want to test so we apply 000001 and so forth this truth table you apply but here to observe this output that this output is connected to this gate right and this is a circuit okay so this line is directly fitting to and so this thing is not available to the output to be observed so one thing you can do is that you bring things as a separate pin out from the circuit then it is very easy you can apply this 5 inputs and you can observe this at the output similar for this gate also this gate is directly connected to this AND gate inside and this is brought out in the chip.

So you can test the circuits fine you can easy apply the test patterns but you cannot observe it directly so you can bring the pin outs so that is one things so for all such internet you have to bring pin outs so now you have decreased the test patens from 2^{25} to k but k which is actually 6 x 2^{5} but now you have to bring lot of pin outs from the circuit that is actually a very difficult situation because if we have 1000 nets which we have to observe then you have to have around 1000 extra pins from the circuit which is again a very inferable situation so we will see how to handle this so these are penalty of the structural test.

Secondly if you have to test this gate last input AND gate the output can be observed because this is directly coming out the circuit but now see again this inputs to this AND gate are not

directly controllable because they are being fault by this 5 AND gates so this gate is fitting so you cannot directly control this so for that we have to make a very.

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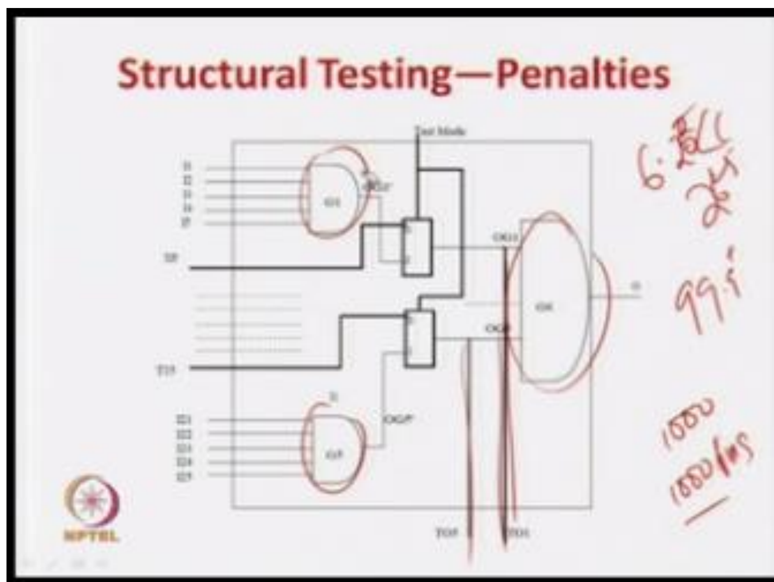

Different arrangement so we will just see so for this case for the output you can say this for the outputs this gate and this gate outputs so which we have borough them as separate pins so this one kind of a penalty so if there is around 1000 such nets to be observed then you require 1000 pins extra which is a infeasible so we will slowly see how we can do away with this but another more important problem that as raised now is that see this AND gate this gate is directly this was directly connected by this one and similarly for this.

Now what has happened is you have to somehow what you have to do is that you have to control this gates now you cannot observe this right so this gate is not directly controllable let us again go back to the original figure.

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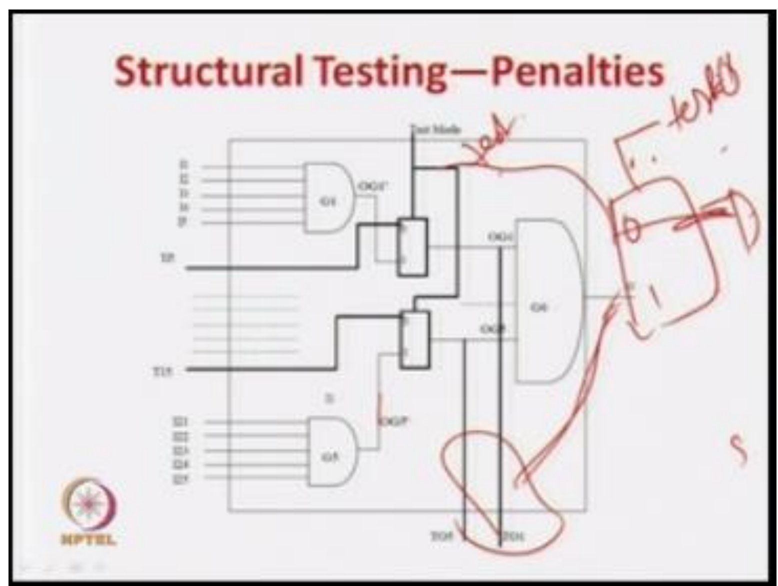

So you can see so now what you do somehow we have brought pins out and we can observe the value but this gate this gate is driving this AND so I cannot apply any pattern over here directly so there should be some extra arrangement so that I can somehow apply the pattern here so how we can do this because there is a some gate you see like this say for example this is connected by another gate now you want to apply some pattern here so how can do that fist you have to decouple this k because otherwise this guy is driving this gate somehow you have to decouple.

This gate and then you can apply some pattern here this is how it is being done so you see what they have done they have put 2:1 multiplexer here and then they have said that say something called a test mode we apply so when you say that test mode is 0 then what happens this output so they sorry let us say that you apply 1 over here first say the test mode we apply 1 so in the test mode if we apply 1 then what happens the output of the gate is to the flip 2:1 multiplexer we have directly connected to this AND gate and the circuit function normally.

So in this case also if it is one so this output is connected here and it fits this AND gate and the circuits is bigger normal operation but now when I want to do a test operation so you if you do a test operation so what you need to do you need to somehow ensure that this guy is decoupled that

is this gate should not be able to control this and this gate should not be able to control this and we should be able to put some values here so now you make this test pattern as test mode as 0 so if you make this test mode as 0.

So this guy connection is crossed by this multiplexer similarly this is 1 this gate crossed and there are some extra add on piece control piece which gets a directs access to in this case so in this case now you can apply 00000 1 or whatever you so now what see what we have here so there was a this is a gate and this I the lien so this is the internal gate say some other gate which is driving now to apply a test pattern because now our idea is to test this gate individual then the whole circuit so what we have to do so this some other gate is driving this gate.

So in the test mode somehow we have to make this gate unable to drive this and there should be some extra pin outs we should now be able to drive this gate so that you can apply test patterns as you like so that you can test this gate individually so this is possible in this case or in all cases by using what you call 2:1 multiplexer so basic architecture is something like this case of 0 and 1 this called the test mode so okay so when the circuit is not in test mode or normal operation then the normal net which is to fitting is connected so it fits there but when you make the test case test mode equal to that when you what to do the testing.

So this normal could or normal combination thing which is fitting this gate gets decupled and there is a separate p now that is called the test pin you can call then this gets connected to this gates which is driving it and you can apply test patterns to test the circuit directly so this is called control ability so what we have to do in case of structural testing there are two things one this is observe ability that output of these gates have to be observed so this you can very easily do by bring this two extra pin out that is called observe abilities.

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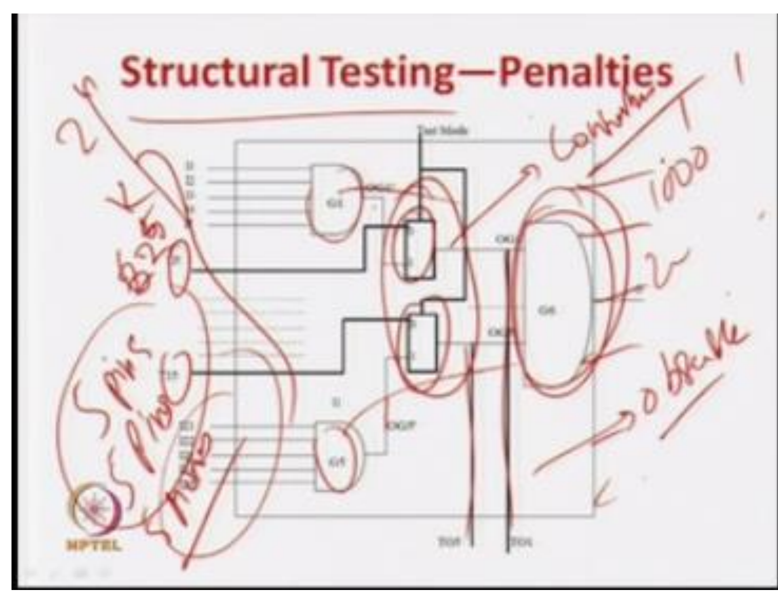

Now you have to also apply to test these gates because these two pins you cannot control directly because these gates are fitting so what we have do we have to put this 2:1 multiplexed arrangements so that these lines also become control level these are actually called control level start so what happens so in structural testing what we have done we have brought down from 2^n x k so in this case so see 2 62^5 but what we have to do we have to have some extra pins.

So how many extra pins for this five gates we have to have 5 pins extra and then that is for observation observe ability and now for controlling this inputs of this gate you require how many control pins there are 5b pins fir this so you require 5 extra pins that is the control pin here and as well as what we have to do as well as we have to put some multiplexers.

So how many multiplexers you require in this case so in this case the multiplexers will be also 5 marches so this is how the this is how is the very difficult problem or you can switch what you call the difficult problem you say that you have to apply some more penalties like structural testing is bring down the testing count but you require extra pins out and you require extra multiplexers okay so extra pin outs is very difficult because if we 1000 lines then you require around say 2000 extra pins also are something.

So a circuit having extra 2000 pins is a very infusible situation so let us see how we can handle this.

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Structural Testing—Penalties

- Each individual gate is tested; however, the integration is not tested.
- To test the individual gates, controlling and observing values of intermediary nets in a circuit becomes mandatory, which adds to extra pins and hardware
- Circuit with about a million internal lines needs a million 2-1 Multiplexors and same number of extra pins. This requirement is infeasible.

So this is what we have been discussing the number of test that are request in this case will 6.2^5 which is around 160 which is much less 2^{25} so if you are having same tester which is 1 mega hertz tester and the time required for testing is only this much seconds and if you have to test a million seconds million samples then you require only 16 seconds so structural testing is one as to be adapted but that is very goof but the penalties of extra pins extra marks somehow we have to take these things into picture so now we will see how we can handle this.

That is people have people could have not yet solved the functional testing is very good because you need not have extra pins you need to have extra nukes but still you have to number of test patterns are very high 2^{25} in this case and this frequency if you are if you cannot apply the test patterns are very high speed then test timing in feasible but in structural testing you can see that in 16 seconds we can say test 1 million.

But extra pin out and marks are there so research now have been done which will study in this course and then we may something is lecture today also that how pins and multiplexer can be brought down that is through the pin but still taking the test frequency higher and going for functional testing is a difficult problem so that is what about the structural testing penalties which you have discussed so you require what you call extra pins and some multiplexers so I mean this requirements are actually directly infeasible so you cannot have that high requirement. So let us see how we can handle the problem extra pin outs and extra multiplexers.

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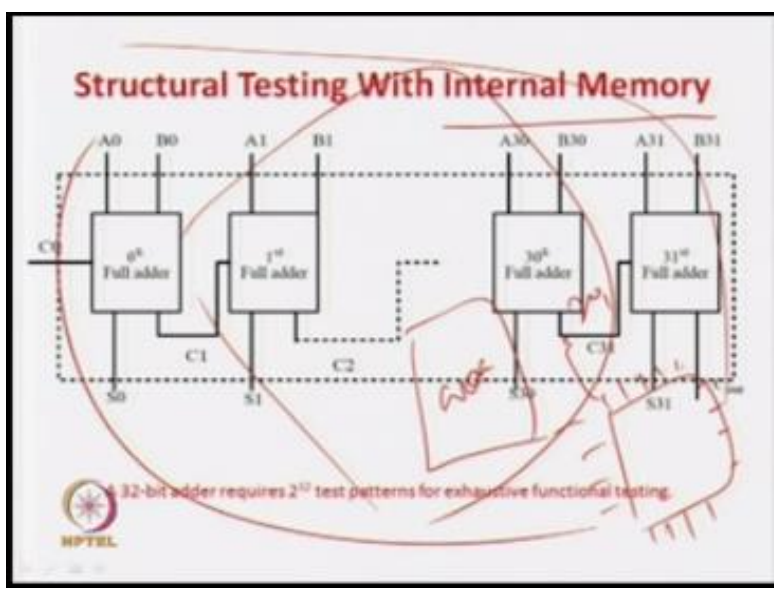

So we will take a very simple another example with of structural testing with internal memory so our main goal is that we cannot have so much amount of thermos say for example I say that I gave you 2000 blokes or I sorry I say I give 22 2.:1 multiplexer 200, 300, 500, 1000 whatever is possible I will give you because they will only increase my circuit area okay but if have a chip size of this much so they fixed number of number of pins which can be applied on the circuit if this goes to 20000 or something they become infeasible to manufacture a device.

So 20000 samples chip we may be as large as this what you call this whole what you can call even a as large as you what you call your laptop so this one chip size may be as large as your

laptop if you require so called 20000 input pins but this also not a very good idea but still I can say that I cannot make manufacture a chip which size about a laptop but still I can have a chip.

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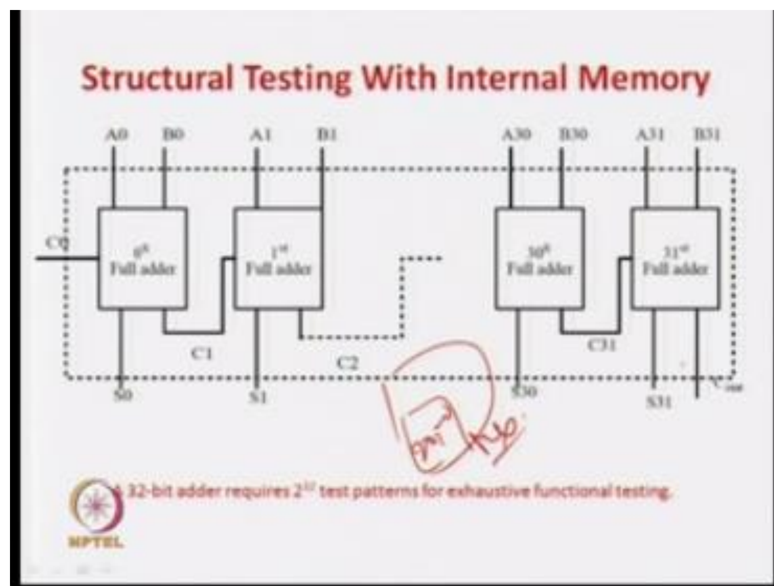

And I can give you another big area in the chip itself where you can have 20000 mucks that is still possible not disable but still possible so let us see with an example how we can do say this major night layer problem of the pin outs so first we have to handle the bigger problem that is of the pin outs and then we will see the problem of the lesser dimension that is actually with the multiplexers so this is a what you call a rubble carrier you can see those are the 32 bit rubble carrier.

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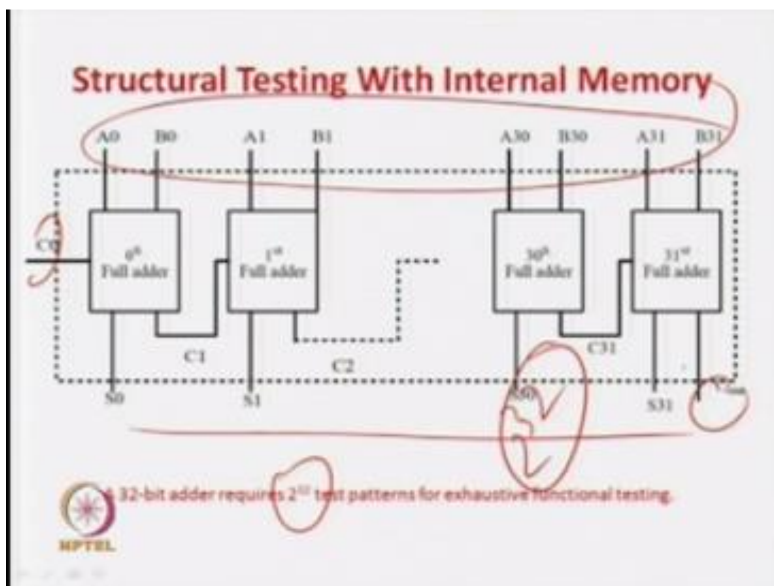

And 32 bits of the inputs and this is the carry and this is the sum and then you can have carrier so obviously if you want to do a structural testing you require 2^{32} input that is that is again infusible in terms of time.

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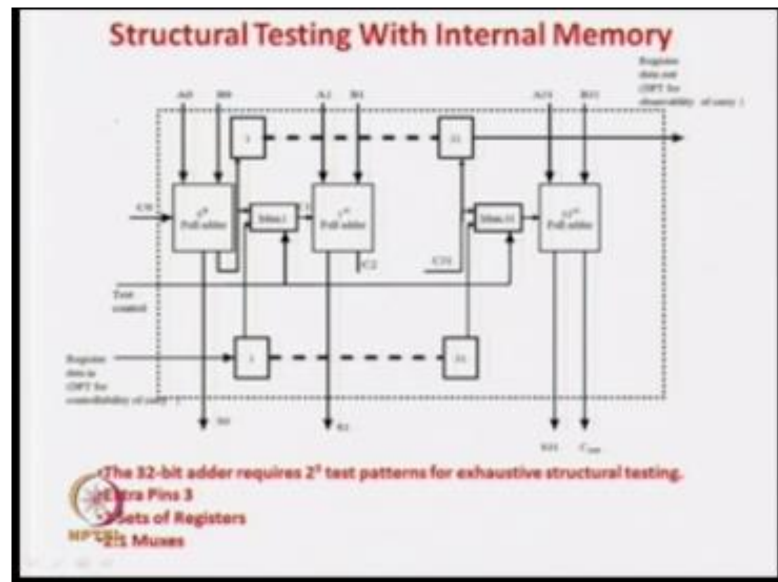

So how to handle this so let us do ask structural testing so structural testing in this in the last case the structural was the gate was the unit that is we where testing a agate and the unit level and we where testing the interconnects now in this case we will not consider gate as a unit level we take it a much bit broader level where.

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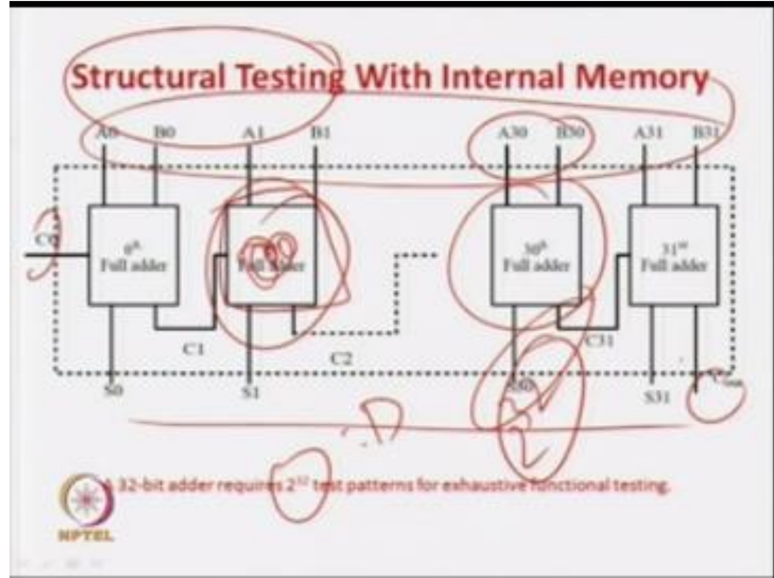

It is full adder is the unit so we consider this as unit we will apply the patterns here and we will observe the patterns here so then there also more input gates inside but for this testing this kind of the structural testing we are considering this hazard unit so basically structural testing as I told the functional testing at the unit level so in the last in the general example which you follow through out or in the last example the gate was the unit but now for us this full adder actually is our unit.

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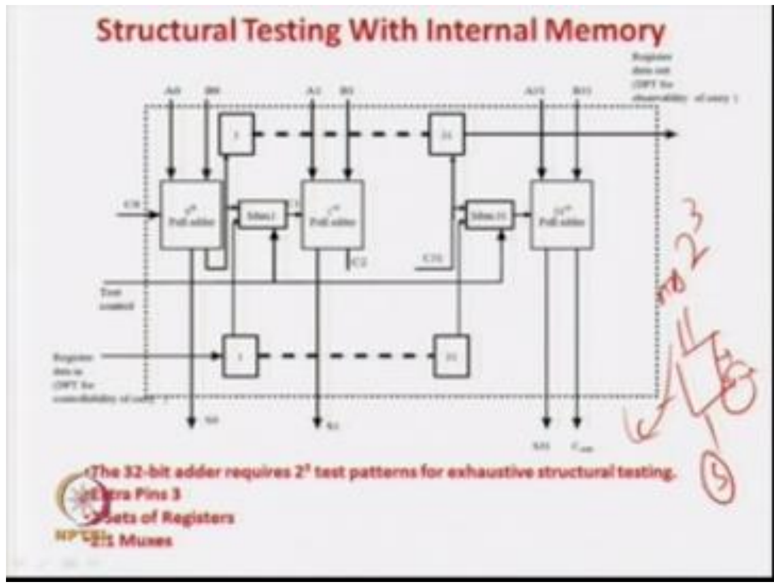

So to test it we as you know that the full adder as 3 inputs this the AB this I the carry input the you have to sum and then you have to carry out so now we have to apply this 3 inputs that is 2^3 inputs only we have to apply per mule per half I mean full adder and then you have to see two outputs that is the sum out and the carrier so now if you look at the structure in this case it is very is simple to apply 3 inputs.

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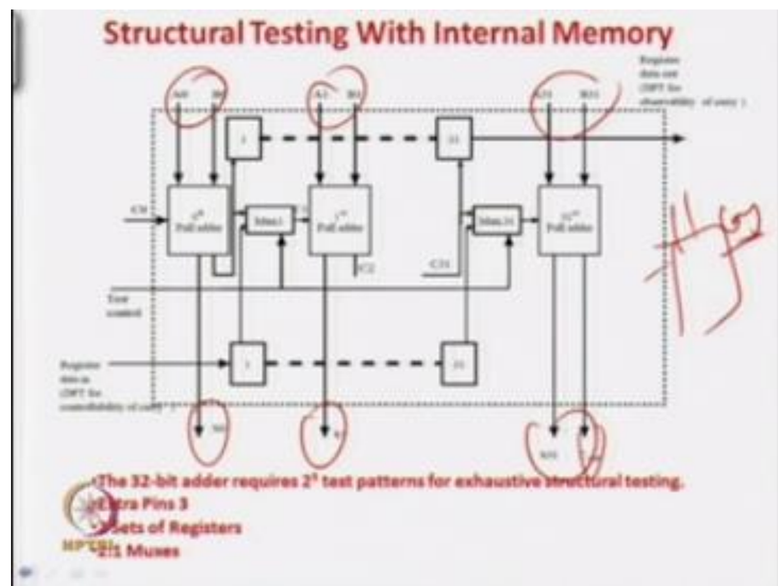

Because they are available at the pin outs okay and we are going to test each individual stuff at a level and also this sum output is very simple you can easily the sum out and also the carrier output now the problem is that for a individual I told you that these are the inputs so this intermediate carry that also as to be observed okay this is the that is this the intermediate.

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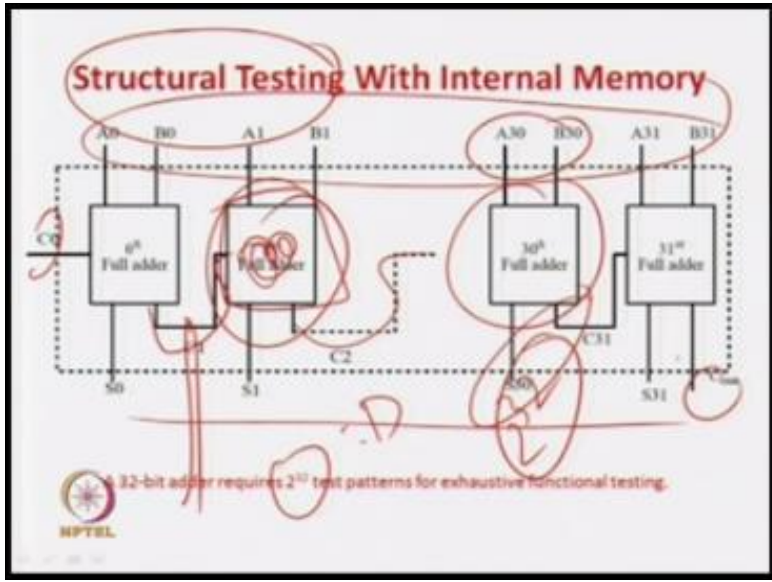

Carry this intermediate carry is going from here to here and here so this is also you have to observe so once this is the way we can take pin out but as I already told you that.

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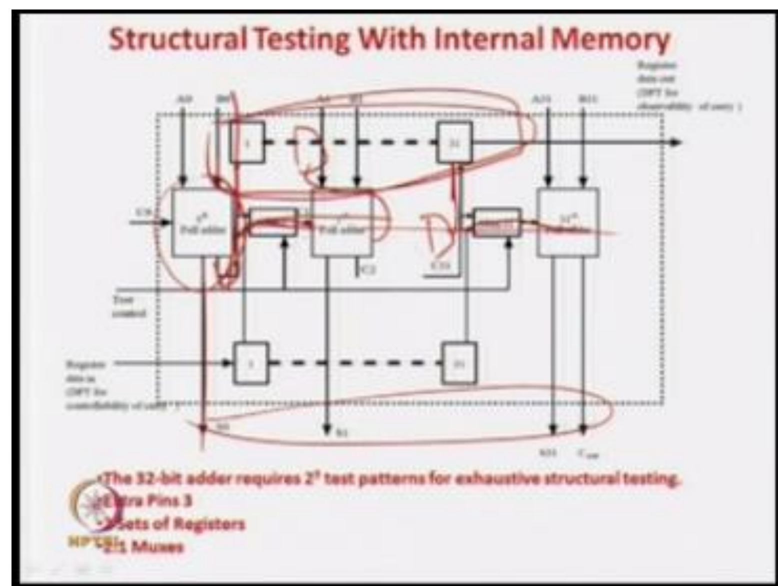

Bring that pin out is infusible in terms of the number of bins so somehow we have to handle this one so how it is handled so in this case people have applied a very simple logic so in this case we have a what you call sorry so we have a simple chip register so what you do so intermediate carrier output of this gate is fitting this for the timing forget about the multiplexer this is being fit to the next level of the adder.

And also the same time same thing is writing to a chip register again there will be another element of this chip register which will be again create by the output of this case similarly the output of the second last full adder will again go to fit the last full adder as well as it will as write the 31 chip register so we have 32 bit chip register here so now what is happening so whenever we get the output is sum you can observe here.

So what we are going to apply so we are applying all the patterns for a full adder now one the sum you can directly see here and the carry is propagated form this one to this one and so forth at the same time insisted of drawing the pin outs of this carry so what you are doing we are feeding it to a intermediate which we are having a chip register so here feeding this chip register so when all the testing is done.

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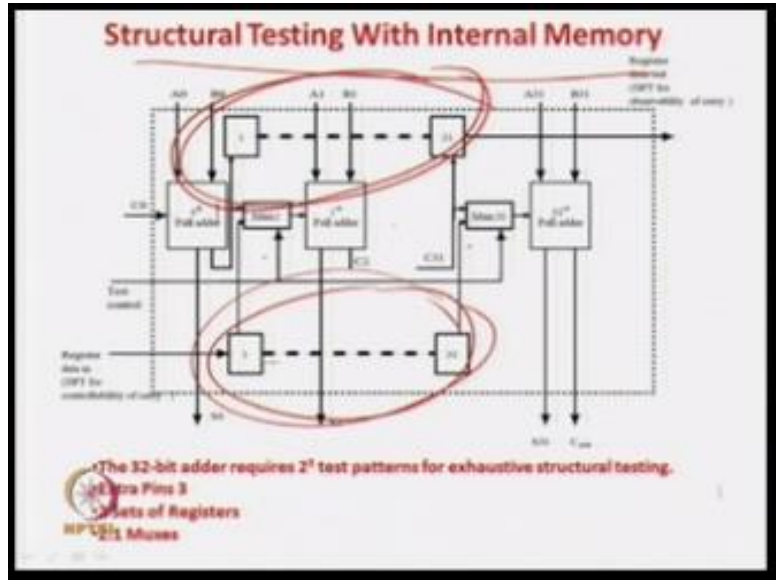

So all this units of this chip register have the value of this 32 bit intermediate carry then you can apply 32 clock pluses so that this data is arrived so now in this case we require 32 clock pluses to get the result because now we are not bring this parallels this output of the carry either what we are doing is that we are feeding this carry to this units of chop registers so now once the testing is done the chip register will be loaded with these value and in single goal you cannot have the result we have to shift out the result the sequential manner.

So 32 clock pulses will be required or I mean in order of 32 I mean you can forget out the last carry bit, s o they have to be shifted out of this thing. So now still you cannot say that I have totally done away with this pin business because we require one extra thing that is there will be a clock for this shift register and as one pin to bring it.

So what we have achieved so if you directly bring out this carry out from all these adders then you require say around 31 or the order of 32 kind of pins, okay and now what you have achieved we require only one clock pin and one shift pin that is shift out you can call data register out that is observation from the carry so instead of 31 or 32 pins in this case we have got the what you call two pins we have done with this. But what is the penalty pin now the penalty where is we

require 32 clock pulses to get the value. Now there is another point that is about the observability.

Now if you look at this full adder so what you have to do again the full adder these two are the inputs a and b which can be directly controlled or there is another full adder here which is directly feeding to this carrying, so somehow we have to again when you are going to test this full adder we need to somehow decouple this as in the last phase example of the AND gate we have achieved so we have to able to decouple this somehow and then we have to apply the test pattern whatever is required.

So same philosophy we apply we apply a 2:1 multiplexer over here and there is the test control so whenever test control is say 0 or whatever so get in one control this output of this will feed this the output of this and this and so forth, and whenever you are giving the test mode then what will happen this guy will be this coupled this guy will be this couple this decouple and you can have a directly control of this what you call this multiplexer sorry, what about this array this carry through the multiplexer.

So in this case you have seen what happens so in the text mode this is decouple and this you can have direct control of this carry by this multiplexer. Now in the last example, we have seen that to control this we have directly bought this is a pin out we have directly bought this is a pin out we have directly brought this is a pin out which was again actually taking a huge amount of area sorry, huge amount of pin outs. So now again to solve the problem they have again put a shift register over here.

So whatever carry values you require at this, at this, at this you can shift in a shift register slowly that will again take 32 clock pulses because now you cannot feed everything directly you have to do slowly in 32 clock pulses but now this again only another pin out is required, so instead of directly controllable pins which you have brought out and also the observable pins which we require to be brought in the previous example, now we are putting a shift register.

So the shift register is requiring only two extra pins that is actually your clock pin and your shifting in pin so that you can get the data ready in the individual points it of course take some clock period but your hugely reduced in the test time I am sorry you are hugely reduced in the number of pin outs. So structural testing with internal memory reduces your pin outs, but we a actually require more number of same number of multiplexers but now we have added to new shift registers.

But and I told you increasing area in a circuit is still feasible but cannot allow to increase in this case 64 more pins because you require some pin outs for each of the outputs of these carry last is already there so you are requiring 31 pin outs to observe the carries and also you require 31 pin out pins to control the individual carries, so this is not at all possible so that is actually more 62 test a circuit you cannot double up your pin counts or have a such a huge number of pins, because then the circuit itself or the packet itself will be having so many pins that one chip can be as large as your maybe your laptop.

So by using this internal shift registers solve the problem, so in this case we have solve the problem but again we have added some more area which is for the registers. Now we will see how we can again solve this problem, okay how can you minimize this area of the extra this thing.

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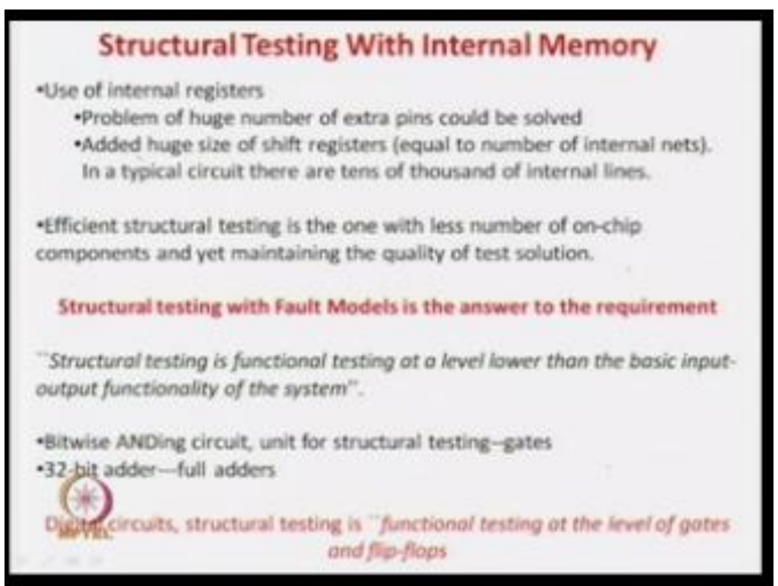

So you see what we have discussed that if you were doing structural testing with internal memory with we require internal registers that is fine but the huge number of pins have been solved. So what is the number of shift registers you can say that is equal to the number of internal nets lines have to be tested, so if there are 10,000 say internal lies then you require around say 20,000 I mean then you may require order of 20,000 blocks or 20,000 flip flops in each shift register that is I mean for each net you require one element of the shift register and you see these are consists of the flip flop so one flip flop per matrix control.

So that is also a very high in number but still that is a less amount of a problem then the pin outs, but now we will see how we can also handle the issue of these large number of pins sorry, large number of this internal shift registers, okay. So now we will see so structural testing with fault model we will actually solve the problem that we will see, okay so now we can say that the some key terms like structural testing is the functional testing at the lower level then the basic input output functionality of the system.

That means what so if you have a circuits says like this so if you want to do a functional testing then you have to say verify that whether my 2^n systems are verified I mean 2^n number of inputs

are verify, at now if you are going for structural testing then you can break up your circuit into individual blocks and then we will find out whether you assume that you have to just test with that this blocks are individually correct or not inside this things we are not bothered.

So in a general structural testing which we is term which we use in testing the basic block levels are the gates and sometimes we can even go up a bit higher like in the previous example our unit was a full adder we were nor bothered to go inside the adder and testing but whether we were finding out that structurally the interconnection should b fine and our case we were functionally testing the full adder and inside we were not going and structurally we were testing that is whether the each full adder is structurally proper or functionally proper or not and the full 32 bit adder we were testing structurally.

In other words, our few 32 bit adder was the unit or the functional circuit so that was the functional element and the block levels where the full adders and we were testing this where the as the units. But in the example if you example before that out circuit was 25 bit input and our individual block was a gate, so in testing in the testimonial or in the terminology of testing what you called this unit is a gate.

So do not I mean generally do not go to an abstract level like adder or something like that out unit is generally testing. So in this case the bit wise and ending unit the structurally lead to us again and the 34 bit adder the full adders where the units, okay so in digital circuits structural testing basically functional testing at the unit of gates and the flip flops, so flip flops and gates are considered as units in the general structural testing terminology.

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Structural Testing with Fault Models

- Structural testing with fault models involves verifying each unit (gate and flip flop) is free from faults of the fault model.
- A model is an abstract representation of a system.
  - modeling reduces the complexity in representation but captures all the properties of the original system required for the application in question.
- Fault model is an abstraction of the real defects in the silicon such that
  - the faults of the model are easy to represent
  - should ensure that if one verifies that no faults of the model are in the circuit, quality of test solution is maintained.

So only for the example we have showed for the full adder but you cannot go think that it is a general terminology kind of a thing this was only for the example to illustrate that what is the structural testing and what is the functional testing. So till now we have seen that functional testing is difficult because of the exponential number of test patterns and structural testing is beneficial because it can give you a very less number of test patterns as well as you can have what you can called we can have k number of pins I am sorry, k number of test patterns which is much, much less than 2^n number of test patterns and yet the accuracy is very high I mean as large as 99.9%+.

But what do we have problems the problem is the huge number of pin outs and also there can be large number of internal 2:1 multiplexers and what you call registers, so we have seen that by using registers we can still save a lot amount of the pins but still the number of registers was yet the problem. so number of test large of input patterns we solve using structural testing then using the internal registers we have solve the problem of large number of pin outs in structural testing so initially what you have functional test then that is 2^n.

So use structural test then we brought down to k then we have large pins outs then way I have solved using the registers. So now we are in a position that we have a huge number of registers so this is what is all flow so now what we have to solve we have to see how we can solve the large number of registers and also 2:1 multiplexers in structural testing. So again what came into the solution is structural testing with fault models.

So now again what we have seen in the last example, that we have a structural testing like a gate as a unit as a gate or a full adder then what do you verify, we verify that whether the AND gate is functionally correct that is 00011011 and in case of full adder you have to verify whether it is doing the addition where sum and carry of this proper or not. But if we go for a structural testing with fault model we will even forget that an AND gate is AND gate and a full adder is a adder, so what we will verify is it is a AND gate we will assume that it do not have any fault from the fault model.

So we will see I mean elaborate in this, but now the philosophy of structural testing with fault model is that we do not even think that an AND gate is the AND gate or what you call a full adder is the full adder that is we completely forget about the functionality of the units. So what is the model basically if you ask me so model is basically a representation of the circuit or representation of a system in a very simple way, but it actually to have all the properties or as I has amount of properties which is required for the particular application in question.

For example, now our problem is to test a circuit that is we have to verify that whether the circuit is correct or whether the circuits have any defects or not, so for that if we have some model then our model should be enough only because the our testing our goal is not to find out whether a AND gate is the AND gate OR gate is an OR gate basically our main goal is to find out whether the circuit is having any defects or not or circuits is having fault or not. So for that if you can find out any fault model which need not be functionality of the gate but still if it can serve the purpose of testing then we have got a very good fault model.

So the for a fault model basically reduces the complexity of representation but at the same time you have to understand that it represents or it does your job or does the job or means the

specification for that particular context in this case which is a what you call in this test, in this case is a testing.

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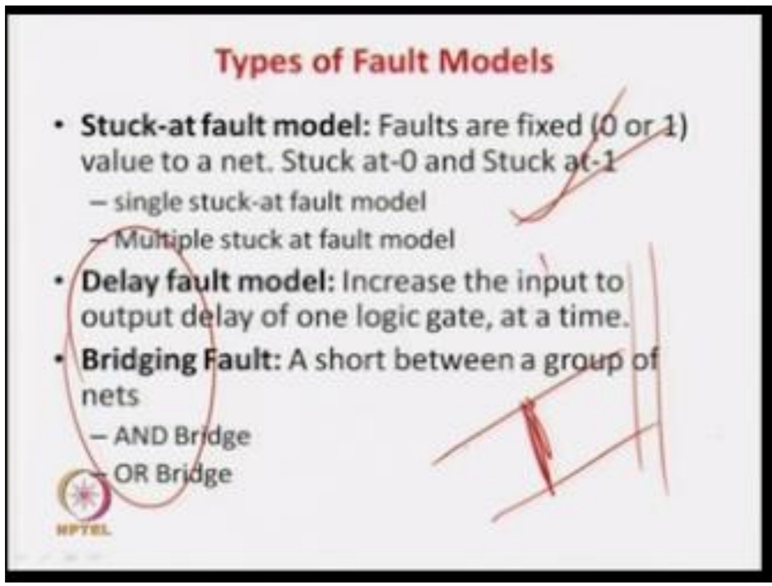

So we will take an example so you can understand better so this is the AND gate so we have already seen that AND gate in case of NAND gate is so complex it has a transistor level it can be for layout level, it can be for so lot of false can be there, so for example let us assume that this is a stack open for, okay this like is somehow cut this input is somehow cut. So this is actually call the defect that the layout is not proper this layout should be metal should be like this but somehow there is an opening now this is called the error.

So there can be 100s of 1000s of defects sorry, this is called defect so there can you can say that this is where so the where is as thick for some place maybe the where is not cut but the this is become very thin so that can be a defect so they it can be saying that some where the line is littler bit thick that can also maybe a defect, so that is very difficult you cannot do all the testing in this small amount of time it is given.

So in this case this is tack open somehow this is the defect, now what is an error so error you actually representation of this defect so in this case if you apply everywhere 1, 1, and 1 and so forth then the answer should be 1 in the normal case but in the error case it is 0. So error actually represents the main hesitation of this defect. Now you can see now I can say another way that there is fault so this is the error is the manifestation of the defect and fault is the logical representation, so you can say that these net is stuck at 0 and also this net is stuck at 0 because whatever value you apply this can net never be 1 and this gate can never be 1.

So structural testing or sorry fault model basically says in this one, so I will just say in another words so if you want to do a structural testing of the gates so we have to find out that you apply 00000 to all 1s and then you to find out whether the output is 0 and 1 in the respective cases. So that is about the structural testing of the gate at the functional level because I told you structural testing is at the gate level is functional testing of the gate.

But the request lot of registers and so forth so now what in fault model it says that, this is I say that if this line is open that is default because now because I am doing testing so I am not interested to find out whether this gate is functionally correct or not, but rather I motivated to know that there should not be any defect in this circuit, because that is testing, testing in case of circuit is not to guarantee or to ensure that the circuit is functionally proper.

Then you have very difficult because it takes lone time, so what I want to do is that I want to find out that there is no defects, but testing for no defects is long time because you have to there is lot of physical defects there is lot crystal defects and it goes into physics, so what I can say that if I say that this line is stack at 0 and this line is stack at 0 in this case because in this case we stack at 0 if we apply anything this line can never be 1 and similarly in this case.

So I can say that this line is stack at 0, so if can ensure that this line is not stack at 0 stack at 1 this line is not stack at 0 and stack 1 similarly for this case and similarly for this case. Then I can say that my AND gate is not having any kind of stack at 0 or stack at 1 false, so we are not saying that the gate is an AND gate and it is properly behaving or the function it is correct but we

can only say that the structural testing says that this AND gate does have any stack at 0 at this point and neither in this line.

So these actually call structural testing at the fault model, now what is the fault model in this case the fault model in this case is the stack at 0 and stack at 1 because these are digital circuits so this line can be either normal stack at 0 or stack at 1, so this is how it can be done. So now we will see how we can or I mean in this lecture or in our few more lectures we will see how this stack structural fault model helps us to reduce the problem of registers.

So there are difference for fault model so stack at fault model is what each line can be stack at 0 and stack at 1, so there can be a delay fault so in delay fault the lines do not have a stack at 0 or stack 1 but in the normal time if you require n amount of time false to rise from 0 to 1 in a delay fault the delay will be higher. Similarly in case of this rise delay similarly there can be a fault delay so the delay will be higher.

So this about a delay fault model, so that I mean circuit is normal or the logic is normal but these are delay to rise and fall then they say a bridging fault that is in between two lines there can be a short so these are some complex fault models which will not study in this course milli we will see at this stuck fault which is the most widely accepted fault model because it has been seen that if you can add to these fault model a large number of faults of these nature and more advance nature gets capture so we will see this fault model.

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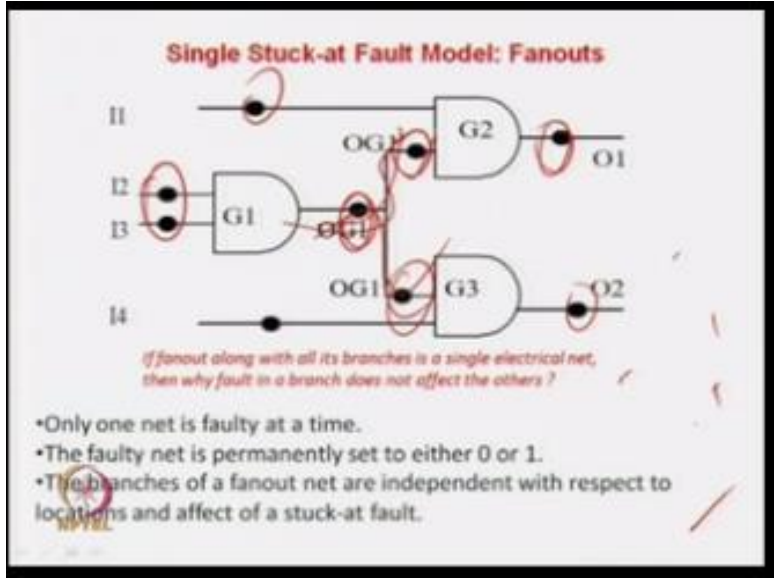

So let us see how was our fault circuit to the fault model bit look like so these are circuit now in structural testing what we have done we have to test these guy individually and this guy individually for that we have to bring we have to observe these are the output so we have to bring them to the output then we have to control these two guys to test these two things then you have to put 2:1 multiplexer here and then we have to either bring these controlling line out or you have to have a two bit but you called register we have to control this so that was the main difficulty in this case.

Be notes we have reduce by the but you called the registers but we could not have done about with the registers that problem was still remaining so now in this case what we have done so if you are doing a structural testing not at the functional level that is the fault level fault model level then what we have to verify we do not have to think that is the Andigade we do not have to think this is the Andigade and so on first we have to verify that these line that have a stuck at 0 and stuck at 1 these lines does not have same stuck 0 stuck 1 and so for.

So we are all the full circuit we are breaking down into individual nets this is one net these are the two nets and this we will see these are fan out this has to be handle separately we will see so

each of the nets we individually concern consider at apply of the apply a test pattern which will verify that none of the gates have a stuck at 0 or stuck at 1 so now we are doing a structural testing but this is not at a functional level and it has been shown that you can if you can do this then also the test coverage is as high as again 99% accuracy.

So slowly we have to see how let me in a few lectures down the line we will see how this structural testing with this fault model it helps to reduce in number of registers number of pin and everything will be varyingly but when the timing just take it for granted take it from my side that if you can if you even test a circuit forgetting about the functionality of the AND Gates and just verify that these have through have a stuck at 0 and stuck 1 faults still the coverage is as high as or you can say that the accuracy has an 99.9%.

But these are very interesting fact here which I should I mention that this is the individual net find these are two individual nets find but this is the single electrical net okay but still for this stuck at fault model says that you have to consider these are the individual name and this has a individual name that is our fan out if this is the fan out you can have a stuck at fault here then the stuck at fault may not be here you can have stuck at fault in this then these two lines are free of stuck at faults when it may happen that this guy is not having any stuck at fault the third net can have a stuck at fault.

Even this whole line is electrically single but this are having three faults I mean three individual faults can be there then now you can ask me the question why is it so the answer is this had been found statistically that is because of circuit generally do not have a stuck at fault now only what we are verifying that we are saying that if you apply test patterns which verify that this lines are this circuit is free of stuck at faults.

Then you can say that what you can say that so what are you saying that we are not in fact testing we are not testing one so we are not trying to ensure that our circuit is free faults which we are trying to ensure say that has be not trying to say that circuit is normal whether what we are saying we are trying to saying that our circuit is having not stuck at faults that is what we are

trying to say then you are saying that no stuck faults stuck at 0 and stuck at faults are not there okay.

Then it implies that circuit is 99.9% plus chance that normal but we are not actually telling the other way down that we are not cleaning we are not saying the other way that if the circuit is normal then no stuck at fault kind of this is not our claim kind of thing so what we are trying to say that we are verifying that the circuit is having no stuck at faults then it is 99.9% chances that the circuit is a normal be so this is that if we but this is the single net then it has been found out mean by statistics of the history that if you under consider these fault then the activates is lower so we have to also consider.

These are the individual net and this is a individual net so basically this is the model in reality circuit does not have stuck at faults kind of a thing it is not as good or as need as a single stuck at 0 and stuck at 1 only we are verifying that no stuck at fault implying that circuit is normal for that result we have to also consider this things.

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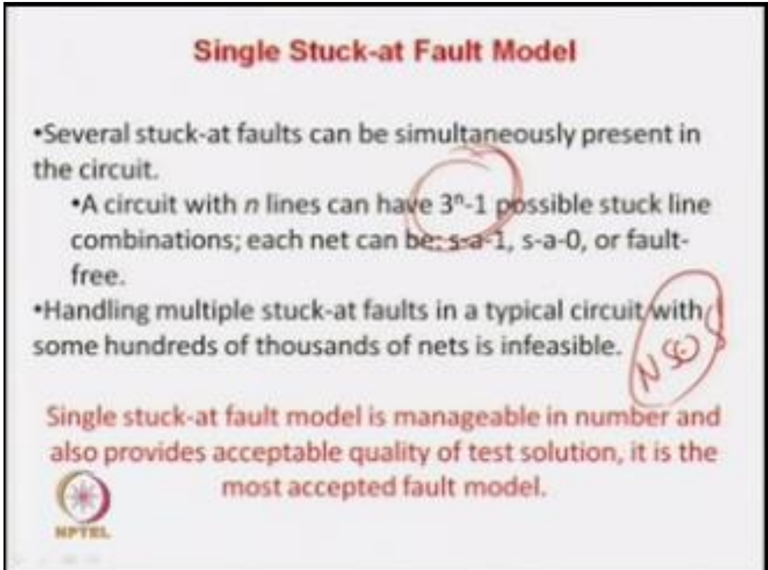

So generally you can ask me that how many stuck at faults at a time so basically the idea is that we can you can say that you can have one lines each line can have stuck at fault now there of lines can have a stuck at fault three lines can have a stuck at fault and dot but if you consider this the number of stuck at faults will be extremely high it will be actually 3^{n-1} because normal stuck at 0 stuck at 1 so if you consider all combinations it will 2 3^{n-1} is a huge number of 1 so you cannot do everything very difficult to handle it so again statistically it has been found that if you consider single stuck at fault.

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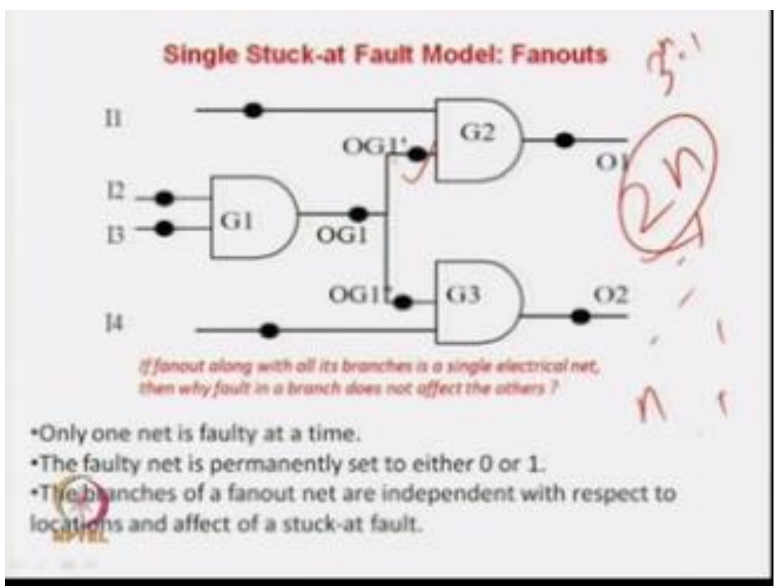

That for at for actually have what is the single stuck at fault you have to think that only one fault at a time I will all consider all the stuck at faults that is true but first I will find out that this fault is not there then I will assume that if I find that fault is not there very good then I will test for this one this fault is not there then this is fine and so for so I will consider one fault at a time so if there n nets and I consider one fault at a time so how many faults are there is actually 2n so if I consider all combination that this line and so for all combinations if I take then it is 3^{n-1} okay but if I consider that only one fault can happen.

At a time but I will consider each one but individually one, one at the time then it is only 2n and statistically it has been found.

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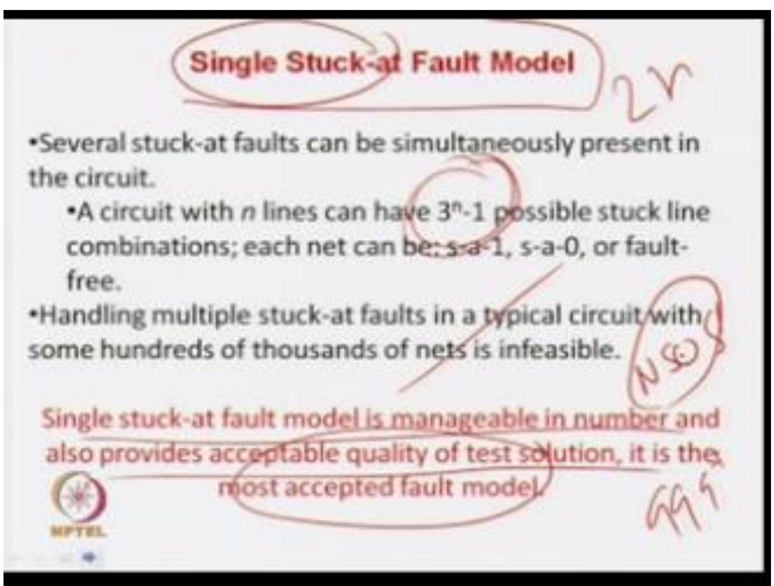

At even if you are taking single stuck at fault model that is handling multiple faults is very invisible of huge number of nets but single stuck at fault is manageable in the number and it also provide acceptable test quality that is we are taking one net having a stuck at 0 at a time verifying it is not there then you are considering the same net it is stuck at 1 verifying it is not there and stepwise one at a time for each net if we verify then it is called single stuck at fault the number of faults are 2n if the number of nets are n then the number of faults are very manageable because a 10,000 lines.

In a circuit only 20,000 number of faults and then you can say that and also it has been found of statistically that these are very acceptable fault model because and what is you called it is very acceptable because this type of testing will be have found that accuracy is around 99.95 plus okay, so that is why the single stuck at fault model gives only 2n faults where is the number of nets in the circuit as well it is the accuracy also 99.9% plus so people are found out that single

stuck at fault model is a very good in a widely adapted fault model so in all future discussion we will be using

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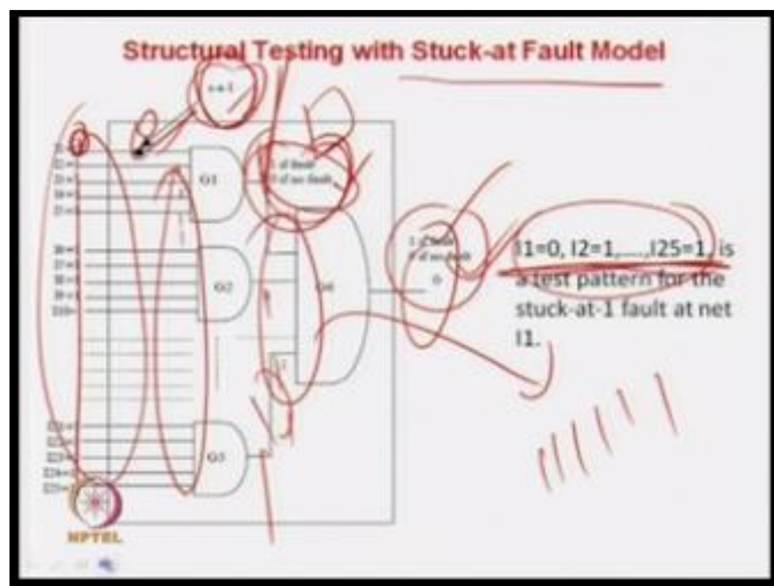

A single stuck at fault model so examples if I can ask you how do you test using a single stuck at fault model so let us consider the circuit so let us say that this net is now having a stuck at 05 so test at stuck at 0 fault what we have to do you have to apply a one over here because this is stuck at 0 you can assume that the electric bulb is fuse so to test that BT bulb is not fused but we have to do we have to have put this switch on so in this case is stuck at 0 so you have to apply a one over here so you have to apply a one over here now you can understand that to see that whether I mean that.

Is what will happen if the circuit is having a fault you will get the answer 0 because of the stuck nature and if the circuit is normal you will get a one but now it is an AND I Gate so if I put a 0 in the last let say in this net I put a 0 then what will happen irrespective of fault is there are not the output will be 0 because these guy will be controlling this output so to avoid this what we have to do is that we have to apply all the other lines has 1 then what will happen I will apply also one at this like.

So what is happening if I apply one at all the lines then what happen in the normal case the answer will be one but if the stuck at 0 in this net the answer will be and 0 this is for the fault and this is for the normal but if I somehow apply a 0 over any other cases then this affect is not brought out in the picture similarly so this is what you are getting 0 if the fault is there and one is the fault is not so again this out this affect have to propagate to the output so what I am doing I am not as I already told you neither I am putting in a pin out to absorb this output now neither I am going to put any multiplexer.

Or register fault so now the fault left affect is here there is 0 if the fault is there and one if the fault in our but I am not able to absorb it because I am not got any pin out here so no pin out is here so I have to propagate this value through this gate okay so now what I do if somehow I get a 0 over here then the propagates fault that the propagation is not there because 0 will be propagated so what I have to do so to keep this effect here I have to apply one over here I have apply one over and so forth so to get a one over here all the inputs of the all other AND Gates should be one so the input pattern 1 all ones if you get the answer one then you can say that this stuck at 0 fault is not there and if you get answer is 0.

Then you can say a stuck at 0 fault is here so by applying this pattern you can ensure that if the answer is 0 the stuck at fault is there and if the and so there is 0ne in no structural for the stay so structural testing with fault model stuck at 01 fault by applying this pattern what we are verified that without using any extra pin out without using any extra pin out without using any extra staff we are verified that.

Our structure with that our stuck at fault 0 fault is not there now if you simply reverse it if you say that these are stuck at 1 fault over here now same thing it is stuck at 1 so I have to some now I apply a 0 over here so I put a 0 in this case and because of the called observe ability thing that is I told you that the fault affect this affect that yeah if the circuit is stuck at 1 here I put all 1 in this input of the AND Gates so if the circuit is normal so this is 0 you applied the answer should be 0 and if this let this native stuck at 1 so you will get a 1 so this fault have to be the affect is has to be propagated through this AND Gate.

All the other inputs have to be 1 so the pattern this one that this net is 0 and all other are ones we will actually prorogate this fault affect to the output so what is the affect the affect is one if they is a stuck at 1 fault here the answer is 0 the what you called the circuit has not fault so this is the pattern which verifies that there is no stuck at 1 fault at this net similarly we do not require any extra net or any extra control ability to test this one so we have seen that structural testing with stuck at fault model is really a very helpful in the sales that we do not require any extra pun outs as well as due to not require any multiplexers or what you called a register.

But somehow we have to find out which pattern to apply to test this is a stack at 1 fault so for this let we have tested for stack at 1 and stack at 0 so we have found that if all 1s you apply you can state first stack at 0, and if you apply this pattern then you can apply test for a stack at 1 fault. Similarly we have to find out patterns and repeat it for all the nets here all the nets here and all the nets here so this is actually call test pattern generation which we slowly see.

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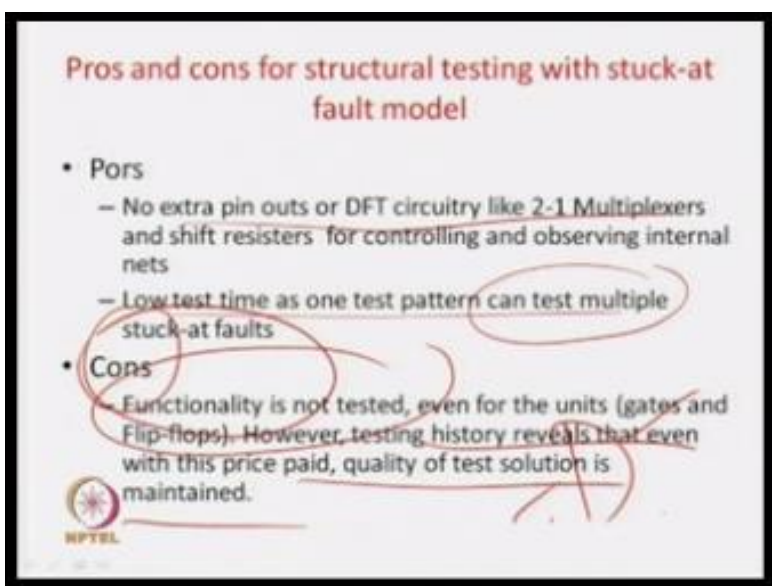

Okay, so what are the pros and cons with structural fault model the pros are we do not require any extra test being or any extra multiplexer or any extra stuff like registers, extra multiplexers

pin outs extra to do the testing. So we are able to find out that is no stack at fault just by into giving some inputs and test time is very low because we will see how with this things we will see later the test time will be lower because in one test pattern you can test multiple stack at for those that means you slowly come into picture and what is the cons what is the disadvantage.

The disadvantage is that functionality no longer tested AND gate you are not testing you are just verifying whether there is no stack at fault are there or not. But still history has showed that even if this functionality is not tested even at the unit level still the test quality is guaranteed to a very, very high level so that is why.

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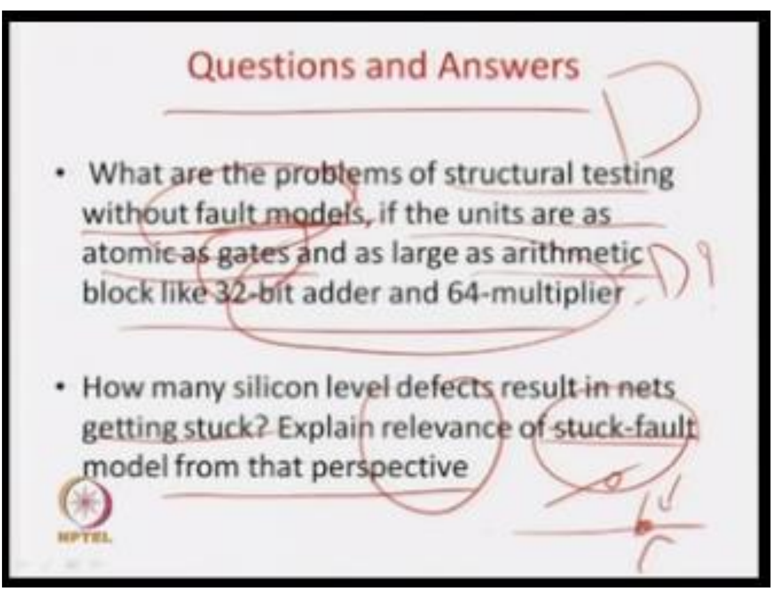

What do you call structural testing with fault model is widely accepted, so before we finish our lecture today so we will go for the questions and answers so we will be putting the questions today and in the next lecture maybe or just before we go to the modification for what we have finish today will go for the answers of the question. So what is the question the first question you should be answer is that, what are the problems of structural testing without fault models, okay.

So we have seen that the structural can be testing can be done with fault models and without fault models, with fault models what are the advantages no requirement of extra pins, no requirement of multiplexers, no requirement of what you called flops and sorry, what is registers and all those things are not required, okay but if you have that is with fault models okay, and so the question we are saying is what is the problem of structural testing without fault models which I have said if the units are gates as well as the units are larger.

So one thing you can say about this we require a large number of flip flops we require large number of registers, we require large number extra pin outs, but you have answer what is the impact without fault model s means you require lot of extra arrangement like pin outs and I told you gates sorry, register pin outs then you require 2:1 multiplexers then you require what you call registers and so forth if you do with, if you are doing without fault models.

Now if the units are gates what is the impact and if the units are very, very large then what is the problem so we have to think of the answer in this way, we all know that this extra stuff will be required if you are doing without fault models. But what is the impact if you consider gate as the block and if you consider adder or full adders, half adders are the blocks then what is the impact so that you have see.

The second question is that we have found that structural testing with fault model is very good okay, then but is that really happens that in nets really gets stack at 0 and s tack at 1 as need as that or as simple as that if it is not so then why is single stack at model so relevant that we can do the whole amount of testing and we can assume that functionalities tested structuralism is tested I mean we should not say that functionality is tested we say that we can say that 99.9% you can be sure that if there is no stack at fault in the circuit then the 99.9% tested adequate to be functionally correct and so forth that is the huge accuracy you are getting.

So how is it possible and why is it so, because the question is this nets in the circuit do not really have such a need stack at 0 and stack at 1 fault because in the real world there are defects like the net maybe torn, the net may have become thinner and so forth. But still why is then stack at fault model if really it is not happening at the level then why is stack at fault model so reified, so these

are the two questions you are putting into pictures so we can go through the lectures and then think over and in the next lecture before we starting it we will go for the answers, thank you.

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