INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

NPTEL
NPTEL ONLINE CERTIFICATION COURSE
An Initiative of MHRD

VLSI Design Verification & Test
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Design verification and test of
Digital VLSI Circuits
NPTEL Video Course

Module VII
Lecture-1
Introduction to Digital VLSI Testing

Hello students welcome to the NPTEL video course on digital verification and test of digital VLSI circuit as you know the courses fee module. So design verification and test as of now we have already discussed in detail the design phase and the verification phase of DNS. So now we are going to third module that is on the test of VLSI circuits.

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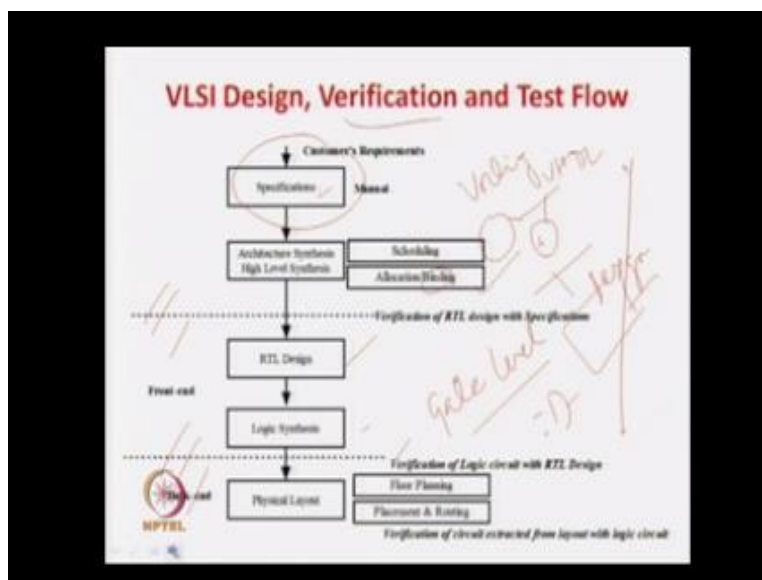

So as we discussed in the first module that start with when is go for Digital VLSI design we start with what do you call the specification of a circuit or specification of a design like for example of a very detailed order strip with specifications like how to design a control flow how to design a add on a simplest. How to design an adult or else as Complex and how to design a control flow of a complex mechanical system at cetera and then, we have seen that we have to write this stuff in some kind of a very simple user language for which is not a technical language then we have seen that it can be coded in form of something called Verilog and VHDL Verilog VHDL language specification.

And then what we have to do is that we have to go for architectural synthesis scheduling a location and binding. That is in case we say that for a given specification to be realized how we can optimally schedule the operators required in the given time step and then we have seen that how individual operators are the harder operators are banded unallocated to the Operations high level synthesis party already discussed in detail in module in Phase 1 of the Constitution design following that.

We have seen that given RTL design register transfer level design we go for RTL synthesis and logic synthesis it is RTL design a logic synthesis we go finally we get is here is a GATE level Boolean Gate level design of the circuit. So this first part as we all know it is called the design part or the front part of the VLSI design following that we go for.

Placement and routing that is back in part of the reason which we have not discussed in this course this first phase of the design this is the VLSI design which is module one of the course has already been discussed and after that in module two which of the verification part of this course we have seen that one phase to another phase from specification to architecture design from architecture design to RTL when you go for logic synthesis that is we get the Gate level design so for the same specification.

We get different form of representation like in this case we can get our control and data flow graph kind of a star for where we get the launch of that is what we can we get is the Boolean

GATE level. So in this case what we get we get some kind of operators in logical step which you call the time step. So same specification like adding control or something we have different representation so every step has to be verified that it is equivalent to the previous specification. That is finally when we have our circuit ready it should be equivalent to specification we have given. So every step should be equivalent to the previous step, so this part was called the verification of VLSI design.

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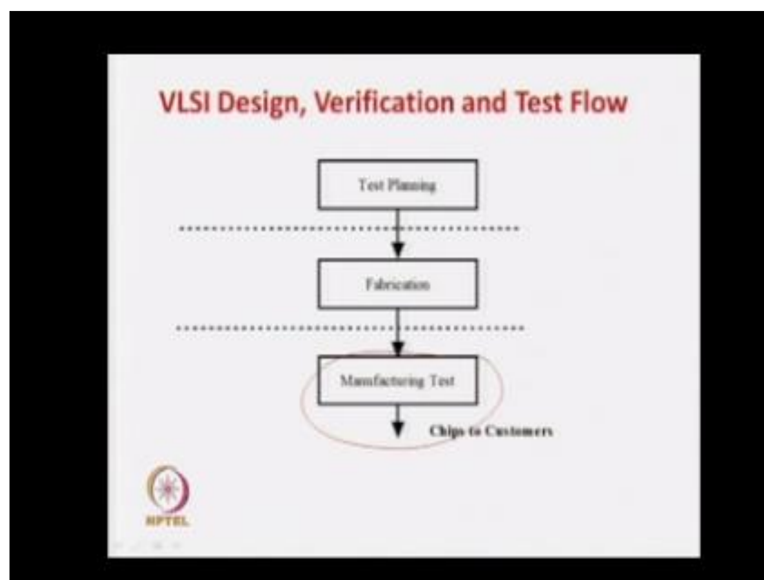

So this part has also been discussed in detail in module 2 of our course. After that what we have seen also discussed in briefly in a very few to initial lectures that after the circuit is done it has been design so it has to be tested that is it should the hardware after the fabrification we get the hardware of the circuit that is the cheap or vertical the packet chip. Now we have to verify that whatever you are shipping to the customer is literally correct that is what ever input signals and the output signals you obtain should be as per what you call specification you are required.

So that is actually called the manufacturing test that is when the circuit has been designed and fabricated it should literally meat the specification. So and when what is the testing that is actually the manufacturing test but as you know that the VLSI circuits are very complex and

circuit with say input of any input if a circuit has around n inputs and say same amounts of outputs. Then to find out the whether the circuit is matching or not electrically all the parameters of specification or all the specification we have mentioned in the now the requirement then we require order of 2 to the power n, input vectors or 2 to the power combinations has to be checked.

But as you know if n is 1000 then 2 to the power 1000 is an the number to be tested. So we have to go for a optimal test or what do you call or test results we apply much less number of then it is 2 to the power n. or any less number of input cases you can apply and then you have to say confidently that the circuit is working perfectly up to a extent and the extent should be around say 99.9 % accurate. You tell that the circuit is operating fine and with the much less number of test vectors 2 to the power n. so for that we require a very detail test planning that how you can achieve this.

So this part is actually called the test planning so in this course the third phase of the which is on the this thing will be mainly discussing how test plans are maid and how you can get a very good cover. That is you can get 99.9 % + accuracy with a minimum level of test cases you can apply. So this is basically what we are going to study in this module so let us go ahead.

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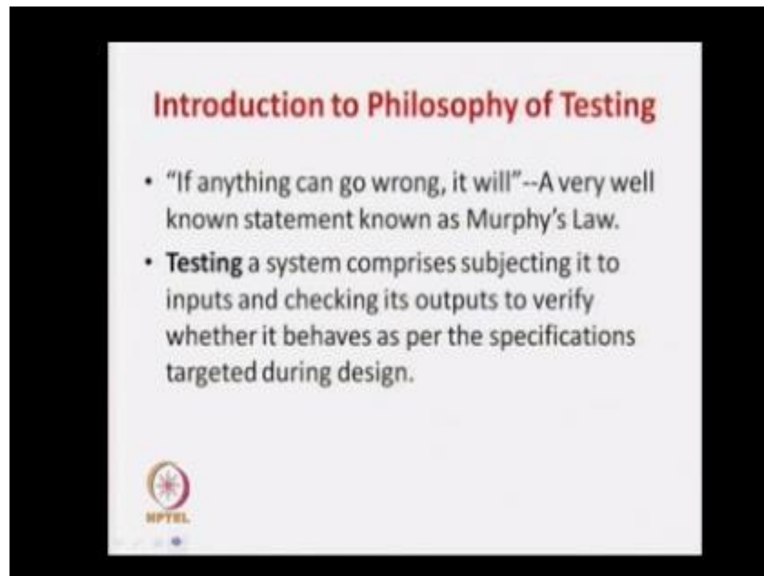

So what is the philosophy of testing so it is a well known Murphy's Law. It says that if anything can go wrong it will. That means if there is probability that system can fail definitely it will fail. There is a very high chance of it and our life as test engineers we should be able to find out that which is cheap of which is the system which is not working properly that has to be discarded and whichever is working properly that can be shift to the customer. So testing if you take a very simple dictionary meaning then it is says that testing a system comprises subjecting the system to inputs and checking that the output at and check the outputs and verify that the outputs are as part the specification target using the design.

So in other words what do you mean by testing so you have this system then you apply some inputs and you get some outputs from the inputs. And you get some outputs now outputs should be as per the design or design specification which we have e told and. So this is actually the output response which is to be matched. Now the question comes what inputs I gave you, so if I gave you enough time and you are infinite amount of available for testing. So you can apply as large number of inputs as possible and your confidence on your testing will rise.

What is the practical scenario number of inputs to be applied during testing will be much lesser because of the time constraints. And there are similar constraints which we will study in this course. So our main goal is that you have to apply as number of inputs as possible to meet the constraints and your outputs should be matching with specification. So what do you call your output should match speciation as large as say around more than 99% + or as much possible as 100% you have to reach that.

So you should show that outputs are matching the specification to that extend. So our output goal is to take the output to a level that you can say confidently with a very high confidence that outputs are matching the specification and at the same time you have to apply as less number of inputs as possible. So this is the testing philosophy.

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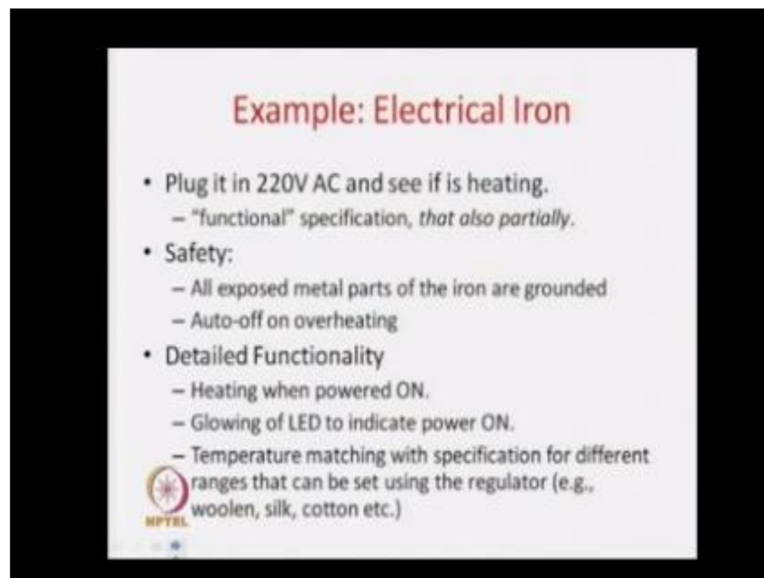

So coming to the next example so before we go for VLSI or circuit kind of testing let us start with an example is a very simple example of an electrical iron or a classical system. So what do you mean by testing an electrical iron if I ask to a man so he or she can say that you just plug in your iron to a 220V AC and see if it is heating is there. So for him it is a testing and in fact in

technical terms this is also proper kind of test, because our input specification for a heater is for electrical iron is that you plug it will be heating and then you can go on for ironing.

So this is also a proper kind of testing so and the technical name of this test is called this is actually the functional specification and so we are actually testing it functionally. Now let us see what more or how integrated testing is you can also understand from this example so these are functional test and these are also partial. But now as we know that electric appliance like electrical iron there is lot of safety features that should be presented. That is all the exposed parts of the heat iron should be grounded. So that there is no short circuit,

Secondly there are many other scientist listing two or three for example if I just put the iron on and then I forget it for some reason then after some certain amount of temperature it should go on for auto off mode. So there are some other specifications that will be coming into pictures that are not that much needed to functionality related to safety part of the specification of the electric iron. So you can see that slowly the Number of testing or number of tests required to verify that your system is operating properly is increasing. So this is another party. So I have to find out that with everything is grounded and you have to subject your heat iron to some overheating.

And then find out whether that it is getting automatically switched off for the following that if I go to a big sophisticated electrical which we can always see which you are now a days which are available then you can see that he has a late show Late. So when you put the electrical iron on the when you heating is going on anything is going on for a LED glows and whenever it is the sum some special temperature is reached the formal step reaches it has been Threshold has been, reached for its features of the heater meaning of the electrical and for some time and then there is a LED glow.

LED becomes off and it goes on in this route so along with also have to test if I am going for a little function it is also see that the LED’s. The LEDs properly working or not that whenever the heater is on it is heating in the late should be powered on. Whenever specification is reaching for example, around say some degree of degrees centigrade the heating is off. Then the LED of

should be powering and so forth. So this is another part of testing. For example electrical iron has sometimes had a thermo state as you might have seen.

And there is something called Silk I think you might have seen then it is call cotton so for all the things you can have different temperature. And if you have different temperatures the thermo stat works accordingly it is so if you have set for the say cotton kind of a cloth and if the temperature is a say around 80 Degrees centigrade or something like that. Then it goes above the switch is off and when is Fossil this world will be different Threshold so you have to now you have to go for that elaborate kind of testing. So you have to set the regulator to woolen, silk, cotton etc. and then again I have to see whether all these functionalities are is like auto cut off then LED glowing etc has to be again has to be tested so in other words.

What I am saying is that you need a very simple, very simple electrical iron you fell that testing can be as simple as plugging on whether it is working whether it is heating or not but in fact this is not the case because whenever you go for a detail functional test. So you can see how elaborated testing becomes. So now let us see the,

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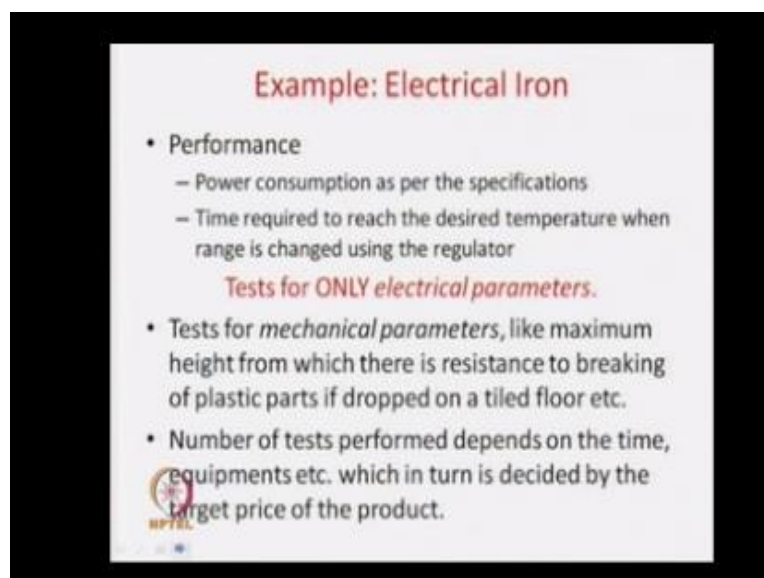

Previous slide we discussed only about the functionalities of the circuit like thermo state settings like cotton and whether light is glowing whether it is heating extra but there are other performance, which is done which is not that must really went directly to an user that is actually performance we say that the heater you say that and now a days the electrical iron is five star comply so that it say the power consumption of the heater on the electric iron is as per specification.

So you also have to see the power consumption. So that is also to be reached then for also some Well branded companies we say that the temperature that will be reached by the iron will be form so for cotton setting or for some silk setting it will be reaches within that within X seconds or 10 seconds or something like that.

That is Performance that my electrical iron is so good let it consume so much power so less power and it reaches the desired temperature in such a low amount of time. So this performance testing also very important, So I mean the more testing you require more time will require and the Test procedure will become more and more complex. Even for our very simple system of a like a classical iron but these are some of the test which are related to the electrical properties of a Iron.

So you can see that the whole Pandora's Box is slowly opening up, so now you can see that there can be some mechanical parameters like you can say that the plastic parts of the electrical iron are unbreakable that is or it is very simple to breaking.

So but on how much so how much distance if I throw it or, how much distance is falls on a wooden floor or it falls on a tile floor what will be the breaking with her whether they will be scratches or not. So there are some kind of another test you may also require to test the mechanical parameters or something like that. So test become so Complex that that you have to have more time for now so now the question is more I do this testing better is my product and better I can advertise it.

So why should I do a less amount of basic physical testing for a common person we can say that we should take as much as possible. That is true if you go for a exhausted kind of testing like for electrical and as I have discussed so what you can get you can get a very good test result and you can say exactly about your error of specification when you are selling.

But now what happen now say for example you are manufacturing 10000 electrical error per day. So testing all the parameters as I have discussed may take even more than an hour or even more than that fine say that my each electrical error satisfy all this properties. So now for each heater you are spending around one hour for testing, so you have to devote man hour you have to devote electricity in your test plan and you have to also devote so many other things. So you are adding into cost, so now actually decided by that.

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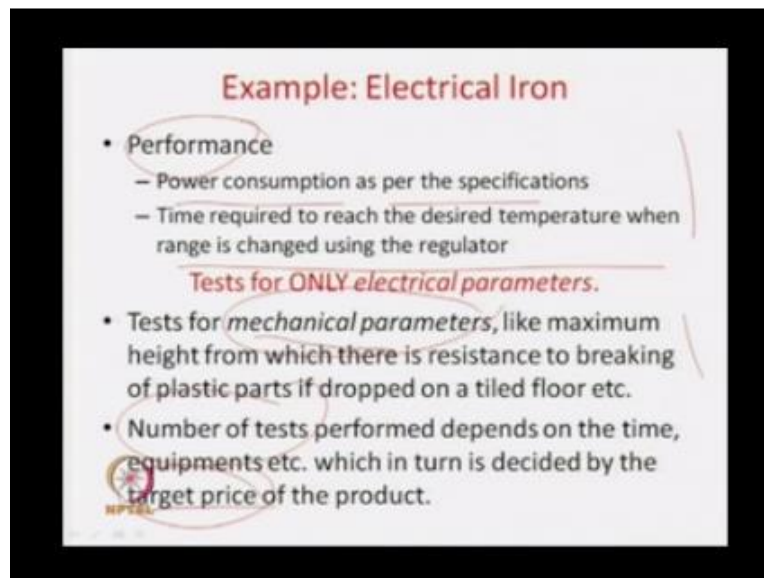

So everything is decided by the target price of the product and some efficiency which will come later. So you can say that if I want to sell my electrical error at 5000 rupees something like that then you can go for the huge amount of it. But as you know in a practical market these things would not survive, people we have very good electrical error and nowadays come below 1000.

So now you have to decide that, I have to make profit in the 1000 or some ex amount of money and at the same time I have to give a reasonably good amount of testing I have to do, so that I can also satisfy the customer. So there is always a trade-off between the number of test performed if you do a large number of tests then you can always go to be very ideal result say that my heater or my whatever performs this, this, this.

But at the same time if you increase the price of your design of your product, so there is always a trade off in between this. So with this we started with a very simple classical example of electrical it was very well known to us.

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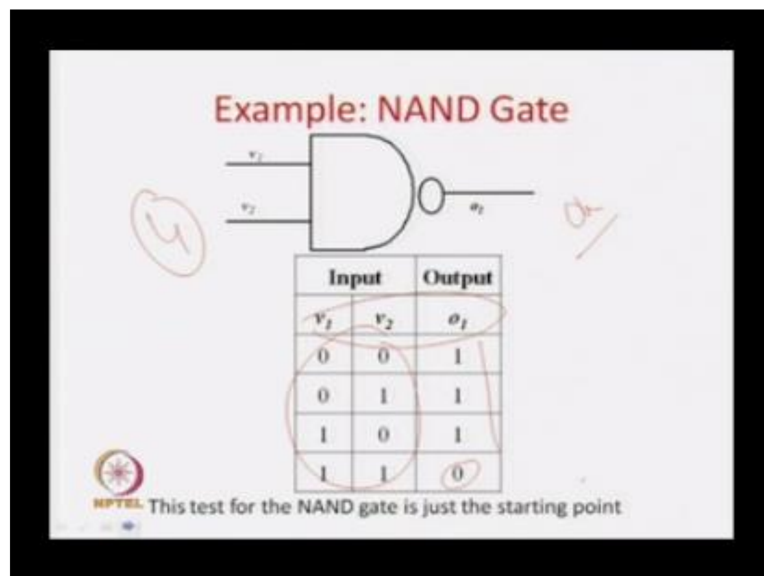

Now slowly we will go to our original course which is on circuit. So we will start off with a very simple and NAND gate, so this is your very simple NAND gate. So now again I need to test the NAND gate. So what is the very first if I give to a person that you have to test a NAND gate so what he has to do? Similarly like an electrical error so you just as the functionally. So what was the test in electrical error just plug it and test it.

So in this case I will go for a functional test, so you can see that I have two inputs and 1 output in this case. So there can be 4 inputs in this case it is 000110 and 11 so these are the input cases. So all the inputs I will give and then I will see whether the output in the first three cases should be 1 and if the input is 11 the answer should be 0. So if I find I know that the gate is okay, I can suddenly get is functionally okay.

So but now you must be surprised to see that this is just the very starting point of testing and NAND gate. So now just like heater sorry, just like an electrical error we will start opening what kind of tests are possible in the NAND gate.

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Detailed tests for the NAND gate

- Digital Functionality
  - Verify input/output of Table 1
- Delay Test
  - 0 to 1: time taken by the gate to rise from 0 to 1.
    - v1=1, v2=1 changed to v1=1, v2=0; After this change in input, time taken by o_1 to change from 0 to 1.
    - v1=1, v2=1 changed to v1=0, v2=1; After this change in input, time taken by o_1 to change from 0 to 1.
    - v1=1, v2=1 changed to v1=0, v2=0; After this change in input, time taken by o_1 to change from 0 to 1.

So see so first is the digital functionality, so it can be done according to the table or what that we already discussed that is all the four patterns 0001, 1011 you give an testing. Now you see, now these are see a NAND gate, so now you have connected it to some kind of a circuit. Now another very important part is the time, so that is a delay, so we might have already started we have already discussed in the first two models that the circuit is working at XZ guard of this time or the time required by an operator.

So an operator like an adder or a multiplier or some hardware is X and X nanoseconds for its frequency is where. So all the speed will depend on the delay that is if some input arise is there and is an output arise here, so what is the time delay of this gate. So in this gate is having a very high time delay. So obviously the whole circuit which will be composed or so many small, small gates will be also large.

And if you want to do go for a minimum delay or you have to increase the frequency or the performance in terms of the speed of the circuit, so this gate should have a low on delay. So that is delay is a very important parameter in case of circuits. So you know that functionality is fine, now if I want to shift my gate or if I have to say that I have manufacture this NAND gate and I want to sell it has a very important parameter is this testing that is actually called the delay test.

Like an electrical error you can say that if I am a very cheap I do not kind of a thing, so I can say that you just drag it into the electrical face and it will start heating, that is the minimum their minimum test. But in case of VLSI circuit like a NAND gate digital functionality is one and the very important functionality which you have to do is a delay test, because unless we say that what is the time required by this gate nobody is going to accept the design.

Because when he is plugging gate into your circuit you should also know that what is the amount of time required by that gate to give the output. Accordingly you can go for this design, because when shipping is product is digital functionality as well as your performance in terms of speed is very important like you might have heard that in case of when you are selling your Pentium processors or AND processors or whatever you say that there are two things that it is Pentium 3 or Pentium 4 or 12 also that case what is basic functionality.

And also it tells that what is the two gigahertz or also one gigahertz, so what that specify that specify that the frequency of the circuit is so much, so there are very, very important parameters which has to be tested. So now how do you go for a delay test, so the delay test will be like from 0 to 1. So initially in the NAND gate these are the gates so initially the output was a 0, now you have to make the output one for some, because of some inputs like maybe the input was in that case say in this gate the input was 11.

And now say input is 00 kind of a thing so in the NAND gate the output will rise. Now the question is how much time it will take to rise. So this is actually this is a very ideal scenario, so these gates are very ideal scenarios. So now you can say that if you are given an input this stuff and then it rises in this where this 0 delay kind of a thing is a very ideal stuff generally we will have a some delay rise.

Now I want to find out what will be this delay will it be one nanosecond will it be point to nanosecond and so forth. So I have to do, now you can see how the complexity it will occur so from 0 to 1 I have to test that is the rising of the output of the NAND gate, so initially if you have, I want to get a 0 over this I have to apply a 11, so v=1 v1=1, v2=1 now you have to find out what is the time required to change the output from 1 to 0 sorry from 0 to 1.

So but in the NAND gate output can be zero or only if the v1=1 and v2=1, but output can be 1 in case of NAND gate in three cases, v1=1, v2=0, v2=1, v1=0, v2=1 and both are 0. So now what you have to do in this NAND gate exhaustively you have to have keep 11 here and then this will be 0 now we apply a 01 over here and see how much time is required for this one to go high. Next to take v1=11 and then you apply v1=0, v2=0 and see how much time is required for the change.

And similarly 11 and from 11 you change to 00 and then you see how much time is required to change. And average you can tell that in the average case this is the time required for the change from 0 to 1 in the NAND gate or also you can say in the case of most case maybe from example form this one to this one the changes required is so much nanosecond. So this is the delay test on 0 to 1.

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Detailed tests for the NAND gate

- Digital Functionality
  - Verify input/output of Table 1
- Delay Test
  - 0 to 1: time taken by the gate to rise from 0 to 1.
    - $v1=1$, $v2=1$ changed to $v1=1$, $v2=0$; After this change in input, time taken by o_1 to change from 0 to 1.
    - $v1=1$, $v2=1$ changed to $v1=0$, $v2=1$; After this change in input, time taken by o_1 to change from 0 to 1.
    - $v1=1$, $v2=1$ changed to $v1=0$, $v2=0$; After this change in input, time taken by o_1 to change from 0 to 1.

And also you can say in the case of worst case may be form example form this one to this one the change required is so much nanosecond, so this is the delay test on 0 to 1.

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Detailed tests for the NAND gate

– 1 to 0: time taken by the gate to fall from 1 to 0.
  - v1=0, v2=0 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.
  - v1=1, v2=0 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.
  - v1=0, v2=1 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.
- Fan-out capability:
  – Number of gates connected at o_1 which can be driven by the NAND gate.

Now again you can also have to have a delay test for 1 to 0, so you know that in a NAND gate already we discussed so we can have a out this curve we are requiring we require how much time is requires for this delay because initially it was one now it is following to 0 it is delay this I required to find out. So initially how do I get the 0 in a NAND gate you know that the answer as to be 11 so all force will be 11but how from where I can reach a 0, we answer is if the inputs are both 00 the answer is one this one and this also from this three input cases if I go this output cases I can get a from 1 to 0 this fall is there.

Again you have to apply the three cases and you have to find out that what is the time delay that has been taken for this fall and then you can again represent that the delay from one to 0 falls is so much in the worst case or in the average cases so much. So this one now we have how many test in now we have done we have done 4 for this visit functionality and then what you can say that now we are doing this delay test, so we are applying another 6 kind of a parameter switches or 6 level input ten inputs still now we have given.

So this was about the functionality of the NAND gate in terms of logic as well as the dealing, now the other important thing which you all sometimes thinking in to picture that this is your

NAND gate in think you might also have seen the fan out case in our previous modules that now that NAND gate can drive or needs to drive several other gate, now the coefficient can be ask that how much gate or what are the drive capability of this fair out, or what is the fair out capability of the derive capability of this NAND gate.

Si I am not going to details of how the test can be done because that is the you requires some complex in to perform this test but again you have to tell that okay this case can pretty well dive so many other gates which so much load in so much time so this about the fair out capability test.

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Detailed tests for the NAND gate

- Power consumption of the gate
  - Static power: measurement of power when the output of the gate is not switching.
  - Dynamic power: measurement of power when the output of the gate switches from 0 to 1 and from 1 to 0.
- Threshold Level
  - Minimum voltage at input considered at logic 1
  - Maximum voltage at input considered at logic 0
  - Voltage at output for logic 1
  - Voltage at output for logic 0
- Test at extreme conditions
  - Performing the tests at temperatures (Low and High Extremes) as claimed in the specification document.

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Tests are for the "logic level" of the NAND gate.

Now again if you look at the digital design as all maintains I have told that we meanly go for six stashing design so one is speed that is frequency speed power and delay, so now so till now we have seen that this what they call the events in the delay and that is the delay that is rise to one fall to 0 so this delay parameter we have testes and we have became report it. Another very important constrain which is say is the power constant that is actually coming in to prominence now a days because of the fact that we are using lot of handle device like a mobile phones your lap tops etc.

So many times you see that our lap top all your processor is working at so much frequency its spend is so much that it is frequency and then at the same time we also say that its power that what is the power of your circuit sorry delay and the speed at the same thing actually I mean area, so will slow after wise we come to area then its what is the area taken by your stuff so the three parameters of designer area delay that is same speed and power this is not speed and delay are the same thing.

Sorry for that so this area delay and power so delay we have already measure then and we can perform the dilators now also you might have for that we sometimes say that your processor like an atom processor is a very low power processor, or it consumes low power so also you have to find out what is the power required by your NAND gate that also you put so if your NAND gate is very powerfully functionally very fine but it takes a lot of amount of power so that may not be also good for your design.

So along with this delay test also you have to go for a power consumption test so I am not going in to details how the power consumption test are done or may be parody complex, so we generally measure two types of power one it is static power that is when the gate is not functioning still there can be some power loss because of leakage and they something called dynamic power that when is your circuit is switching from 0 to 1 and 1 to 0 so there will be also some kind of a power loss that is the dynamic power so you have to measure those power.

Then you can say that the power of my circuit is this much delay of my circuit is the so much functionally it is correct in area we can measure from the design part that is your when you have done your designed your circuit then you have done a back in that is you have done sub lay out and sub division has been then you can also report your area. So area we generate you not cover on the testing but you can directly report this is the area.

So minimum this three parameters we give and this things we generally can verify from your test results and say that your NAND gate is such and such okay, so these are your around you can say that a logic bullion functionality kind of a thing. Now that is the depending on your functionality and all those thing, now another important thing we always say that so slowly you can I am

telling you that to test a basic NAND gate how much sophistication it is so that is how we also started with the very simple example of an error and then we saw that how what are required to be tested in that error to get very good amount of what you called test results or very amount of confidents.

Same thing we are doing for a electrical for a we have VLSI circuit for a NAND gate and then will do the compression to give you the philosophy, so now what another testing that is required we say that logic 0 and logic 1 basically nothing call logic 0 and logic one there is some voltage that corresponds to logic 0 and there is some voltage corresponds to logic one generally we can see that if this is the say some kind of circuit say five volts is consider as a upper threshold and say 0m we considers the 0 volt we consider at the low as threshold.

Then we can see that if anything is around above 4. 8 volts and to say 5.2 volts or something so we can call this is the logic one and logic 0 we can say that If the voltage is up to say 0.3 volts or something which is there a logic 0 so this specification I say that if I get something with less than 0.3 volts or below I call it logic 0 and from 4.8 volts to 5.2 volts I consider logic one now again all that test I have done for zeros and Ones I have to apply this all the inputs in the NAND gate in the table one as you already seen that we apply 0001 10 and 11 and then we get the answer say 11 and then we get 111 and after some pattern we give the answer zero.

Now for each you have to measure what is voltage like for all the ones voltage level should be within 4.8 volts to 5.8 volts and for 0 volt it should be within say 0.34 so now you have to measure all these things using analog techniques because digitally we cannot measure those kind of a stuff and then you have to find out that this all the voltages at the logic 0 and logic 1 and everything is meeting so Logic 0 and logic 1 compatible with input voltage like this.

Now again I know that you suck it can be subjected to and the set of test so you can be subjected to very extreme conditions that can be subjected your, we say that your VLSI are device or whatever will work properly. Say for example say 5^0 centigrade to around say 6^0 centigrade kind of for the we generally write that so your device will work properly within so and so simple with that is there military grade equipment we said that it operates from 60^0 centigrade kind of a stuff

just an example they not be correct but say some form minus exhibition to some classic degree centigrade, so all the test which I have done now have to be done for extreme low and high extremes which is actually scrammed in the specification documents.

So if it is temperature do all the operations are such an high temperature and also if you are some specific is like and work at so much pressure of the marker and so for so all the test we have done have to be also verified at this high extreme test conditions will be applied and then only we can say that your NAND gate is actually operating at this or it is satisfying all the condition which is required in the specification document as well as it is it all the things or your a NAND gate will operate functionally correct and with all the parameters lectures like it is like power consumption threshold delay etc, within so and so degree of such temperature and so and so degree of pressure.

So now we can understand the complexity that for a simple NAND gate with two input how what is the amount of test I have to do to assure that it works at so and so frequency it operates at so much and so delay it takes what do you call this amount of power and this is the voltage levels and it operates are this are the so all the things I have to do for simple NAND gate you can understand the complexity of testing a circuit to assure that.

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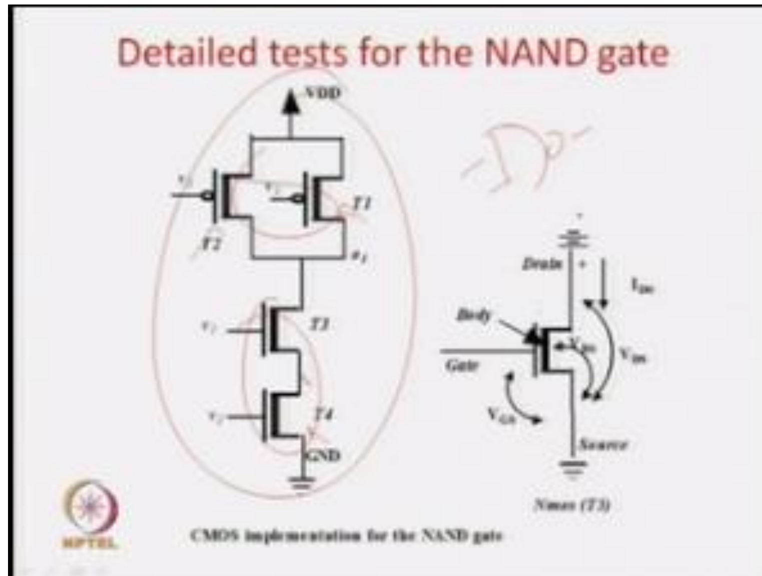

So assure that it is operating properly. So this till now we were talking about the NAND gate only from the logic level point of view that it is a digital NAND gate. But actually if you look at the NAND gate from internal sol it is not a simple NAND gate it is not just like a digital stuff you understand inside it will look like this it has to pre most on this test it is just ten mass on design it is corrected in this way.

Now if you want to say that your NAND gate operates properly sometimes we have to go for detail test of this transistors okay and then only we can say that your transistor or this four transistor operating properly so we can guaranty much better test or much better specification coverage for the NAND gate so I will not going to very details of how the test of this mash facts are done because they are part of analog testing for just to give an idea.

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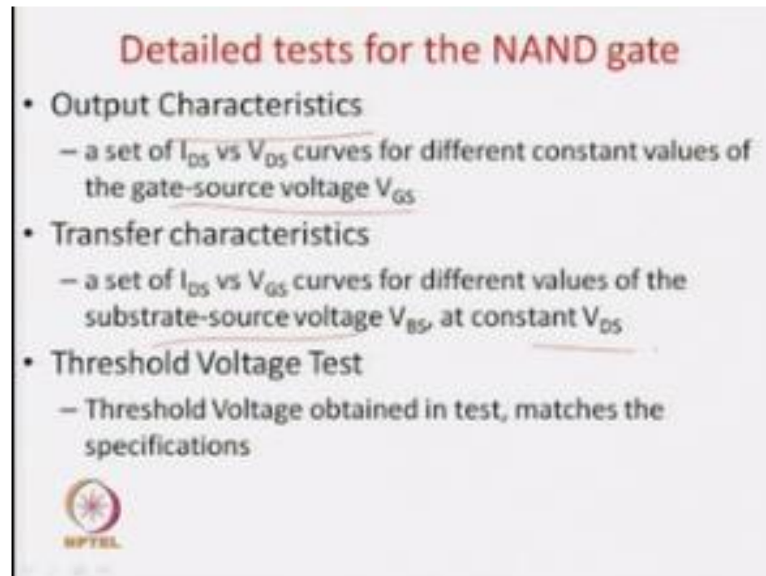

But actually if you look at the NAND gate from internal so it is not a simple NAND gate is not just like a digital stuff you understand inside it will look like this, it has to p most transistor is used to in motion design is connected in this way now if you want to say that your NAND gate operate properly, some time sometimes we have to go for details test of this transistor okay, and then only we can say this of your transit this four transistor is operating properly.

So we can guarantee much better test or much better specification coverage for the NAND gate. So I will not going to very details of the test of this Sudden because a part that part of analogue testing just to give you an idea so you can see you have to find out the out characteristics of all the transistors like a set of input current but his input voltage current for different values of volt to dins sources then also there can be trans again some threshold voltage test for some transistors also be some sub state source voltages for constant Vgs. So they did not going to the details.

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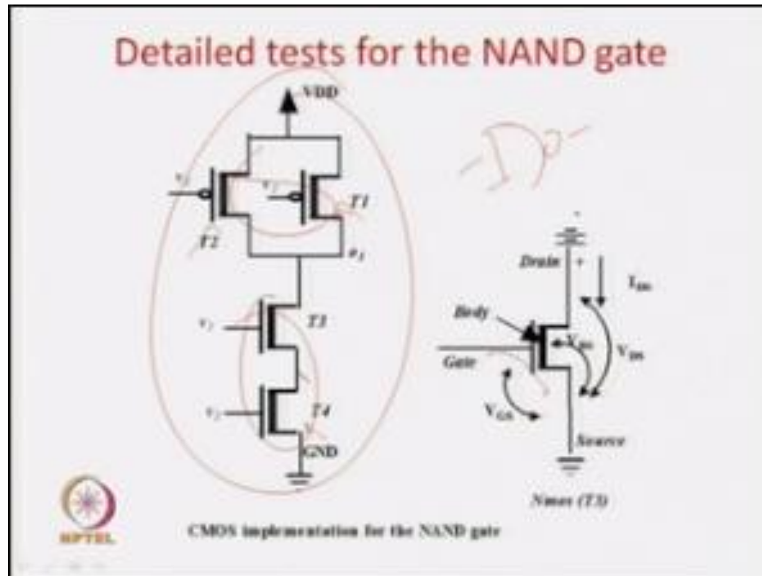

But for each of the transistors like this we are testing what is the voltage what is the this current versus this voltage at this constant this one and so some of the parameters we are giving constant and we are starting the voltage versus the current for this type of thing and all the transistors we are doing that and then we are reporting the results, so more depth we go more amount of test are coming in to picture for NAND gate

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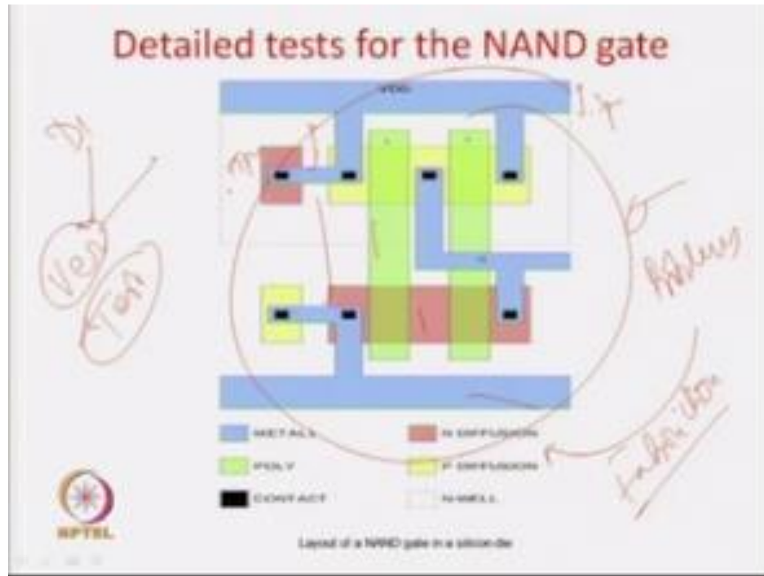

So that was about the transistor level design. But now our transistor is design the transistor is when you are laying out the transistor in a physical back end or in a VLSI circuit so your one single gate NAND gate generally looks like this, so this is your metal so this is your end diffusion this is you poly so this is a physical layout of your circuit now if I want to test this things will become much more complex and the device required are now you have a electron micro scope kind of a thing because now I say that for a NAND gate I say that this specification is a fine 0.5 micron.

So if this much more than that then I can say that you not as from a specification we can also say that the distance between say these two metals should be say 0.7 micron or some specification now after this has been made out now you can go for a very complex micro scope or the several other very complex needs to find out whether whatever was the minimum requirement for those kind of a NAND gate is have properly laid out.

Because laying out or circuit out fabricated is circuit is also very complex proceed your so we do not know that after the fabrication because all the fault you know circuit as well as I looking in this series of lectures on testing when they are happens because there are some what you can all

that is problems some problems in this fabrication. That is the main thing so if I tell you what is the difference between verification and test so verification what do you verify you verify that I wanted to design a NAND gate.

So whether if I really written a code that actually had the adder so that what I verify that it is functionally what I intend it to design what I have designed or not, so if there is any failure in this verification phase then you can be sure that it was happen because it was the designer mistake but when we say that testing so what does testing verify the testing verify that I have my design say D1 I have verified it so if I verified it that means all my mistakes have been taken care of.

And now I am getting are designed to see which is functionally correct that means whatever code I have written that actually implement the specification now this D2 will be manufacture and say manufacture you say I achieve get is manufacturing say A1 so what is the manufactured cheap look like for the NAND gate it will be basically looking like this in a dye.

So now this a fabrication process of the manufacture process are lot of imperfections, so we will slowly see why they are so because of this imperfection this M1 may not be equivalent to your D2 so testing procedure basically test weather are have been problem in the manufacturing step that where M1 is not be coming equivalent to D2 so that is why to less we have to find out whether this has been la down weather this thickness is proper or not and we test equipments and test level numerously and you the externally high if you are going for a test at this level.

So what we have seen is that basically with this the layout of a NAND gate then you as the transited level of a NAND gate then you have seen that electrical parameters of the NAND like delay power and then simply the functionality a NAND gate 011011 1011 kind of test so more depth you go the more number of tests we have to do for a relay circuit as in the system away understand that are model typical persona as million of 2 input NAND gates.

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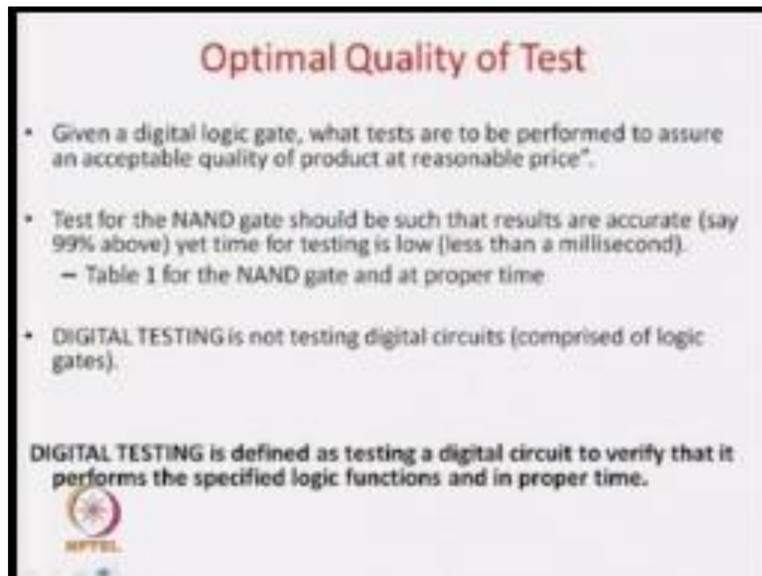

So you can understand that what is the complexity of testing so what is the basic idea our idea of testing as I already repeat that for in case of the NAND gate of for whatever circuitries that your actually as should be very high more than 99% and your testing should be very low see even less than a Millie second because they told a circuit may have millions of gates and if you start taking one to one or even one or two seconds for one cheap to 1 C1 circuit will take 1 million seconds to do it with may run in days and we now that for a single design we fabricate millions of circuits and we let they market it.

So you test producer here will run into 100 of year so that is not possible. So what we have to do we have to have as high as 99% accuracy as we have to take test should less than a mile second so all digital testing procedure or digital is planning how can we achieve this matching so between this course will see that so now digital testing is not say that so if you say me ask me what is digital testing so for my 11 point of you or from a is no experience you will say that digital testing is testing results are.

But it to be own resize it is not testing the digital circuit because digital circuit testing we have seen such a complex is case of NAND gate so you have to go for functional testing speed testing

delay testing power testing threshold testing and then for the layout so that is very complex even if I start doing this I will take even more than one hour to test a circuit and one gate and a circuit will be in days and for 1 million circuit will be in you it will be Ares so basically I denote have time for such a sophisticated thing.

So basically digital testing is defined testing a digital circuit to verify that it is performs the specified logical functions and in proper time that is I am not much bothered whether it is taking weather the layout is proper or not or whether it is there some issues in the poly on some stuff so basic this is actually we should solve the basic because more or if you become is to call it sophisticated digital testing or advanced digital testing then it will become more complex the very busy very digital testing is that I want to know that my digital NAND gate is performing proper in case of 0001 1011 11011 and it as to give me result proper time.

If this is done more or less my basic digital testing is open so digital touch circuit is not about testing the digital circuit entirely which you have seen the last two slides but it is basically this slides. I want to go for advanced testing so all things will come into picture okay.

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VLSI circuit testing Versus Classical System Testing

VLSI Testing	Classical Systems
Technology matures and faults tend to decrease, a new technology based on lower sub-micron devices evolves	Basic technology is matured and well tested
Diagnosed and repaired	Binned as defective and scrapped (i.e., not repaired)
Yield is Low	Yield is almost 100%
Expensive equipments and Specialized Manpower	Simple Test Setups and Technicians
All Samples to be tested	Random Sample Testing
Test arrangements in design	Rarely Required

So now we have seen about two what you call two systems one was the classical system of hyper and one was the gate now let us just have very quick look at what is this what is the basic difference of a basic similarity between in this so in case of classical system we never go on for a very complex string like a electrical which I have mentioned we generally do a very film nary test and then you are satisfied now why but for circuit we have to do it we have to excitably test all the circuit I having much more complex there are system.

But why this so because in case of electric system the technology very well mature but we all know how to design the electrical error and it is and the technique is the reaming similar for last say 30 to 40 years the style modification so whatever we produce are more or less grunted to be over the pipe.

So random test random testing kind of a thing with a few more samples is fine but in case of now we have what Technology say 0.5 micron technology so we are having lot of problems with the technology manufacturing is not proper then we quickly go for we are having lot of issues of some tests are pending but still we are going for 0.5 micro technology now due to market pressure some others company say come up with a point 25 micro technology.

So even the more 0.5 micron as matured and there is very little scope for errors and technology coming into the market because you are getting to get better performance in those nor some micron then we quickly moving to new technologies so even before a technology matures and send to decrease that is technology is matured and stabilized we go on for new and newer technology so always false are enormous is number and testing is a prominent thing that has to be done.

But in case of classical systems so other way out so another important part I will go this part come to later this is slowly we will move to the course and then will come in the end so another so now in case of classical systems we say that yield is always 100% that may get 1000 electrical errors our can know say around 99 will be operating or may be all 100 will be can be solved with little repairing but in case of circuit idea is not the because the technology is always

maturing so in the event as well 50% that I made 100 chips 50 after I thorough them of only 50 will survive.

Then that is why id such a high amount of failures are there so you have to go on for testing each and every part because if I miss them is a very high probability that I can ship you on the customer fault chip but sill how the VLSI will profit because they can sell it a slightly higher price that is not the issues but I always have to be at part the market that is if I have a very nice Nokia mobile phone or very nice Motorola phone I will go for that event that a very old kind of a phone because always the technology is maturing in case of VLSI and we are getting newer and newer gadgets.

So I can slightly go buy a higher price if I get a very good gadget that is what is the or a very good performance so that is why we all are going towards newer and newer technology even if there are errors or even if there are faults so that 50 % of my service I am ready to throughout but still I have to catch up with the market of the latest trends so with high number of faults so that's I why testing is so important secondly in case of classical system test are very simple just you plug it on or even a simple then circuit can do your test but each in case of this electrical but VLSI circuits as we have seen for NAND gate.

It is a very difficult process you can see that you require microscope sometimes you required sometimes at that terms so very experience equipments are required for this one and test arrangements I will tell you so next is so this array samples so as I told you that in case even this is almost 100% so almost all circuits are operating files so you require as less as say around say 1 or 2 random samples you can test and find but in case of citrates all these gates as to be tested.

So because the number of what you call the number of faults can very high as 50% of the circuits may fault so all samples has to be tested, so that is why each and each very unit has to be tested in case of circuits while in case of classical system like iron or heater or something so as the number of faults are very less so you can even take 3 or 4 random samples and you can do it, so now we will slowly see in this circuit basically about these two parts these are not very I mean we cannot explain in this initial lecture.

That is in case of circuits we generally do not go for repair and in case of classical system if you find some repair we can if you find out some system some of the electrical and not some system have a fault and you generally go for repairing and then we sold it sell it in the picture but in this kind of VLSI circuit test arrangements I mean basically it is not required we have something we test it and then we find out that there is some problems in case of the VLSI testing is not performing finally.

We generally then throw them out that is we do not believe in what you call repairing and all those things so this is basics some difference in VLSI testing as compared from classical testing but some of this things like this arrangements in the design okay and test you know such type of stuff in case of classical systems, we will slowly see this points like billing and defective non repairing so these parts will slowly see when will going to the other parts of your mean slowly we will go progress through the course.

So basic differencing is of normal testing and a classical testing as well as well as the system I mean VLSI testing is that classical testing almost all the products are correct so random resting we so and very simple kind of test so even a technician can so but in case of VLSI around say 40 to 50% or even more then that circuit can have defect so you have to have all the circuit tested and the test procedure is quite expensive so you have really sophisticated instruments and engineers to do that.

So that is the very basic difference between normal classical testing as well as system testing, so compared to classical systems in VLSI testing it occupies a very, very important parameter so in therefore in our course we have kept one third module only for testing, so let us slowly go into the course.

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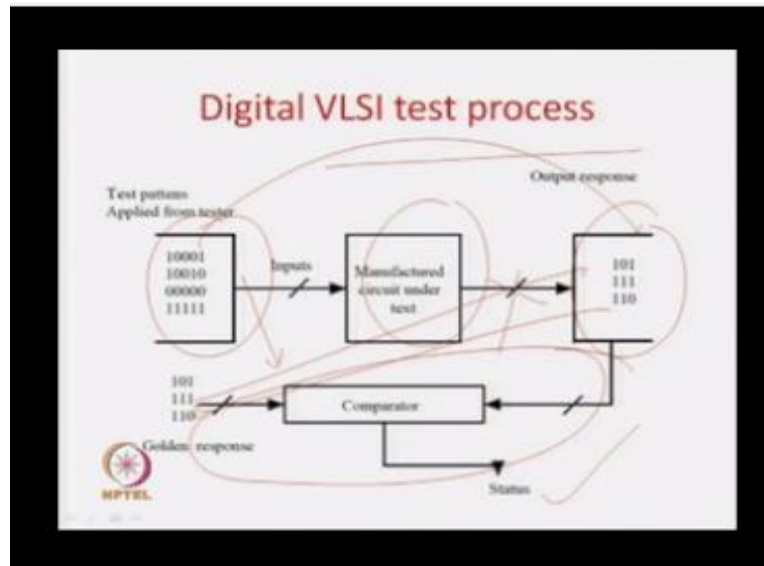

Basic introduction so in case of circuit so what we will have, We have manufacture circuit we give the inputs now these inputs as I told you should be as less in number as possible then there is a golden response that is we know that for this input this should be output then this is the comparator so it compares this output with the golden response and if all the responses match we say that the circuiting is operating fine.

And also we also measure the delay in this case of requirement so if this is the process then we say the circuit is correct otherwise if there is a some mismatch between this and this then we say that these are fault and this circuit can be scraped or that is it means it can be declared as a faulty circuit so this is the basic digital test process.

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So this is an equipment automatic now if I have told you that I have to do testing of power, delay so and so, so basically whatever test equipment look like, this is the automatic test equipment we call in AT so this is the test equipment here we put this circuits in a dye I this case and this big equipment and oscilloscope, CRO generator logical analyzer and then the most of the testing for the, so this is the automatic testing equipment and is a extremely expensive equipment and very big companies can only can afford this instrument that we have to understand.

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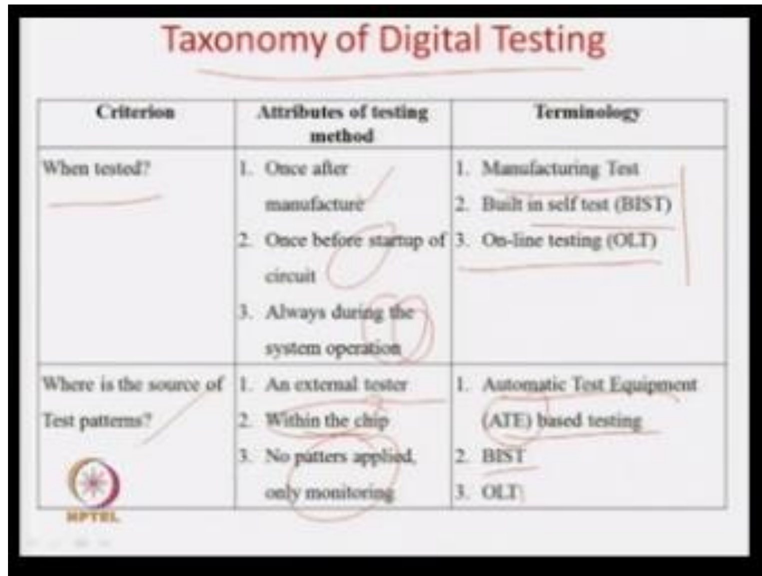

Criterion	Attributes of testing method	Terminology
When tested?	1. Once after manufacture 2. Once before startup of circuit 3. Always during the system operation	1. Manufacturing Test 2. Built in self test (BIST) 3. On-line testing (OLT)
Where is the source of Test patterns?	1. An external tester 2. Within the chip 3. No patters applied, only monitoring	1. Automatic Test Equipment (ATE) based testing 2. BIST 3. OLT

So now before we go in more details let us see what are the taxonomy of testing that, what are the different types of testing that is available in the market, so first question is when tested that is the criteria when do you want to test the circuit. So if you just do it before the manufacture then it is called the manufacturing test, also after this circuit has been manufactured and I just been sold in the market now it is in your laptop on in your palm top or your PDA.

There are and that time also you can have false so before the circuits starts with operation I can always have my circuit tested that is I can your PC whenever you start your PC it shows that the RAM is being tested and if the all the RAM is by gives that okay and the circuit goes so therefore many of the circuits are tested every time before this circuit starts that is actually recall built in self test that is circuit test itself when the circuit is starting in operation and for very vision critical systems like nuclear, plant or air lines, flights or rockets you can understand that the circuit should also be tested every time or concurrently when it is doing its operation.

That circuit is operating and the same time you have to say that you have to test itself so that is actually fault tolerance that is every time the circuit is all the time circuit is operating apparatus is more entering for its operation, so these things are for mission critical applications like

avionics' nuclear plants etc, so then it is called all line testing, the circuit is operating as well as the same time you are for testing the circuit.

So when the circuit is testing these are the basic terminology, now the question can be asked, who apply the test patterns like we have seen for the NAND gate 0001, 10 and 11 now the question can be asked with applying the test patterns, so if it is a manufacturing test the ATE example I have shown you, so that is an ATE as a equipment so if the equipment applies the test pattern we call it the ATE best testing like now in a best so what is a best, best is build in self test so in this case what happens.

Circuit is doing with operation I mean it is starting is operation before that we are applying some test patterns and we are getting a response, now if I have manufacturer circuit and I put it in your laptop obviously you cannot bring the ATE machine and test yourself so in that case the test pattern generate a and the test pattern and response analyzer are within your circuit, so this is the we will slowly see it was the end of the course we will see how it is done.

For equipment is simple you apply the patterns you observe the response but now the whole best of 80 circuit a miniature version output in the circuit then this patterns can be applied from the circuit and also it can be analyzed in the circuit also, so in the pattern are applied within the chip then in the case of a best and now you see what is the case of online monitoring in online monitoring what happens.

The circuit is doing its normal operation you are just monitoring, so obviously in this case you cannot apply any pattern circuit the circuit is doing its operation more patterns are applied you are only monitoring and then you are judging whether the circuit is behaving properly or not.

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Taxonomy of Digital Testing

Criterion	Attributes of testing method	Terminology
Circuit in which form is being tested?	Wafer IC Board System	1. Non packaged IC level testing 2. Packaged level testing 3. Board level testing 4. System level testing
How are the test patterns applied?	1. In a fixed predetermined order 2. Depending on results	Static Testing Adaptive testing

Now that criteria is in which format is tested, so I think I see you have seen we are all have seen that this is a back chip with some pins here and there it is called the IC so circuit has been fabricated and you want to test it so this is actually called package level testing this circuit has been packaged and you want to do testing, actually they have wafers now we have also seen in a both so you can have a PCB kind of a thing, so you have I think all of you might have seen this is per printed circuit board.

And you have chips which are interconnected so this is called the board level testing circuit has already been in the board now how can you test it, in case of a IC you can apply pattern in all the points but in case of a board you can only apply the P that else which are the input output of the board it is very difficult to control a pin here okay in this circuit because this PIN is already connected to another part of the circuit.

So directly getting an access to the very difficult but if it is in a IC level thing you can easily all the pins so if this chips are with are placed on us board and you are doing a testing is it actually call the broad level testing, now all the many number of PC these are connected and you have a

made a system like a PC or laptop then now you have to do the testing so it is more difficult because in IC you can get access to the all the things of the IC.

Now if I put in a board you can access only the PINS which are in the input output of the PCB all inputs output of the IC you cannot get it now if I go for the system which is called the system level testing, testing somewhat because more difficult because now all the PCB are connected in a system and you can have access to only input output of the four system this is the system there were many PCB's in the PCB there are many IC's.

But you can only access the input output of the PCB, internally you can access. Now there is something call wafer, wafer is nothing but when the circuit is fabricated it is a die and inside the die you will have a wafer, this is the direct circuit with this circuit is actually put in to IC and then this is package.

So directly with the wafer can also be tested because it is very easy to I mean get access to all the pins like for example if you have a IC like this so they are lot of many, many, many gates only few of them you can be access at the pin of the IC. But if you accessing then it will be die so you can access many more pins of it, so more system level you go less is the number of pins you can access and les more difficult in the testing so this is a very raw testing which call non-packets IC level test you can have lot of pins.

So no lower you go the or more abstract level you go the less number of pins you are having and so forth, so but these are the different levels of testing in terms of when the circuit is testing. Now the course how with the test pattern apply so there can be two things you can have tactic you can plan ahead then what you want to apply and also it can be adaptive level depending on the output performance of the test you can change your test patterns.

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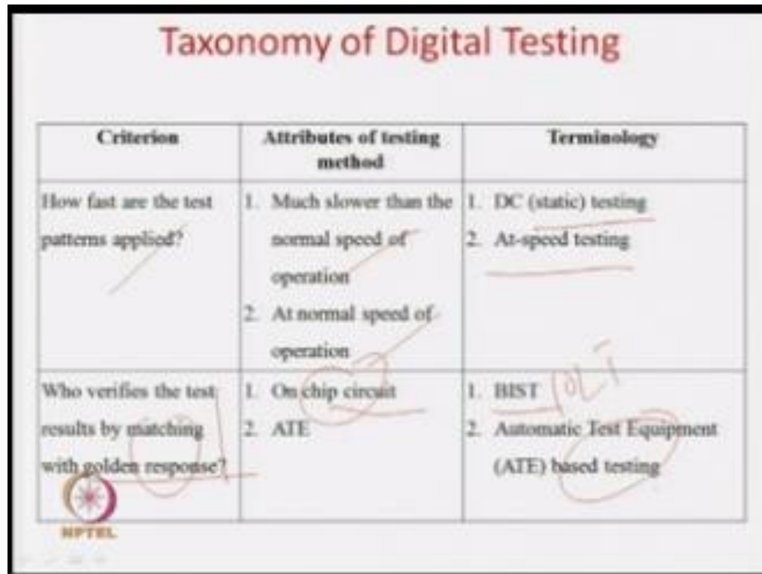

Then there is few others like how fast is the test pattern applied so if you are doing at the normal speed of operation that you are testing at Giga hertz it is called at speed testing but if you tester or you cannot supply speed test that is at that level you can do much slower than it is call DC or this is slow testing. Now again who verifies the response of the output that they say be some person should response match the golden response.

So if it is in case of an automatic test equipment the equipment have everything but in case of BIST that in case of a circuit or online tester or in case of building say if it is the on chip there should be an open chip circuit because in case of BIST the chip is doing the online testing sorry, the BIST is doing the BIST circuit is doing the testing in case of online testing the circuit on GB is doing the monitory so in this case the response analyzer sits within the on the chip.

So then in this case if the person who matches the golden response on GB you can call it BIST online testing and in case of ATE, it is ATE based testing knew the equipment will do everything for you.

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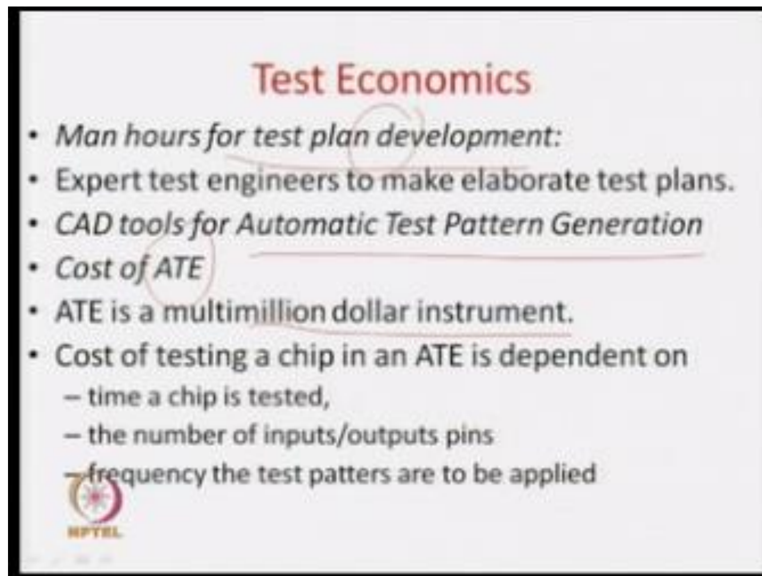

Now what do you gain and what do you pay, so to pay what you have to do you have to make test plan you require testing engineers you require automatic test equipment which I have shown is a extremely expensive equipment so more is a multi dollar equipment so more time you spend on new tester that many amount of money you have to give that is more amount of test patterns or more test you want to do and more amount of time you have to use the ATE and more amount of test you have to pay.

And if you making a very intelligent test plan then you have to pay the engineers, right so that is the test now every if you increase the test time then you have to use more amount of ATE and more amount of money you have to pay, and but if you make a very intelligent kind of a test plan so that with less amount of equipment patterns you can test your circuit then you should have a very good test plan.

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Test Economics

- DFT/BIST circuitry
  - Additional circuitry kept on-chip to help in testing results in raise in chip area
  - Rise in area power and lower yield
- At-speed testing by ATE is extremely expensive.

Tradeoff

- Returns
  - Proper binning of Chips:

In case of VLSI testing, it is not of much concern as how many chips are binned as faulty, rather important is how many faulty chips are binned as normal.

But again than then you have to be very sophisticated or very highly skilled man power is required which will again take the money, so whole testing process is basically about trade off of economics. Like now these some people say that if your ATE equipment is very expensive why not you could some extra circuitry on chip which can do a part of the testing for you in that case your some of the patterns can be applied from the ATE and some of the patterns can be applied from the on chip circuit.

So this things will be see in details so that which we are again doing the tradeoff between the ATE and your circuit like my ATE is the third party to third party equipments so I have to be very ATE even that, so I have to apply some amount of testing I can do on chips circuitry like BIST or online testing kind of a stuff or some circuit I could on chip to the testing then I can say some time or some amount of patterns in ATE.

So but again I have to increase my chip area then again there is a tradeoff that where do I should pay the ATE vendor or whether I put some extra circuitry on the chip for testing and I make the chip size. But now what do I get I get a proper binning of chips, testing in case of VLSI will

never assure that all the chips are correct or I will repair my circuits so well I can say all my circuit that is our difference between VLSI testing and a classical system.

Classical system you test a circuit then you say that all I repair all my some irons if I find in faulty I repair them and then I sell off through the market. But in case of VLSI circuit is not that some if the out from 100 say some 60% circuits are fine which is good and some 40% circuits are bad which I have to through them out. Now what are my circuits VLSI testing is emitting a thing a very proper portioning of 60 and 40.

If I somehow sell a defective bad circuit into a good look and I sell it to a person then that will be a big problem. so that is how test economics will what it will help me test economic basically will give me a very proper kind of, it will give me inside it is seen that in case of it is VLSI testing is not proper concern that how many chips are being faulty, it is another important that how many faulty chips are binned as normal.

That if you have a faulty chip you bin it and in how does sell it to a person the person will have a defective chip in his because it is sold to him that will be bad representation on the country. So amongst and because there is no scope of repairing a circuit, so what we have to do our testing will give you a what you call good circuits as good and bad circuit as bad.

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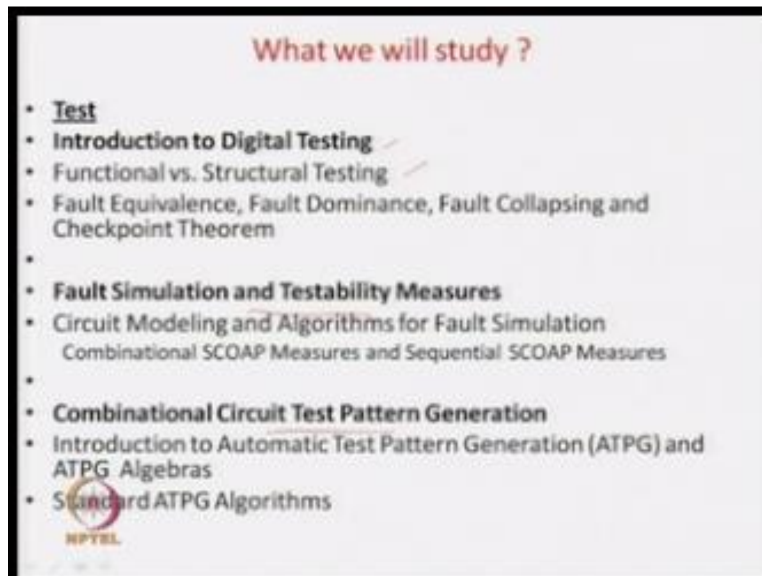

So that you can go for a what you call a proper VLSI testing that is good is being as good fault is being as fault and then you give the proper thing to the circuit. So in this course what we are now these was the very introduction to digital circuit testing the basic philosophy I have told you and what is the difference between classical testing and VLSI testing I have told you because till now in our mind we have the ideas of classical system.

But now I have explained you that VLSI testing philosophy of VLSI be different from classical system, so in this third module what we are going to read so today we have about introduction next in the few lectures we will be looking at structural verses functional testing and so forth then we will go for fault simulation then we will see combinational circuit test pattern generation.

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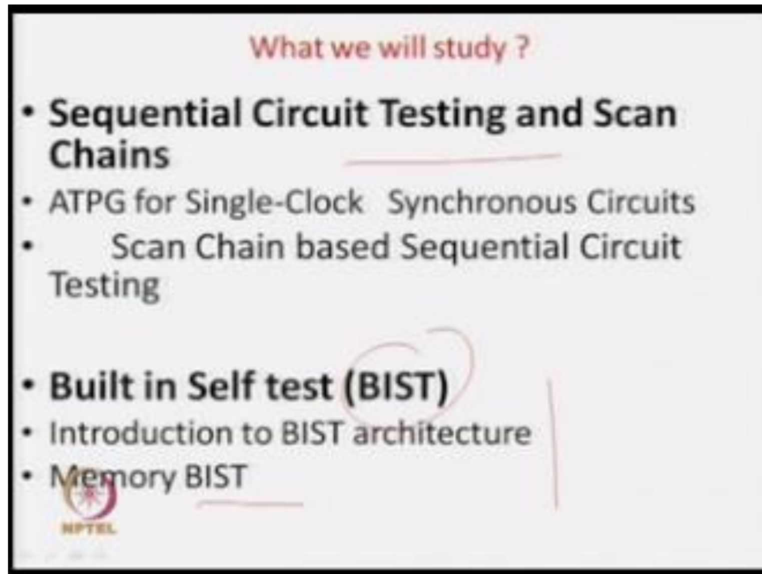

Then we will go sequential circuit test pattern generation and finally we will see if I have to put all the testers on chip that is build in self test how it will go and then we will also see if something like build in self test and maybe some ideal online monitoring.

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So with this we come to the conclusion of the first lecture in case of VLSI testing that was the introduction in the next class we will see that how we can intelligently develop test patterns or how we can intelligently plan test so that I apply we less number of test patterns here get a very good confidence that my coverage is very good that whatever binning I am doing is proper, thank you.

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