INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

NPTEL

NPTEL ONLINE CERTIFICATION COURSE
An Initiative of MHRD

VLI Design, Verification & Test

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Welcome in this module we will start our discussion on geometric synthesis or physical design geometric synthesis or physical design comes after the logic synthesis step at the end of the logic synthesis and technology mapping step we have a detailed circuit diagram of the chip of the functionality that we want to implement in terms of cells macros gates and transistors that will be used in the design and their inter connections. At the beginning of the physical design step the circuit diagram is usually represented as a data structure called net list.

Net list is a graph like structure in which the nodes are the modules that is the cells macros transistors gates that we just mentioned and the edges are the inter connections. So the edges will be if two cells are connected via wires there will be an interconnection between these two modules and this will be represented in the net list as an edge.

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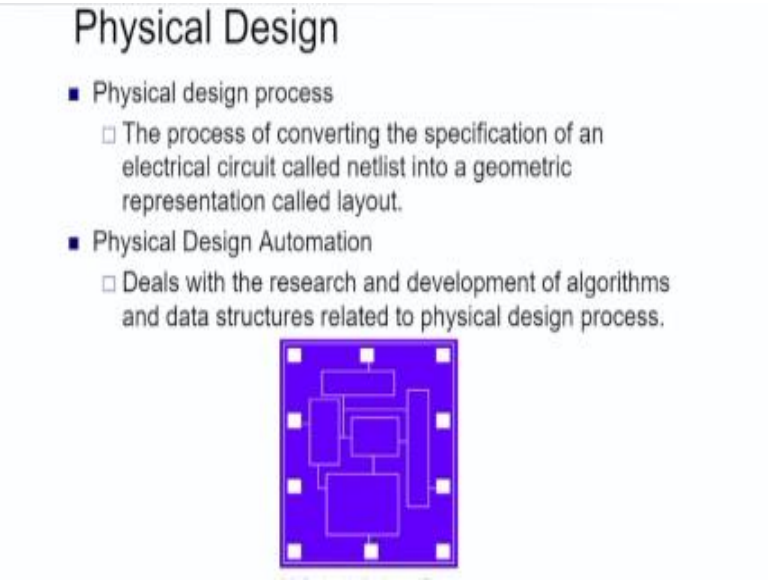

So what is the physical design process given this net list to obtain a geometrical layout the process of converting the specification of an electrical circuit called net list into a geometric representation card layout the diagram that we have shown below is an example of a layout on this layout we express here the floor of a chip the entire blue square box is the floor of the chip on the periphery of the chip PC terminals and there are blocks these rectangular boxes that are shown in this diagram are the circuit blocks.

We are also seeing here that this circuit locks are connected through wires. So the chip area will be covered by three main types of components one are the terminals here scene which takes very less space, the blocks that is the circuit blocks themselves the logic block and we need area for interconnection between the blocks. So the physical design process is very complicated because the circuit diagram form from which we have to obtain.

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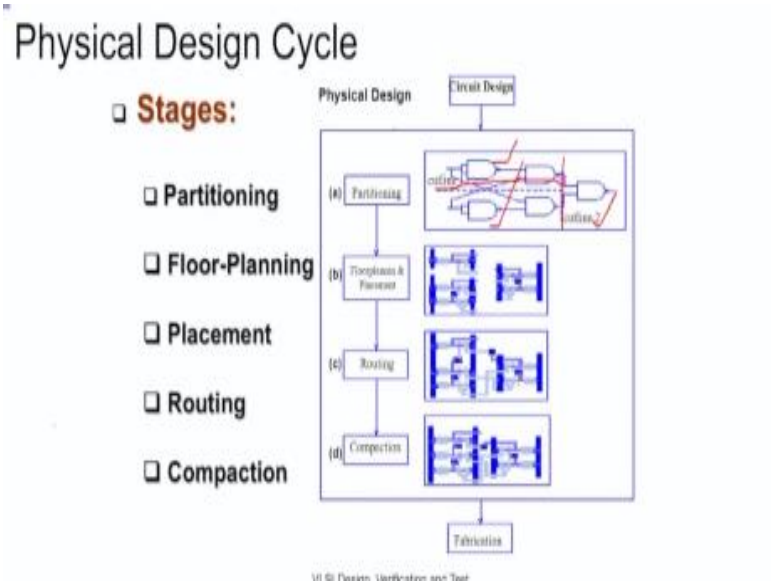

The final geometric layout can be very huge consisting of millions of transistors interconnected in very complex ways and we have to obtain an optimized layout which tries to minimize the chip area say would be minimizing the critical length of a wire in the whole design in the need to maximize performance in the face of constraints such as limited area number of metal layers or routing layers available extra.

And hence the whole physical design process has been divided into a set of stages or steps. The first step is partitioning in the partitioning process we partition the entire big circuit diagram that we have into controllable sub circuits or sub partitions this circuit here who has been divided into three partitions using to cut lines cut line one and cut line two and we have three partitions partition one partition two and partition three.

After the partitioning process each of these partitions will be called a block and there will be interconnections among blocks so each block will have a specific geometric properties because in this block we will now have a fairly good idea of what are the components in these blocks how are they interconnected. So we will get an approximate size and shape of each block as well at the output of the partitioning process.

So hence at the output of the partitioning process we will have blocks along with that interconnections. Now these blocks have to be placed on the floor of the chip this is done in two steps of floor planning and placement. In the floor planning step we place the blocks such that no two blocks overlap and the area of the whole chip after their placement on the floor can be minimized. We also want to minimize a total routing area required as well.

So after the floor planning step we come to the placement step where we find the exact coordinates of the blocks on the floor of the chip in the floor planning phase we only obtain a relative order of placement of the blocks on the floor of the chip we don't get the exact coordinates for each block.

At the placement phase we obtain the exact coordinates of each block. In the routing phase what we do is we obtain for each wire connecting the blocks a set of areas through which it will be interconnected so we have areas between the blocks the vacant place within the blocks will be divided into structures called channels and we will switch boxes and we have to route each wire each interconnection between two every two blocks through these vacant spaces and over also over the top of the blocks and connect these blocks. This is done in the routing phase in the compaction phase what we do is to reduce the size of the entire circuit to obtain.

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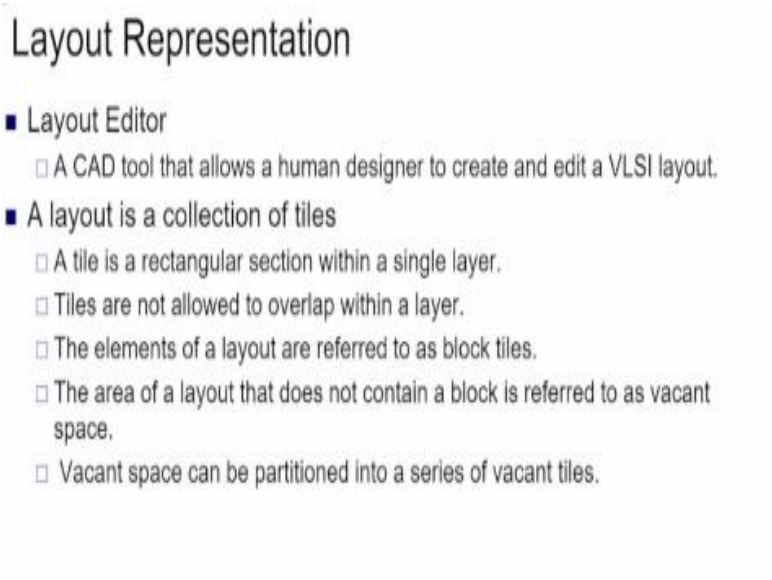

Now before going into the algorithms we need to understand how do we represent and manipulate a layout through the design process. So the layout is manipulated through a CAD tool current layout editor so layout editor is a CAD tool that allows a human designer to create and edit VLSI layouts. So what do we have in a layout? A layout contains a tiles a tile is a rectangular section within a single layer tiles are not allowed to overlap with in a layer.

So within a given layer I cannot overlap two tiles the elements of a layout are referred to as block tiles so we will have blocked tiles and vacant tiles. The blocks in the circuit will be represented as block tiles the vacant spaces will be represented as vacant tile the area of the layout that does not contain a block is referred to as the vacant space. The vacant step space can be partitioned into a series of vacant tiles.

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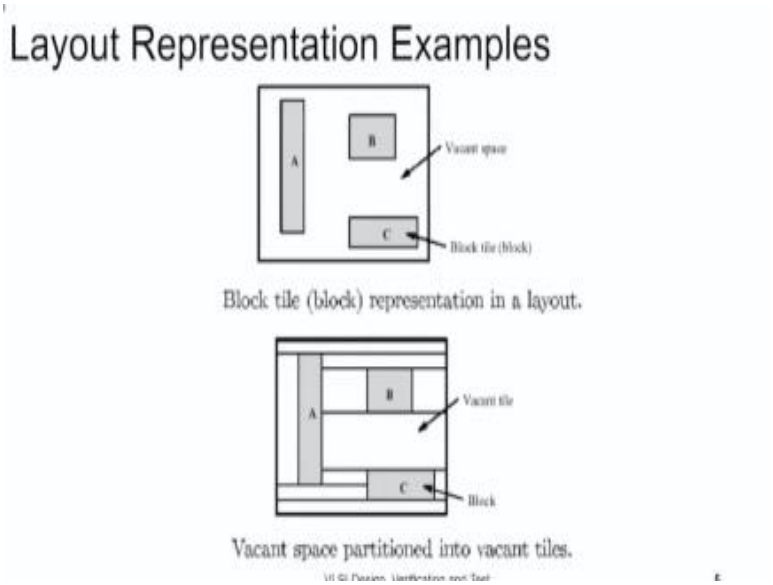

So here we represent an example we have three circuit blocks A B and C and we have this vacant space here. Now here we have also divided the vacant space into tiles so these are vacant tiles. These will be vacant tiles and these are block tiles right the vacant space is also partitioned into vacant types.

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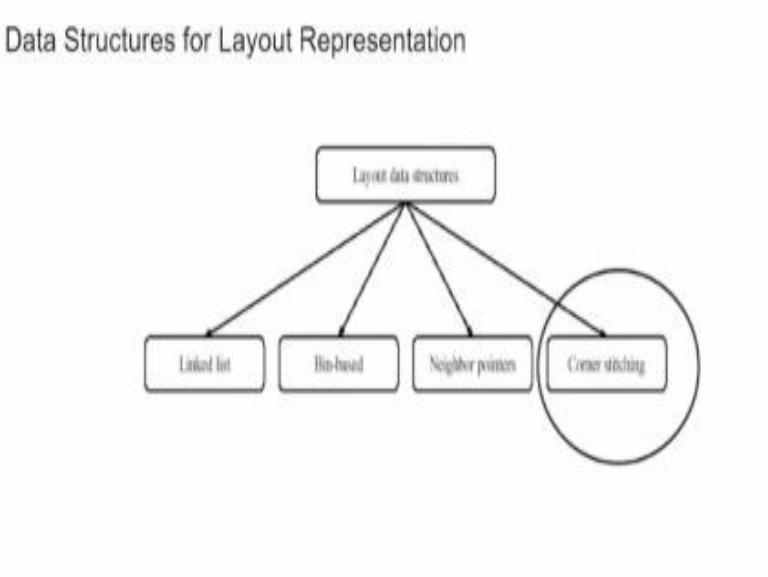

Now given this layout editor we also require data structures to represent the layout so that is done using the corners teaching data structure. There are other legacy data structures but the most important data structure that is used today is a corner stating the data structure and we hence we will discuss this data structure here.

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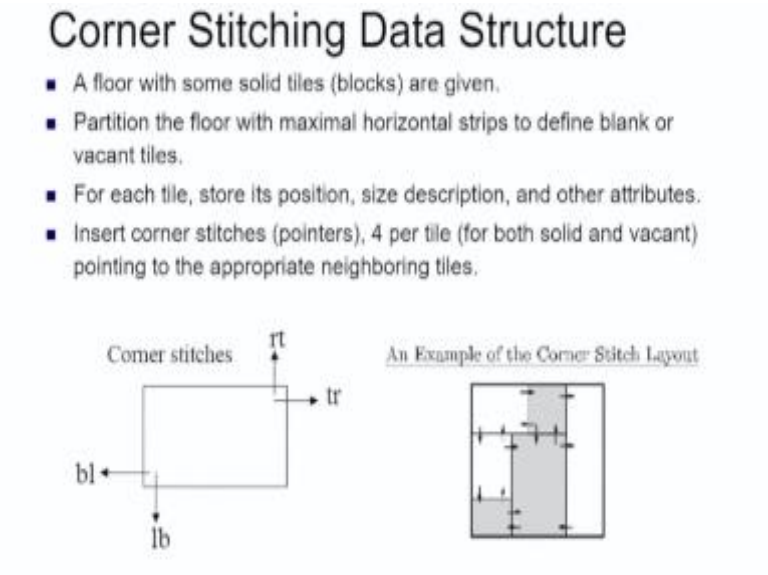

In the corner teaching data structure a floor with some solid tiles or blocks are given to me then we partition the floor with the maximal number of horizontal strips to define blank or vacant tiles. So at the beginning we are only given a vacant space with blocks on that and then we have to divide the vacant space into maximal horizontal strips for each tile we have to store its position size description and other attributes.

And then we insert corner stitches pointers for per tile for both solid and vacant tiles pointing to appropriate neighboring tiles if this one is a tile it has four pointers RT pointer, right top , top right, bottom left and left bottom these for pointers point to four tiles which are neighboring to it right and this is an example as to how the whole layout will be represented through the corners teaching data structure. We see that each time is stitched to the tiles neighboring to it right through the pointers that we have here.

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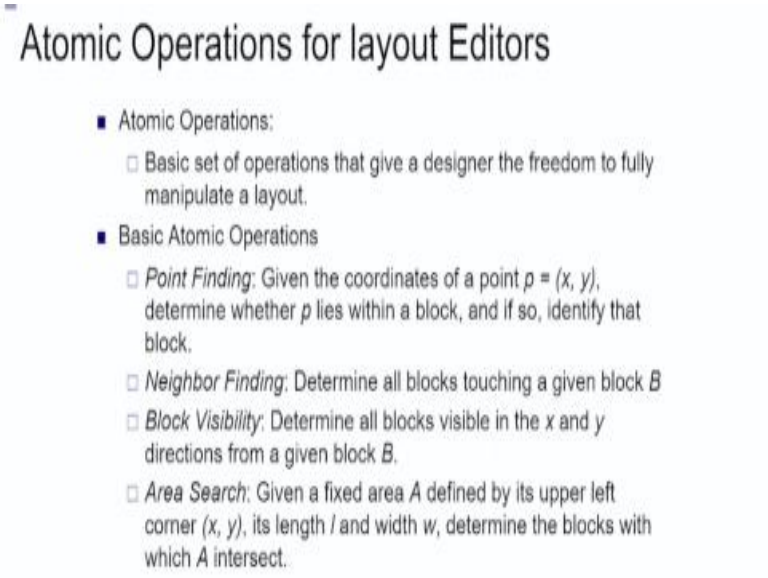

Now we offer we have defined the data structures we need to also have operations to operate on these data structures so what are the atomic operations that can be performed on layout editors the basic set of operations that give a designer the freedom to fully manipulate a layout are called the atomic operations. So we are now discussing operations that can be used on the layout editors the algorithms will use these operations to manipulate the layout so point finding given the coordinates of a point P XY determine whether P lies within a block and if so identify that block neighbor finding determine all blocks touching a given block B so that means if I have a block there can be many other blocks that is touching its boundaries.

So this function will allow us to find all the tiles that are neighboring to this block B. Block visibility determine all blocks visible in x and y directions from a given block B. Area search given a fixed area A defined by its upper left corner its length l and width w determine the blocks with which A intersect so we have a time which has a fixed location on the floor of the gym right it's upper left corner is defined by the coordinate X, Y. We also know the length of the chip and the width of the ship so now this operation will allow us to determine all blocks with which A intersect with which A overlap.

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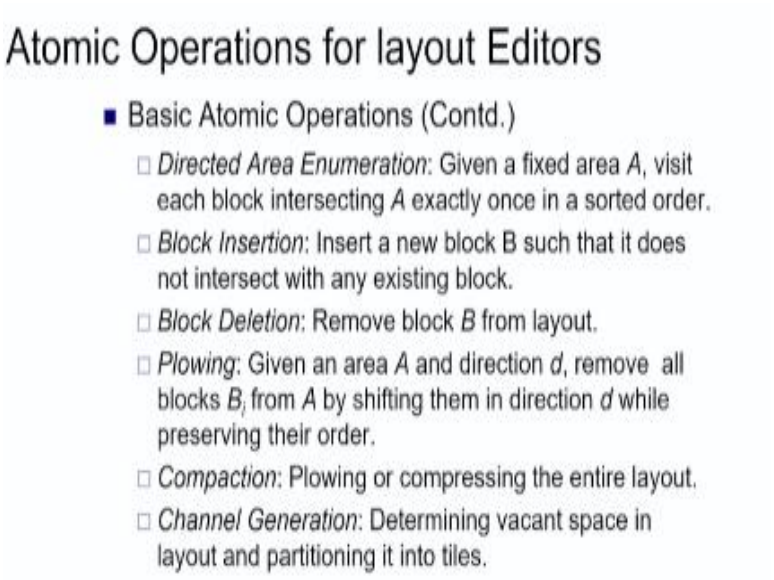

Directed area enumeration given a fixed area A visit each block intersecting A exactly once in a sorted order. So whoever is intersecting A we will visit that block intersecting A exactly once in a shorter order. Block insertion insert a new block such that it does not intersect with any existing. Block deletion remove a block B from the layout, Plowing given an area A and direction D remove all blocks bi from A by shifting them in deduction D while preserving their order.

So we are given an area A on the floor of the chip and we are also given a deduction D say right left extra so we have to remove all blocks from this area A in the direction D. Such that we have to keep the order of the block that were previously there we cannot change the order of the blocks on the layout. The order of the blocks on the layout should remain same but we have to remove all blocks bi by shifting them to in the direction D.

Compaction plowing or come to compressing the entire layout is called compaction. Channel generation determining vacant space in the layout and partitioning into tiles with this we come to the end of this module.

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