

# INDIAN INSTITUTE OF TECHNOLOGY GUWAHATHI

## NPTEL

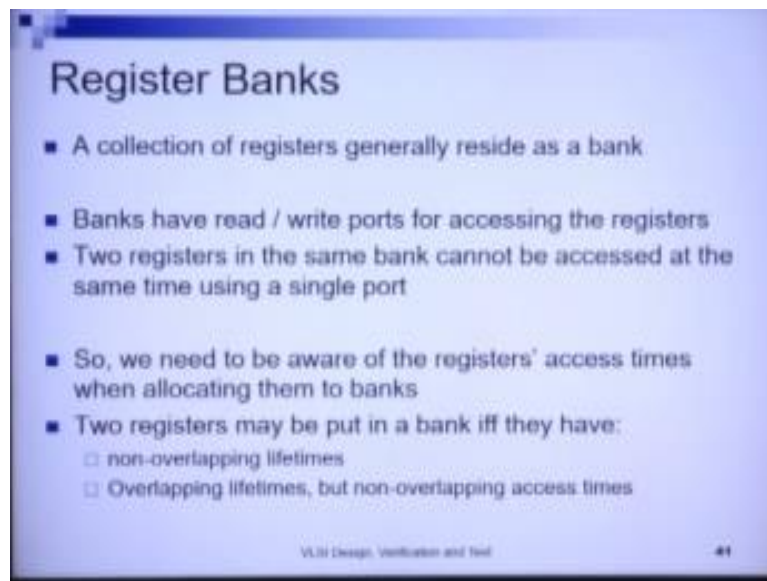
### NPTEL ONLINE CERTIFICATION COURSE An Initiative of MHRD

#### VLSI Design, Verification & Test

**Dr. Arnab Sarkar**  
**Dept. of CSE**  
**IIT Guwahati**

You welcome in this module we will look at a few extended resource sharing and binding problems first problem is related to register banks a collection of registers generally reside as a bank so till now we have looked at individual registers.

(Refer Slide Time: 00:44)



But typically registers in recital a large register file or a bank say in a in a risk machine and these register bands so the register inside these register bands can be accessed through read/write ports so a collection of registers generally reside inside of guy banks have read write ports for accessing the registers to registers in the same bank cannot be accessed at the same time using a single port so if you have two registers in the same register bank you

cannot access both the registers at the same time using a single port so you need to have multiple ports in the register bank for multiple accesses to registers in the register bank.

So therefore we need to be aware of the registers access times when allocating them two banks so two registers maybe put in a bank if and only if the these registers have non overlapping life types that means that all variables assigned to register r1 sake and register r2 sake have non overlapping life time so all temporary variables all temporary variables assigned to register one have are in the interval say this one and all registers in temporary with all temporary variables in register to add in another interval say this one and these two are non-overlapping.

So the registers themselves have non overlapping life times or the registers may have overlapping life times but non overlapping access times so I cannot access the registers together that can also happen so this is a more constraint scenario that I have overlapping life times but they have non-overlapping access tanks there none of the registers within the register backyard access together using the same port okay.

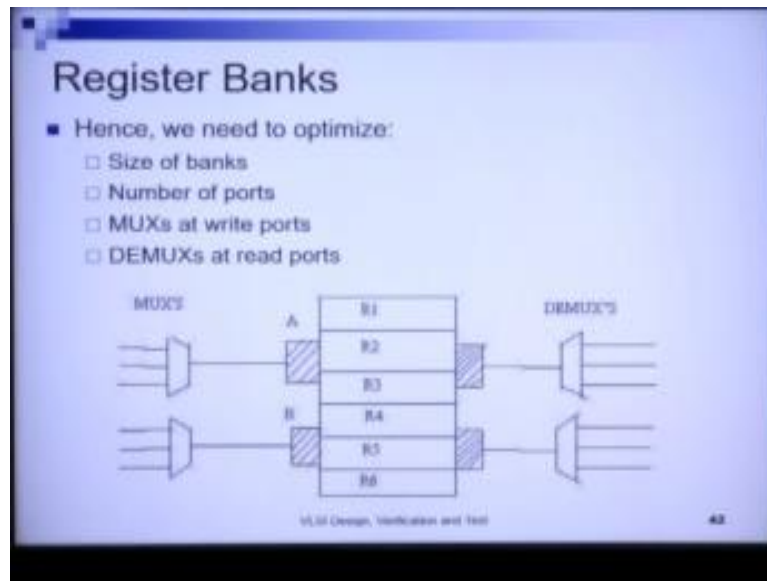
(Refer Slide Time: 02:56)

## Register Banks

- A collection of registers generally reside as a bank
- Banks have read / write ports for accessing the registers
- Two registers in the same bank cannot be accessed at the same time using a single port
- So, we need to be aware of the registers' access times when allocating them to banks
- Two registers may be put in a bank iff they have:
  - non-overlapping lifetimes
  - Overlapping lifetimes, but non-overlapping access times

VLSI Design, Verification and Test 41

(Refer Slide Time: 02:57)



Hence we need to optimize size of banks number of ports Max's at right ports and de Max's at read ports I have ports import a for reading and writing and cold be for another reading and writing so I have two ports a and B so I have Max's circuit points float circuit points float their outputs on the muxes and the max chooses one of the circuit points and places it on port on the right port of a and from a I can choose any one of these registers similarly this dmax the d-max will read from the reed port from the report and choose any one of the circuit points.

(Refer Slide Time: 03:44)

**Port Assignment**

- Assign ports such that MUX cost is reduced
  - An  $n \times 1$  MUX is needed to connect  $n$  points to 1 port
  - If there are 2 ports.
    - Best case - Each of  $n$  points connected to one port only
    - Worst case - Each point connected to both ports
  - Hence, minimize number of points connected to both ports
  - Best case is not always possible. Example,

The diagram shows a vertical stack of four register bits labeled 'a', 'b', 'c', and 'd' on the left, with a vertical label 'Register Bits' to its left. To the right of the bits are two ports, 'Port 1' and 'Port 2'. Port 1 is connected to bits 'a' and 'b'. Port 2 is connected to bits 'c' and 'd'. On the right side, under the heading 'Circuit Points', there are three points labeled 'X', 'Y', and 'Z'. Lines connect Port 1 to point X, Port 2 to point Y, and both Port 1 and Port 2 to point Z. To the right of the diagram, three time points are listed: T1:  $a \leftarrow x, b \leftarrow y$ ; T2:  $c \leftarrow x, d \leftarrow z$ ; T3:  $a \leftarrow y, c \leftarrow z$ . At the bottom of the slide, it says 'VLSI Design, Verification and Test' and the number '43'.

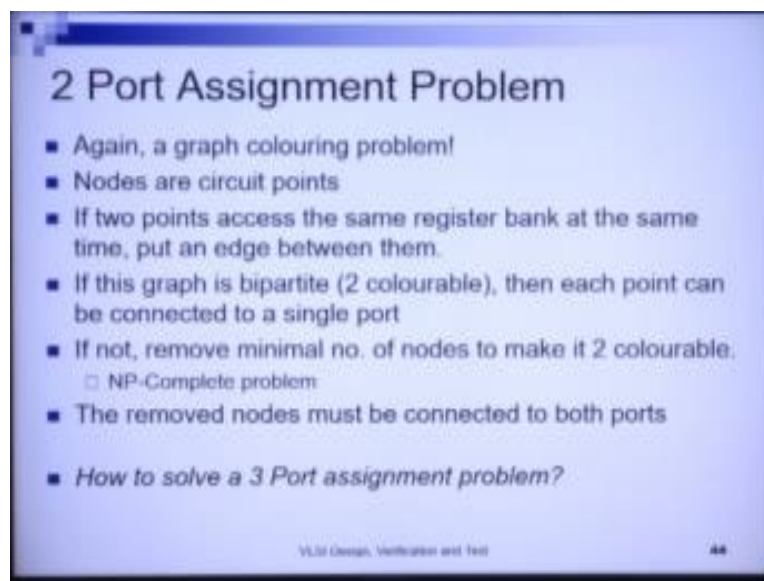
The port assignment problem is it as follows so we want to assign ports such that marks cost is reduced and  $n \times 1$  muxis needed to connect  $n$  points to one port if there are if there are two ports and we have  $n$  points and each of the seen  $d$  points is connected to one port only then we have the best possible solution but the worst case is that we need to connect each point to both the ports hence we want to minimize the number of points connected to both ports.

The best guess is not always possible why let us consider three time points and we have three register assignments register transfer assignments in time step one we have the assignment  $i$  equals to  $x$  and  $b$  equals  $2y$  in time step two we have the assignment  $c$  equals  $2x + d$  equals  $2y$  and in time step three we have the assignment  $i$  equals to  $y$  and  $c$  equals two said let us say we use port one for this assignment  $a \leftarrow 2x$ .

So I put the value in  $X$  to the register  $a$  through port one because I have used port 14 at the first time step for this register transfer I need another port so I use this register you I do this register transfer  $b \leftarrow 2y$  through port to now I come to step 2  $X$  was already connected to port 1 I can connect the same port I can connect through the same port and put the value of  $x$  in to see in time step two.

Now Z is another new circuit point let us say Ito sport24 Z and do the register transfer z2 deep through port to now in time step three we see that both y and z it has been previously allocated to port 2 and at least one of them has to be allocated to port 1 as well to effect to appropriately affect the register transfers at time step 3 because both y and z wants to access the two registers in the same register bank at the same time and they are connected to the same work where previously connected to the same port so at least one of these points have to be connected to both ports.

(Refer Slide Time: 06:14)



Now to solve this problem we again have another graph colouring problem we again have another graph colouring problem here the nodes are circuit points if two points access the same register bank at the same time we put an edge between them and that means they access two registers in the same register back at the same time they are we put an edge between them so when there is an edge between two circuit points we cannot use the same port for both these circuit points.

Therefore if the graph is bipartite that is too colourable if this graph is to colourable I can use two colours to colour this entire graph that means what do I have I have two distinct colours that means two distinct ports and I have been able to give a to give a colour to all vertices while not putting the same colour two adjacent vertices that means I have been able to II put

each circuit point connected to a single port only and this is the best possible solution that I have.

However if this best possible solution is not possible then our job is to remove the minimal number of nodes to make it to colourable we have if the if we have two ports however this removal of the minimal number of nodes is again complete problem the remove nodes must be connected to both ports then so what we do we first do a two colour and try to make the graph bipartite we try to make a tow colouring.

And then if this tow colouring is problem not possible then we try to remove the minimum number of circuit points such that two colouring is possible and for these circuit points the remaining circuit points which I had extracted out from the from the graph must be connected to both ports now this is for the two colouring problem what do we do for the three port assignment problem with this question posed to you I come to the end of this model.

**Centre For Educational Technology  
IIT Guwahati  
Production**

**Head CET  
Prof. Sunil Khijwania**

**CET Production Team  
Bikask Jyoti Nath  
CS Bhaskar Bora  
Dibyajyoti Lahkar  
Kallal Barua  
Kaushik Kr. Sarma  
Queen Barman  
Rekha Hazarika**

**CET Administrative Team  
Susanta Sarma  
Swapam Debnath**