Basic Electronics
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Module - 4
Operation Amplifier (Op-Amp)
Lecture - 8
Comparator

Today we will discuss about an important application of op-amp as a comparator. The comparator compares a signal voltage on one input of the op-amp with a reference voltage at the other input and the op-amp will act in an open loop. The main principle of the comparator is that it compares two voltages which are given at the two inputs of the op-amp. Let us take one example of a comparator.

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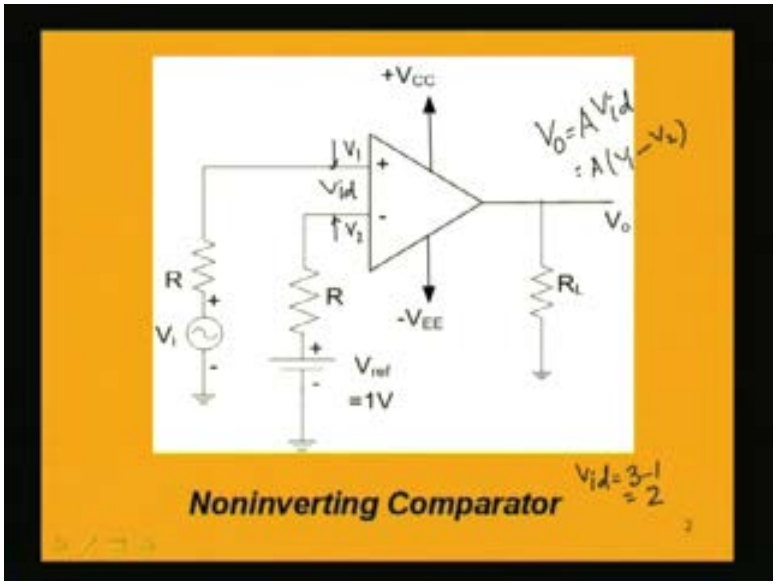

The op-amp is having two voltages, as we can see here. For example, we are taking the signal V_i, which is a sinusoidal signal and this is time varying that is taken at the positive terminal of the op amp and the constant reference voltage is 1 volt reference voltage which is taken in the negative terminal of the op-amp. The resistance R is there for compensating the offset current. We are having basically the comparing that is going on in this circuit. If we now see the two terminals, positive and negative, we know that the

op-amp output V_O will be given by the gain of the op-amp because it is working in an open loop fashion. We are interested in finding out gain V_O. It will be A, gain of the op-amp multiplied by the difference voltage V_{id}. That is the voltage available between these two terminals that is the difference between these two terminals, if I name it as V_1 and V_2 so V_{id} will be equal to V_1 minus V_2. So, AV_1 minus V_2 should be the output voltage.

These op-amp has plus V_{CC} and minus V_{CC} supply voltages that are to be connected to all the IC's of the op-amp and we have earlier also discussed about saturation. That is the output voltage cannot go beyond the supply voltage which is typically plus 15 minus 15 for 741 IC. So V_{CC} and V_{EE} will be plus 15 and minus 15 accordingly. Even though we may have a very high gain around 2 into 10 to the power of 5 or in that order, it will not be physically possible to get such a high voltage because the output will be saturated by this supply voltage. Maximum voltage that is obtained practically is around plus 14 volt and minus 14 volt. These are the saturation voltages, a little below the supply voltages practically we obtain. The output voltage in no way or under no condition can go beyond 14 volt and below minus 14 volt typically. That point has to be remembered while studying about comparator.

Now coming back to the output voltage V_O, which is given by A into V_1 minus V_2, if we consider the time during signal V_i, it will have a magnitude varying with time. Starting from zero if we do, it will go to positive peak and go down and it will go down to negative peak and repeat. At any instant if we consider an instantaneous voltage that has to be compared with the reference voltage because we are taking here a reference voltage of plus 1 volt. At any point, the output voltage will be determined by the difference input voltage V_1 minus V_2. At V_1 is this signal. When this V_1 is greater than this V_2 that means the supply voltage is higher than the reference voltage, 1 volt, the difference voltage will be now obtained as V_1 minus V reference. For example suppose we are considering an instant where the input voltage is 3 volt. Because it is a sinusoidally varying voltage, its voltage at any point we are considering it as having a value 3 volt then, what will be the reference voltage V_{id}? V_{id} will be 3 minus 1, that is 2. So output voltage V_O will be 2 into

gain. Although the gain is very high, we will get only around plus 14 volt, but it will have a saturated volatge if V_i is greater than reference voltage.

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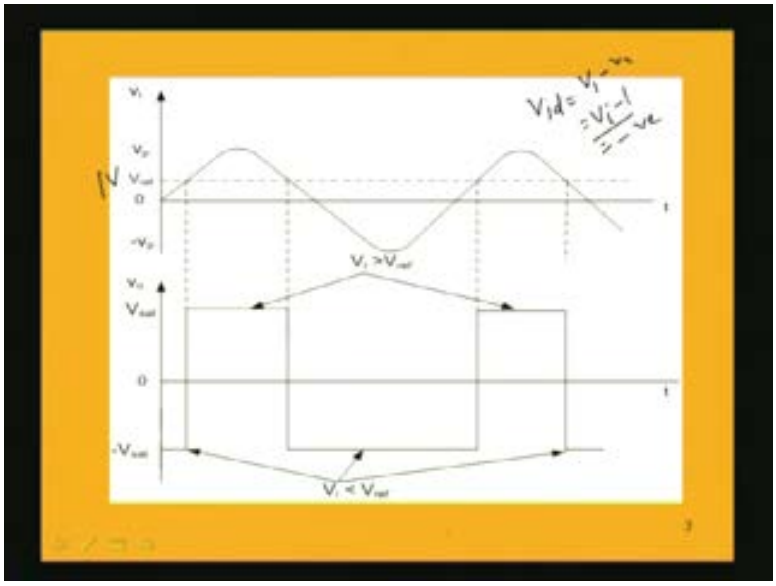

Let us consider a sinusodal voltage like this which is V_i and the reference voltage is 1 volatge. This dotted line is 1 volt reference voltage and suppose we are considering that the peak voltage of the sinusodal input V_i is greater than 1 volt. That has to be considered practically in order to get both the positive and negative saturation. For the portion when the input voltage V_i is less than reference that means this portion from zero to that point of 1 volt we will get the difference voltage V_{id} as V_1 minus V_2 and V_1 is the signal voltage V_i and reference voltage is 1 volt. For this portion it is less. So what will happen is that we are finally getting a negative volatge because V_i is less than 1. For example if it is 0.5, it will be minus 0.5; so, we are getting a negative difference voltage. So the output will be negative; A times this V_i. V will be V_O; so, V_O will be A times V_{id}. This will be negative and it will be limiting to the saturation voltage around minus 14 volt for 741 IC. We are denoting it by minus V_{sat} that is the saturation voltage in the negative. That means for this portion from zero to the point where it is less than 1 volt reference volatge, the output volatge V_O will be saturated at minus V_{sat}. This is the region.

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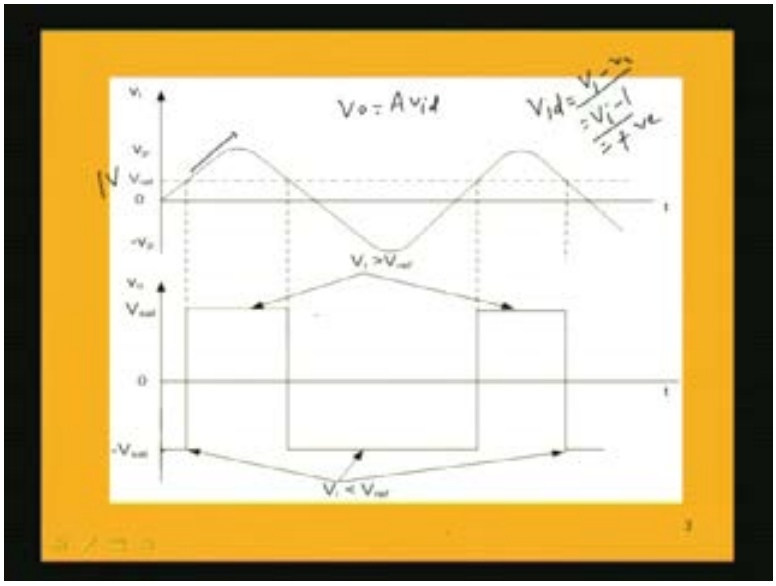

As soon as V_i becomes greater than the reference voltage, from this point onwards V_i is higher than reference voltage. So this value of V_{id} will be now a positive quantity. Because V_i is higher than 1, we are getting a positive value. As soon as the input voltage V_i becomes greater than the reference voltage, we will get an output which is positive. But that will be also saturated because it cannot go beyond the supply voltage. Around 14 voltage will be the typically obtained value at the V satutration, around 14 volt V saturation; but this is positive we will get at the output.

Till the point when V_i again becomes lesser than V reference, this will be saturated at that V_{sat} voltage and then again when it is less, when V_i becomes less than V reference then again will get a negative saturation. It will jump from the positive to the negative saturation voltage as soon as V_i becomes lesser than V reference. That is why it is jumping to this negative. Again, this will continue till the point when V_i is still less and as soon as it is greater than reference voltage, V reference then again V saturation will become positive. Like that we will get a digital pulse. Here we are getting a voltage between two discrete levels only, V saturation and minus V saturation. This is like a digital voltage we are getting which is only in two levels. Instead of input voltage which is analogue which is a continuously obtained voltage, at the output we are getting a

digital pulse. This comparator is giving at the output a pulse like this. One thing to be noted here is that we are getting an output voltage. Here it is a non-inverting comparator. We are connecting this signal at the positive end.

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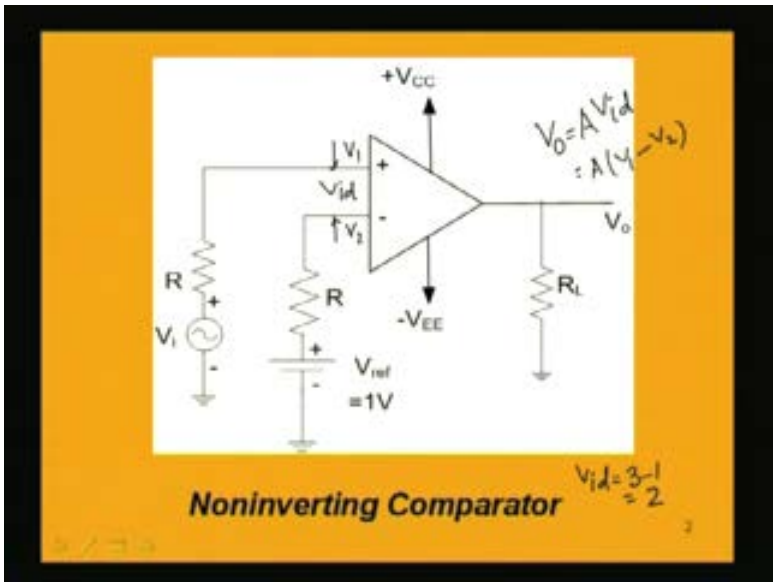

The width of the pulse basically is dertermined by the reference voltage because we can change the pulse width. That is the region for which it is positive and the region for which it is negative that can be controlled by choosing the level of the reference voltage.

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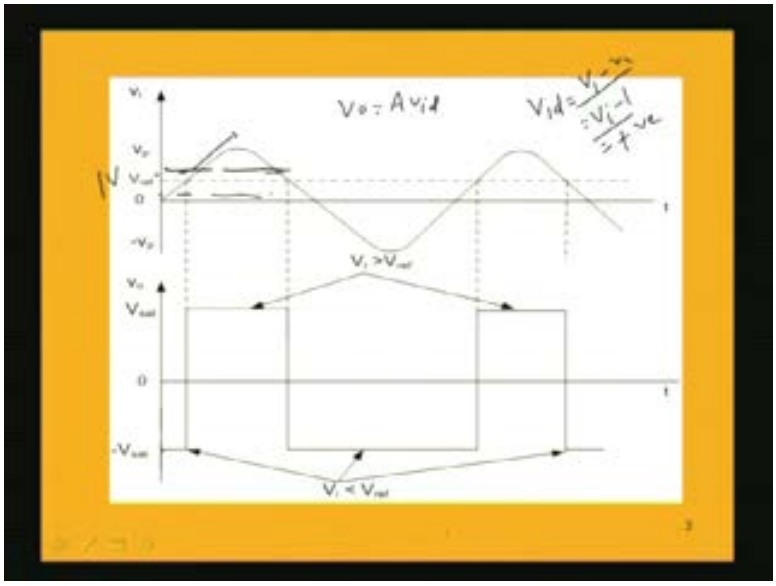

We can see that if the reference voltage is now increased or decreased if we have a voltage above this voltage, 1 volt or if we have a even lower voltage then the region for which it will be positive and the region for which it will be negative that will be changed. Now let us take such an example having a reference voltage negative.

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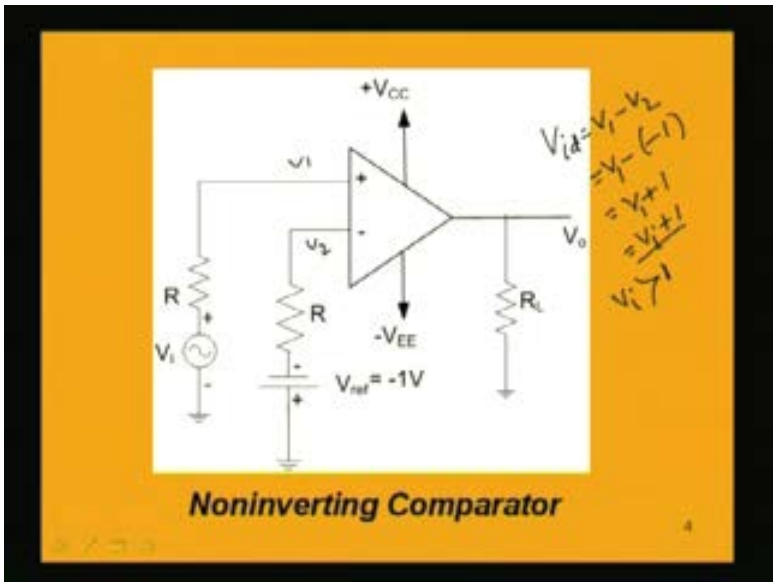

We are again taking this example but, we are taking a reference voltage minus 1 volt. If we have now minus 1 voltage as reference what will happen is that, again we will consider that sinusodally varying voltage V_i and we have V_{id} is equal to V_1 minus V_2. This is V_1 at the positive terminal, V_2 at the negative terminal. But here V_2 is a reference voltage which is negative, so that is 1 volt. Ultimately it will become V_1 minus minus 1 volt. That means it is becoming V_1 plus 1. What will happen when V_i is greater than 1 volt? Suppose V_i is greater than 1 volt, here this will be positive quantity. Then we will get the positive saturation voltage that can be seen here.

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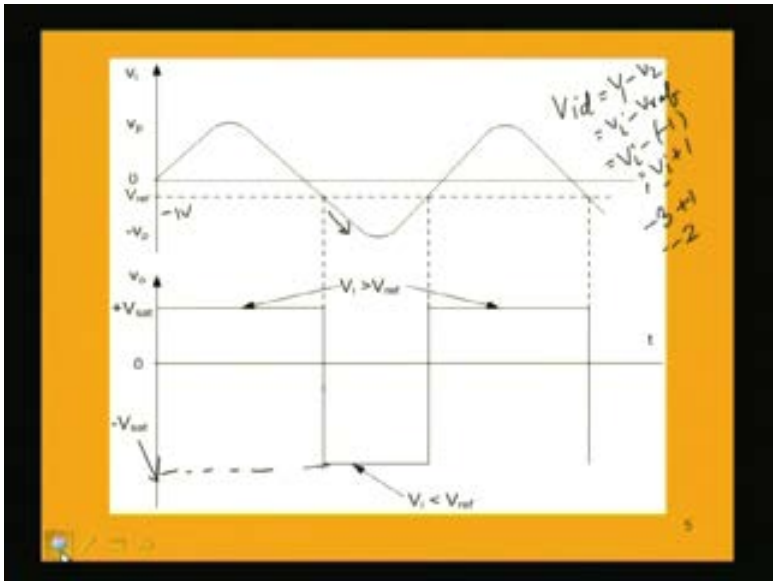

We are having this input voltage V_i given by this sinusodal voltage and reference voltage is negative minus 1 volt. This is reference voltage. For the portion starting from say zero, I have starting from here, for the whole signal up to this point V_i is higher than V reference minus 1. If this voltage is higher than this minus 1 volt, we will get a positive saturation voltage which will be around 14 volt for 741 IC. This saturation volatge V_{sat} is obtained from zero onwards till the point when it becomes lesser than minus 1 volt. From this point onwards it is negative direction and it is lesser than minus 1 volt. The momemt it becomes lesser than minus 1 volt, what will happen is that V_{id} is equal to V_1 minus V_2. That is equal to V_i minus V reference. But V reference is a negative voltage, minus 1

volt. So it is V_i plus 1. The input voltage is for example say minus 3 volt. It is lesser than minus 1 volt reference. What will we obtained that becomes minus 2 volt. The output will be negative and it will be saturated to the V saturation negative that is around minus 14 volts. The moment it becomes lesser than V reference, the output voltage jumps to minus V_{sat}. This is minus V_{sat}. This is the minus V_{sat} voltage around minus 14 volt for 741 typically. It will continue like that again when V_i becomes higher than V reference again it will jump to V saturation in the positive direction.

Here we are getting again a digital voltage. That is it is jumping between only two levels plus 14 and minus 14 volt. Here we have seen one difference from the earlier one. If we consider the width of the pulse that is the portion for which it is positive and the portion for which it is negative that is not same. This pulse width for the positive one and pulse width for the negative one is not same. It is not symmetrically positive and negative. That can be varied by varying this V reference voltage; that example we have seen.

Now if we consider a comparator that means although we are getting a pulse type of voltage or the digital voltage we are not getting the voltage having equal positive and negative portions. We want to get an ideal pulse having equal positive and negative portions; for equal time the pulse should be positive. That is V saturation should be there for equal amount of time with minus V saturation. V saturation and minus V saturation voltage which are there they should exsist for equal amount of time. If we consider a time period T, then for T by 2 it should be positive V saturation and for T by 2 it should be negative V saturation. That type of voltage if we want then we have to consider a circuit where we will get this type of voltages and that will be posible if the reference voltage is made zero.

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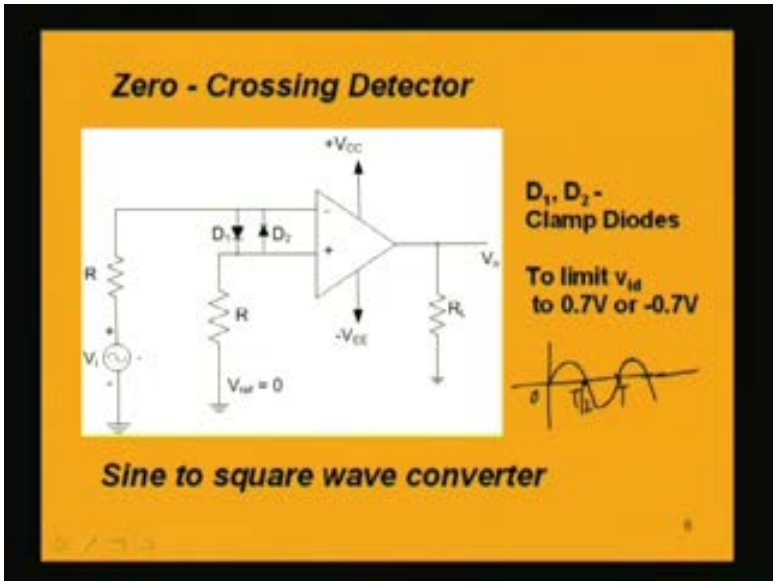

Let us take one example of that type of zero-crossing detector. This circuit which we are going to discuss, will be able to detect when the input voltage crosses zero and in what direction? Input voltage is a sinusodal wave form you are taking. V_i is sinusodal and V_i is a voltage which is crossing zero after a certain amount of time say T by 2. This is T by 2, this is T, this is the time period. The moment T by 2 if you consider it will cross zero. This is the zero line. It will cross zero from positive direction to negative; from positive to negative it is crossing zero and at this T it is crossing from negative to positive. So a circuit is able to detect the moment when it crosses zero and in what direction of the input voltage? That means we are trying to detect at what moment the input voltage which is the sinusodal voltage is crossing the zero line and in what direction? That is is it crossing from positive to negative or from negative to positive direction that can be detected by a circuit which is shown.

Here the reference voltage is zero voltage. Positive terminal if you see it is having a resistance R and it is connected to ground. That is zero voltage is the reference voltage at positive terminal and the negative terminal of the op-amp is connected to the input sinusodal voltage. But there is a resistance R also which is connected in the positive as

well as the negative terminal the reason being that there is need for compensation of the input offset current. That is why this resistance is connected as well here.

One important point to be noted is that there are two diodes which are connected in the input of the op-amp, D_1 and D_2 and their connection is also in the opposite way. Here D_1 has p and n in this fashion and D_2 has p and n connected in the opposite way. The reason for connection on this diodes is to limit the input difference voltage given as a input to the op-amp. Because if V_i is very large that may damage the op-amp. In order to limit the input voltage we are connecting these two diodes. What these diodes will do is that when the diode conducts it will have a drop of 0.7 volt typically. The input difference voltage to the op-amp will be limited to 0.7 or minus 0.7 irrespective of which diode conducts. If this diode conducts or this diode conducts correspondingly we will get a voltage drop either 0.7 or minus 0.7 and this resistanc is there to limit the diode current.

We are having the circuit and our aim is to detect zero crossing. D_1 and D_2 are additional components which are known as clamp diodes because it clamps the input voltage given to the input of the op-amp. That is the difference voltage which is clamped to 0.7 volt and minus 0.7 volt respectively. If we are considering a sinusoidal input voltage V_i, then what will happen? We have an instantaneously varying sinusoidal voltage at any point if we consider and compare it with the reference voltage zero. If this is the voltage, we are now comparing it with zero voltage as zero is the reference. We will have only two portions to consider. That is direction, whether V_i is positive or V_i is negative.

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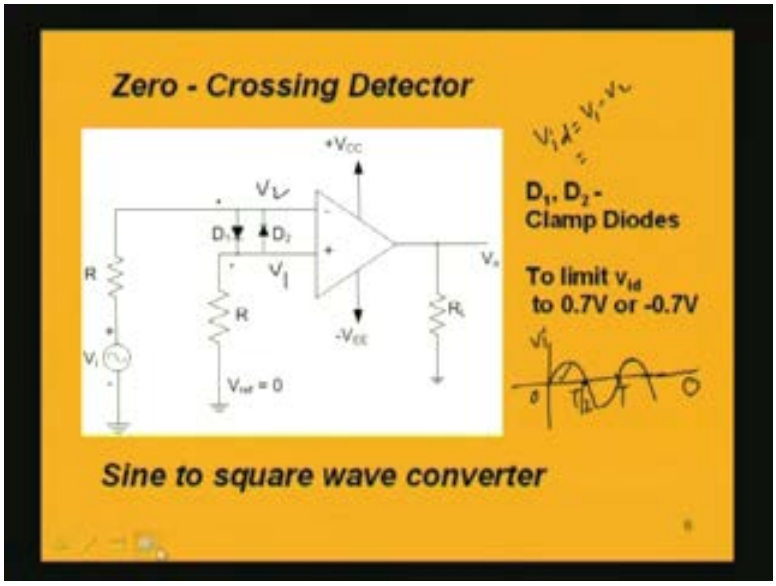

In this positive half cycle V_i is greater than zero. Here we see where it is connected. If in the positive half cycle, the voltages are such that this is V_1, this is V_2, difference voltage is V_1 minus V_2. But then we will have to now take care of the connection of the clamp diodes because when V_i is positive as it is greater than zero, this diode D_1 will now conduct. So diode D_1 conducts and the drop across this diode D_1 will be 0.7.

Now the output voltage will be what? Output voltage is V_1 minus V_2 into A because now, V_{id} is V_1 minus V_2. V_{id} is minus 0.7 because this drop is 0.7 across this diode. This is 0.7; here positive, negative 0.7. But as the difference voltage is V_1 minus V_2, so it will be minus 0.7. So minus 0.7 into the gain A but that will be limiting to the saturation voltage around 14 volt but negative saturation. So we will get a negative voltage when V_i is higher than V reference means in the positive half cycle.

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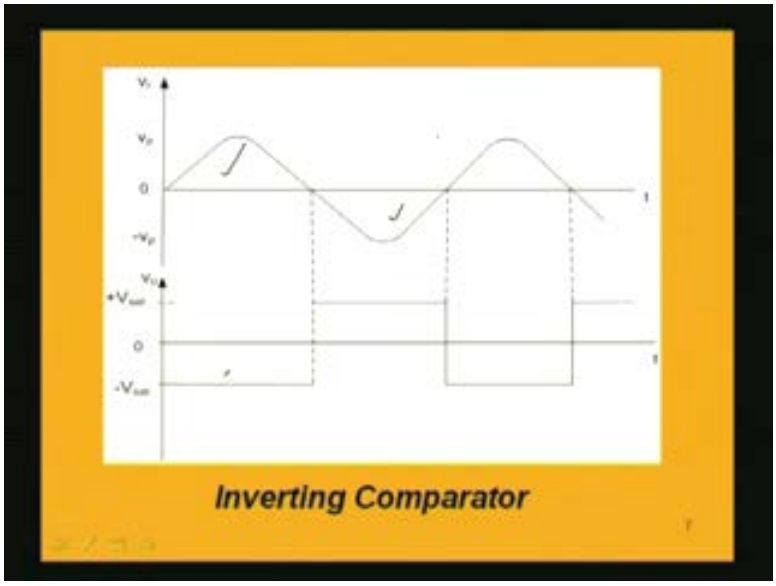

In the positive half cycle of the input voltage we are getting negative V_{sat}; that means it is inverting. It is an inverting comparator actually and when the input voltage V_i is in the negative half cycle, in this portion then what will happen is that as this is now negative, this is zero. This diode D_2 will be now conducting because it is forward biased now.

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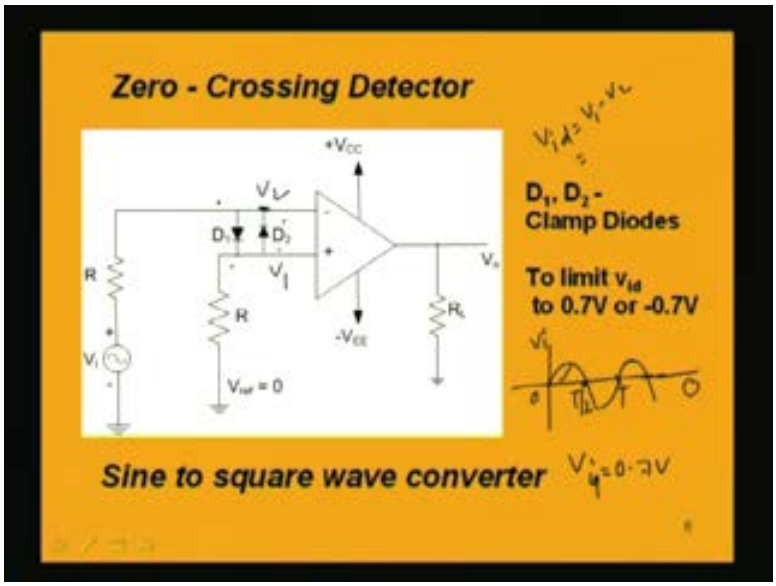

Because now it is negative; this will be negative now. The D_2 will be conducting and D_2 conducts means 0.7 volt. This polarity will be positive here and negative here that means we will get 0.7 volt which is positive and V_{id} is 0.7 volt positive. For this portion V_{id} is 0.7 volt. So, output voltage will be positive but it will be saturated. We will get output voltage V_O and positive V_{sat} that is around 14 volt.

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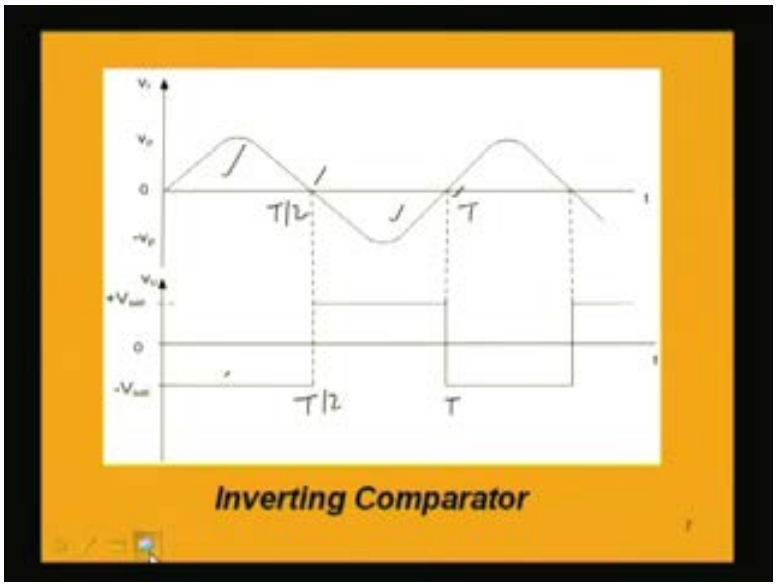

For this portion when this input voltage is negative we will get V saturation in positive direction. Here, this is the constant V saturation voltage. Again it will change to V saturation negative when it crosses over to the positive half cycle again. One point to be noticed here is that the circuit here is able to detect the moment when the input voltage crosses zero because at this point the input voltage crosses zero and at that point the output voltage jumps from one saturation level to the other; that is from negative to positive or positive to negative. Here it is crossing zero; again it is changing from positive to negative and the direction of the crossing either it is from positive to negative or from negative to positive that can be also detected from the output voltage. Because at this point when the V saturation is jumping from negative to positive correspondingly V_i is changing from positive to negative. That means it is crossing zero from positive to negative direction.

The moment when it crosses zero from positive to negative direction, the output voltage V saturation jumps from negative to positive and similarly when it crosses from negative to positive, V input crosses from negative to positive, then at that point the V saturation jumps from positive to negative. We can now detect the moment when it crosses zero as well as the direction of crossing zero. Either positive to negative or negative to positive that can be detected in the circuit by observing the output voltage change. The time period for which V saturation exists is same as the time period for which V saturation negative exists. T by 2 if we consider, this is T by 2. This is T. This time period is also same. So, we get here a perfectly square wave at the output. That is a digital voltage at the output with equal magnitude of time or equal amount of time for which positive voltage exists and negative voltage exists. This is a proper square wave we are getting.

If we now see the circuit although it is giving a perfect square wave there may be one situation where it is misidentifying zero crossing for a noise. As noise voltage is present, when the noise voltage also crosses zero that can be also detected as a zero crosser for this circuit. That is one disadvantage basically and another disadvantage if the frequency of the input voltage is very high that is if it is very fast, the input voltage is changing very fast, then the output voltage may not be able to track that because it will take some time. The speed of the op-amp is one important criterion; the output voltage also should change very fast in order to keep a track of this change of the input voltage but that has some limitation.

The speed of an op-amp has to be considered because it may not be very fast. It may not be so fast as to track this input voltage frequency. Because of these two difficulties that is faced by this circuit of zero cross detector we have to think about some other circuit which can tackle these two difficulties of detecting noise as the zero crossing voltage and to take care of the fast changing input voltage.

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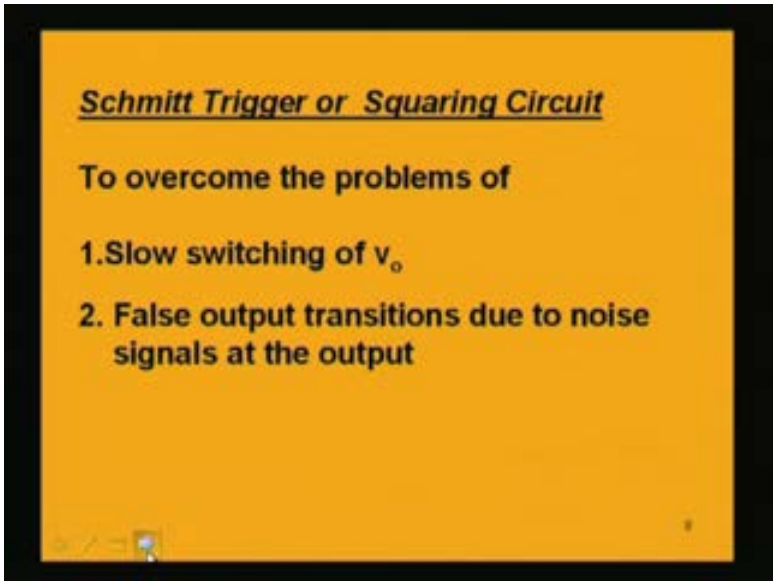

We have another circuit which is known Schmitt trigger. This is also a squaring circuit but it overcomes the problem of slow switching of the output voltage and false output transitions due to noise signals at the output.

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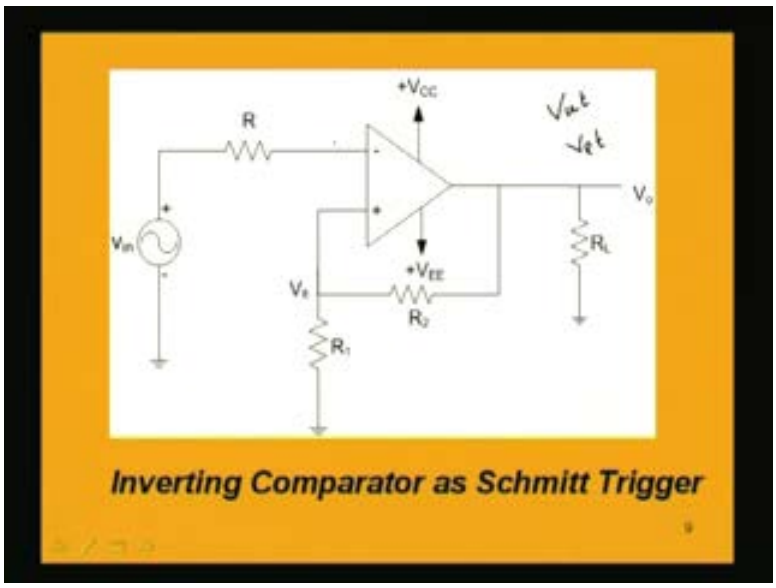

The circuit which is the circuit of a Schmitt trigger is shown here. It is also an inverting comparator but here instead of the reference voltage which we were taking as zero, here

the output voltage is fed back via this feedback network R_1 and R_2 to the positive terminal of the op-amp. So, it is a positive feedback again and we have this input voltage V_{in} which is a sinusoidal voltage and how it works that has to be understood by considering the reference voltage. Here there are two reference voltages known as V upper threshold and lower threshold, V_{ut} and V_{lt}. There are two threshold voltages or reference voltages V_{ut} and V_{lt}.

If we consider this polarity of V_{in} positive here and negative here in the positive half cycle then the voltage which will have to be compared with the reference voltage is V_{lt} or the lower threshold; in the negative saturation it will be the lower threshold and in the positive saturation voltage V_O, it will be upper threshold. If we consider this voltage V_{lt}, that is nothing but the voltage at the output into R_1 by R_1 plus R_2. We know that this is voltage division but then what will be the polarity? If we consider this V_{in} when it is positive it will be comparing with the voltage which is available here and this voltage is coming from the output voltage via this feedback network. The voltage here is output voltage which will be either V saturation or negative V saturation. When it is positive that is this point is positive then it will be here negative saturation. Because it is an inverting comparator, it will be comparing with this voltage and the moment this voltage V_{in} is higher than this threshold voltage V_{lt}, then switching will occur.

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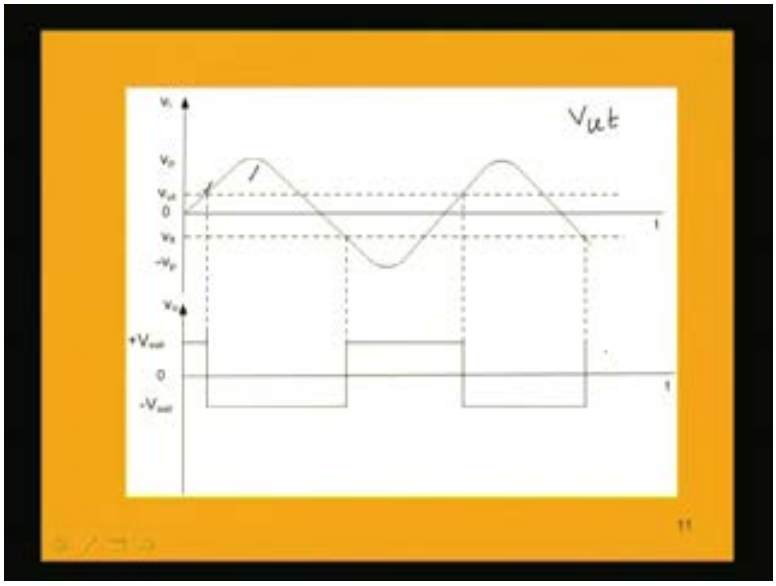

For example let us take what will be the output voltage for a sinusoidal wave form like this?

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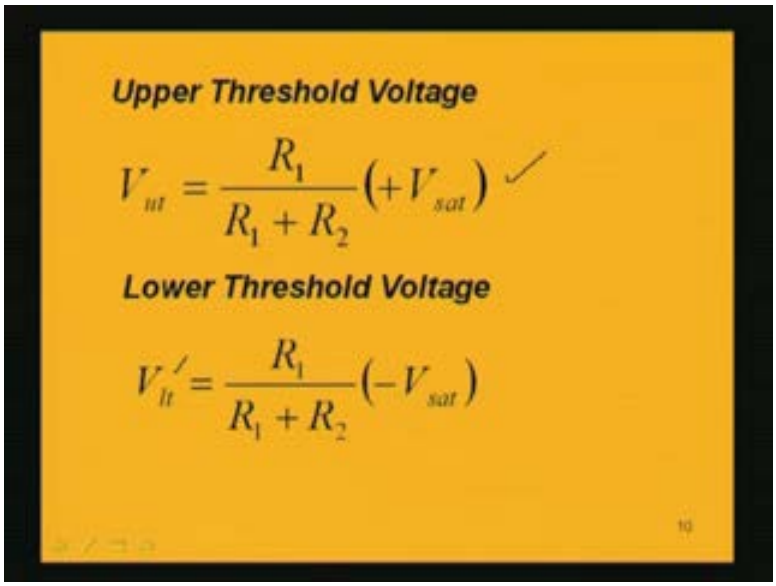

Let us take this V_{lt} and V_{ut} and calculate them. V_{ut} is upper threshold voltage when we have the output voltage V saturation. Then output voltage V saturation will be given a voltage V_{ut} which is equal to V_{sat} positive into R_1 by R_1 plus R_2. In the lower threshold

that is minus V_{sat} that will be minus V_{sat} into R_1 by R_1 plus R_2. That is V_{lt}. The moment when this voltage V_{in} is higher than V_{ut} that is we see here, this is V_{ut}, this is V_{lt} and the voltage magnitude will be equal because V saturation and minus V saturation these are equal and then we are considering R_1 and R_2 same resistive network. If V_i is less than V_{ut}, from this point to this point (Refer Slide Time: 31:20), then what voltage will we get?

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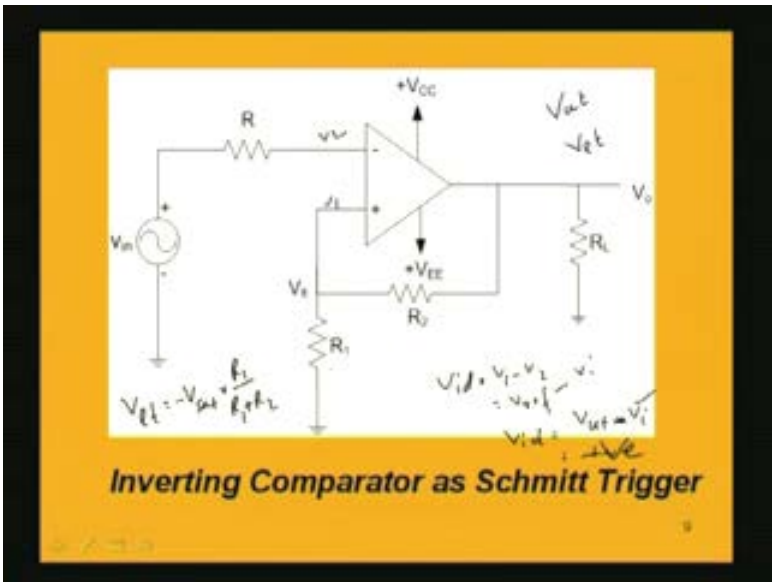

Because here if we consider this is say V_1, this is V_2; V_1 minus V_2 is the V_{id} that is the difference voltage and V_1 is this reference which is V_{lt} or V_{it} minus V_i. When V_i is less than V_{ut} that is happening here. That is V_{ut} is here and for this portion V_i is less than V reference which is V_{ut}. So V_{ut} minus V_i that is the difference voltage. This is higher positive, so we get positive saturation voltage at the output. The moment when V_i is higher than V_{ut}, then this difference if we consider this is higher. So, it will be negative. Now it will be negative and it will be limited to saturation voltage so it will be saturated to V sat minus. As soon as it becomes V sat minus then again what will be the reference voltage here? It will be V_{lt}. V_{lt} is lower threshold voltage. V_{lt} is equal to minus V_{sat} into R_1 by R_1 plus R_2. This is around minus 14. That means a negative voltage, V_{lt}. This is shown by this negative voltage.

As soon as this output voltage jumps to negative V saturation we have a reference voltage given by the lower threshold voltage V_{lt}. During this portion when this output voltage is V saturation negative we have to compare with this reference voltage V_{lt} and from this point to this point (Refer slide Time: 33:53), V_i is higher than V_{lt}. That means we will get a negative saturation voltage V_{sat} minus throughout this portion and as soon as V_i is lesser than V_{lt}, then again it will jump to positive V saturation and at the same time we will have a reference voltage given by V_{ut}. From this point to this point when positive V saturation is the output voltage then, we will have to compare with the V_{ut}. The difference voltage is dependent upon the difference between V_{ut} and V_i.

V_{ut} is higher so it will continue to be positive and this will be repeated or continued. Basically here we have seen one interesting aspect that the output voltage is a square wave, perfectly square wave. The output voltage versus input voltage if we consider we find a hysteresis and that is shown here.

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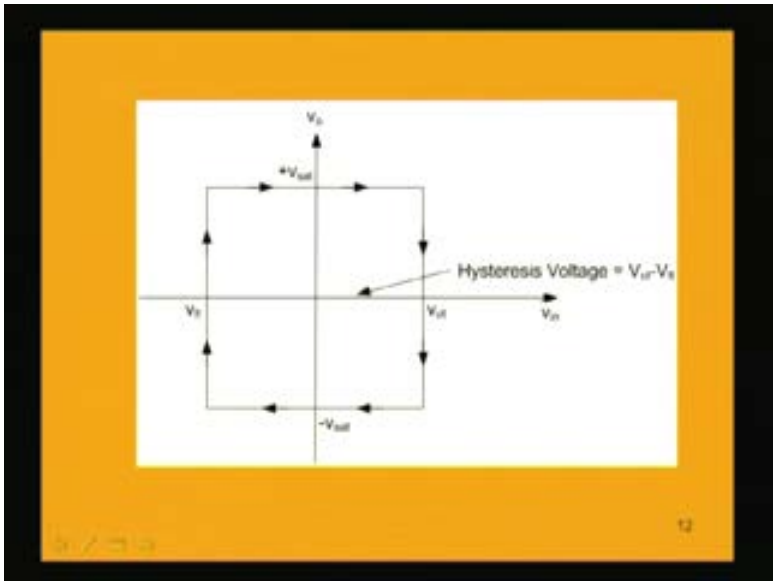

That is if we plot V_O versus V_i, then we see a hysteresis kind of a thing. That is if we consider say V_{in} or the input voltage now, this is the axis of the V_{in}, this is the axis of V_O. When we have V_{in} less than V_{ut}, this is the positive V_{in} in the positive half cycle. This is

the upper threshold voltage because in the positive half cycle the output voltage will be V saturation and that is shown here. Till when V_{in} is less than V_{ut} then we will get a V saturation and then if we have V_{in} greater than V_{ut}, we will get the output voltage jumping from V saturation to minus V saturation and here it will continue to be at minus V saturation for all these portion till when you have V_{in} less than V_{lt}. When V_{in} is less than lower threshold voltage in this portion then immediately the output voltage jumps from minus V sat to plus V sat. A complete hysteresis is obtained and this hysteresis voltage is known as the difference between the upper threshold voltage and lower threshold voltage that is V_{ut} minus V_{lt} is the threshold voltage. This is a very interesting aspect of hysteresis being observed in this Schmitt trigger. In this Schmitt trigger, we have seen that we can get a hysteresis voltage and that voltage is the difference between upper threshold and the lower threshold.

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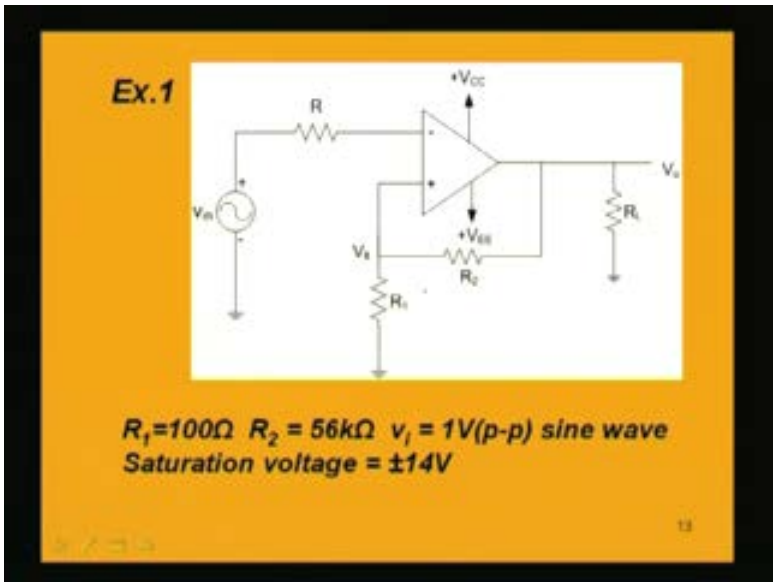

For example, suppose we consider a circuit where we are using the resistance R_1 and R_2 as 100 ohm and 56 kilo ohm. Input voltage is a sinusoidal voltage whose peak to peak value is 1 volt and at some frequency which is not very much important because we are going to find out the shape of the output voltage and here the saturation voltage is plus minus 14 volt. This is the Schmitt trigger configuration where we are given the resistance

values as well as the input voltage. If we find out what will be the lower threshold voltage and upper threshold voltage for the Schmitt trigger, we can calculate the lower threshold and upper threshold.

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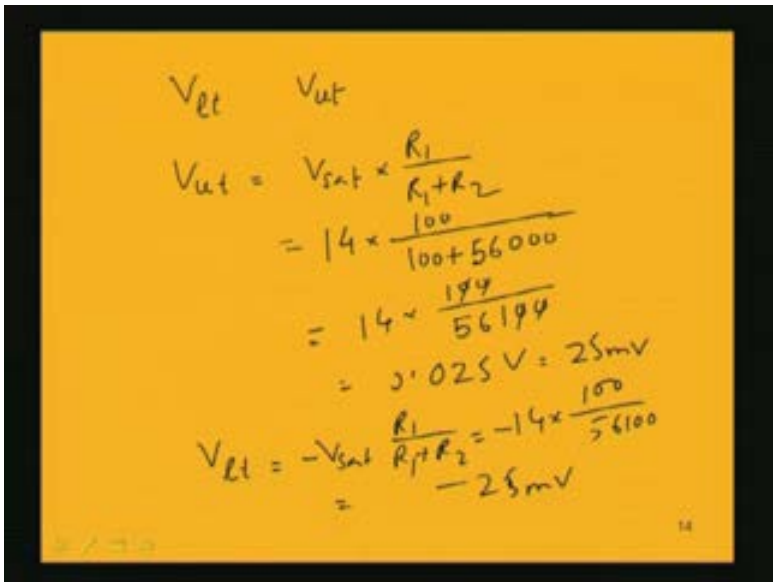

What will be the upper threshold voltage for this example? That is V saturation into R_1 by R_1 plus R_2 and V saturation is given as 14 volt. Positive 14 volt will be the V saturation positive, R_1 is 100 and R_2 is 56 k. So, 14 volt into R_1 is 100 by 100 plus 56 k, so, 56,000 ohms. That is equal to 100 by 56,100 and if we calculate this value 14 by 561, it will be almost equal to 0.025 volt. That means 25 millivolt is the upper threshold voltage and lower threshold voltage will be just opposite in polarity but magnitude is same; that can be verified. What is lower threshold voltage? That is minus V_{sat} into R_1 by R_1 plus R_2 and as V_{sat} is same 14 volt for both the positive and negative, it is minus 14 volt into R_1 is 100 by same value; so, 56100. We get minus 25 millivolt. That is the V upper threshold and V lower threshold voltage.

What will be the hysteresis voltage that can be also found out.

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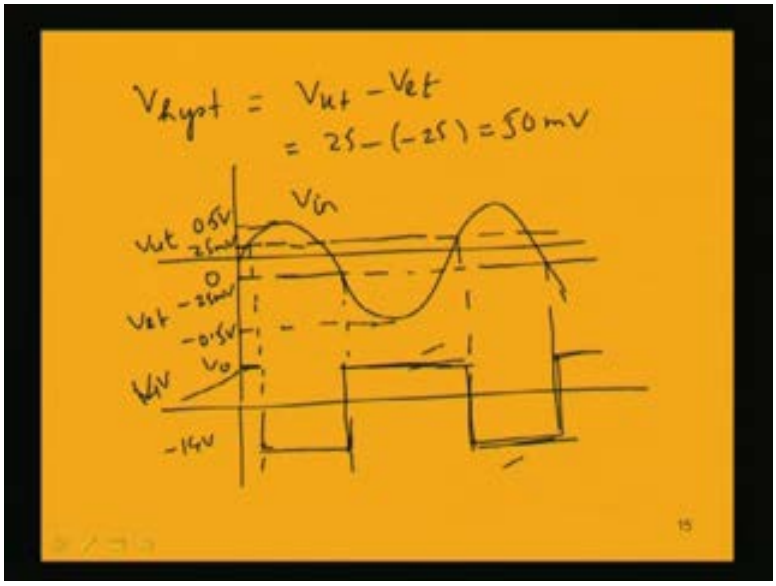

The hysteresis voltage equal to V upper threshold minus V lower threshold and that is equal to 25 minus minus 25. So, 50 millivolt is the hysteresis voltage and if we plot the input and output voltages, V_{in} is this one. It is varying between the peak to peak voltage of 1 volt. This V peak will be 0.5 volt and this will be minus 0.5 volt for the input voltage and the upper threshold and the lower threshold voltages are 25 and minus 25. So 25 is for example somewhere here; plus 25 millivolt, it is not to scale. I am just showing to illustrate this example. Suppose minus 25 is here; this is V_{ut}, this is V_{lt}. The output voltage if we plot V_O, it will be comparing with this upper threshold and lower threshold. This is lower threshold and this is the upper threshold; this is the lower threshold. This is V_{sat} which is obtained as or given as 14 volt and this is say, minus 14 volt. So in between these two it will be varying. It will be like this. This type of wave form we will get. This half and this half are equal; this drawing is improper. These two halves are equal. We get a square wave between plus 14 and minus 14 volt with this example of threshold voltage and the resistance values.

In this comparator circuit which we have discussed till now basically we have got output voltage digital no doubt but the magnitude of the output voltages are not sufficient for driving a TTL logic circuit. Because in TTL logic circuit, transistor- transistor logic

circuit which are used for digital IC's we require plus 5 volt or zero volt as 1 or 0 we have to use these voltage levels. Basically we need a circuit to limit the output voltage to around 5 volt. For getting that type of voltage limiter, we have to now think about a circuit which will give the output voltage limited to a particular determined value.

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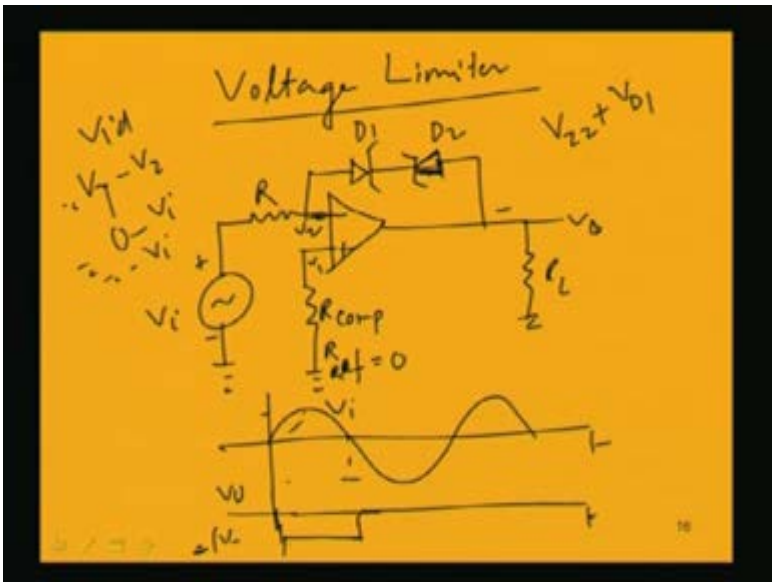

Let us take one example of a voltage limiter circuit and see how the output voltage will be limited to some predetermined value, not to saturation voltage because saturation voltage whatever we got 14 volt or negative saturation minus 14 volt is too high. Such a circuit can be devised or obtained by using Zener diode and ordinary diode. Let us take this similar example of the comparator circuit again but here we will connect a Zener as well as a normal diode. This R is a compensating resistance or compensating the offset current basically but the reference voltage is zero; we have taken the zero crossing detector reference is zero. But we are having a Zener diode and in this case we are taking two Zener diodes. This is the load resistance where we are connecting the output voltage.

In this circuit as two Zener diodes are there, their Zener voltages must be lesser than what we get at the output saturation. That is 14 volt. It should be less than 14 volt. What will happen when we have the input voltage sinusoidal. This is V peak, this is minus V peak.

Let us consider the positive half cycle. In this positive half cycle, this half cycle, this is the reference; reference is zero. The comparison will give output V saturation at V_O and that will be negative V saturation because V_1 minus V_2 is V_{id} and that is equal to zero minus V_i, so that is a minus V_i. We are getting here a negative output voltage which is magnified. That is the op-amp gain we will be getting at the output. If we consider V_O for this portion, we will get a negative. But then what will be this voltage? This will not be saturation voltage because as this Zener diode is connected, what will happen is that when it is negative this diode is D_1, this diode is say D_2; so the reverse breakdown will take place in the case of the diode D_2. Because it is negative, p is negative, this is connected in the reverse direction and as far as the diode D_1 is concerned, it will have the ordinary drop of around 0.7 volt that is typical for silicon.

We will get the total voltage drop V_O as V_{z2} plus drop D_1, V_{D1} that is the diode drop of D_1 plus the Zener voltage, which is the Zener voltage drop of the diode D_2 because D_2 will be having reverse breakdown. That is Zener breakdown will happen, it will be conducting. But here it will be normal conduction because it is forward biased when it is negative and that is happening in the region when this V_i is positive. We are getting this voltage as minus; this is minus. This voltage if we consider, this drop plus this drop with a minus sign, we will get minus V_z.

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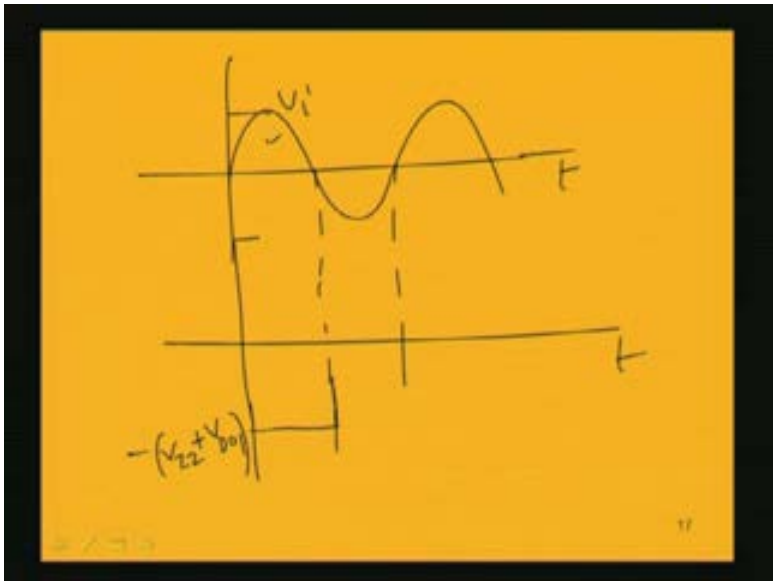

Here for this positive half, we will get for this portion a minus V_{z2} plus V_{DO1}. V_{DO1} is the normal diode drop in the diode D_1 and V_{z2} is the Zener voltage drop in the diode D_2 because that is conducting as a Zener diode. This is for the negative half cycle. This negative voltage you are getting for the positive half cycle.

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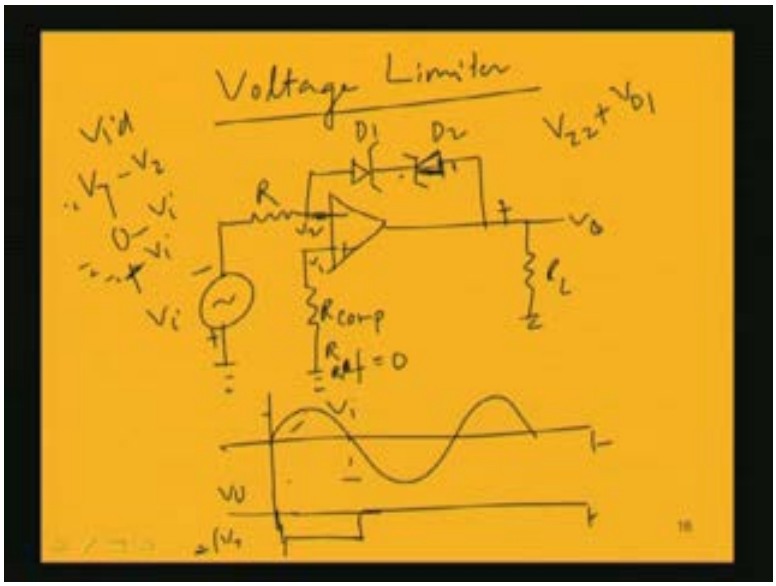

Then what will happen in the negative half cycle? In the negative half cycle this V_1 minus V_2 is zero minus V_i; as V_i is negative, we get a positive voltage. We are getting at this point positive; when this is negative this is positive so we are getting a positive. Now D_1 will conduct as a Zener diode; Zener break down will take place. We are assuming that this Zener voltage is less then this V_O saturation V_{sat} 14 volt. Now breakdown will be here in the D_1 and D_2 will act as a normal diode, ordinary diode which will have the normal diode drop of V_{DO2}. This voltage we will get. That is in this direction we will get plus here, this is minus.

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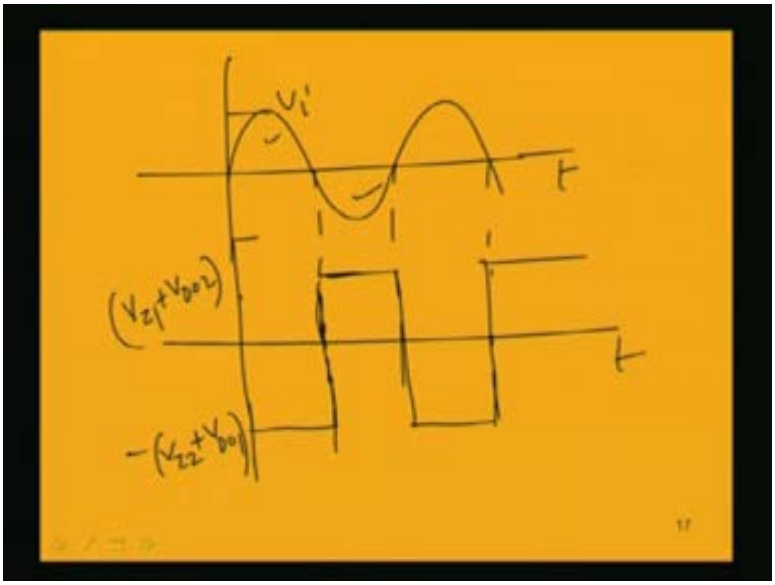

We will get a positive voltage V_{z1} plus V_{DO2} for the negative half cycle. It will be like this. We are getting that means a limited voltage not V saturation but it depending on V_{z2} or V_{z1} and V_{DO} for the two diodes and if we take a Zener diode having say 5.1 volt Zener and 0.7 volt as the diode drop we can get as 5.1 plus 0.75 or around 0.8 volt, not 14 volt V saturation that we were getting.

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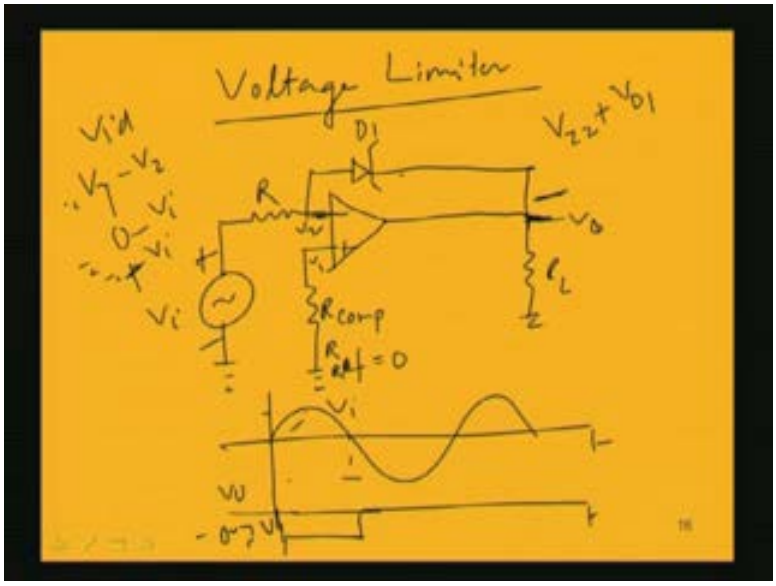

We consider similar circuit with only one Zener diode instead of this. Suppose we now have only one Zener diode; this has been removed. In this case we want to find out the output voltage. When it is in the positive half cycle what we will get? In the positive half cycle means when this is positive, we are getting a negative voltage, saturation voltage V_O and this will now act as a normal diode. When it is in the positive half cycle, the output voltage is negative V_{sat} and this will be acting; D_1 will act as a normal diode so, we will get a normal diode voltage drop which is 0.7, but negative. Here we will get a 0.7 volt negative.

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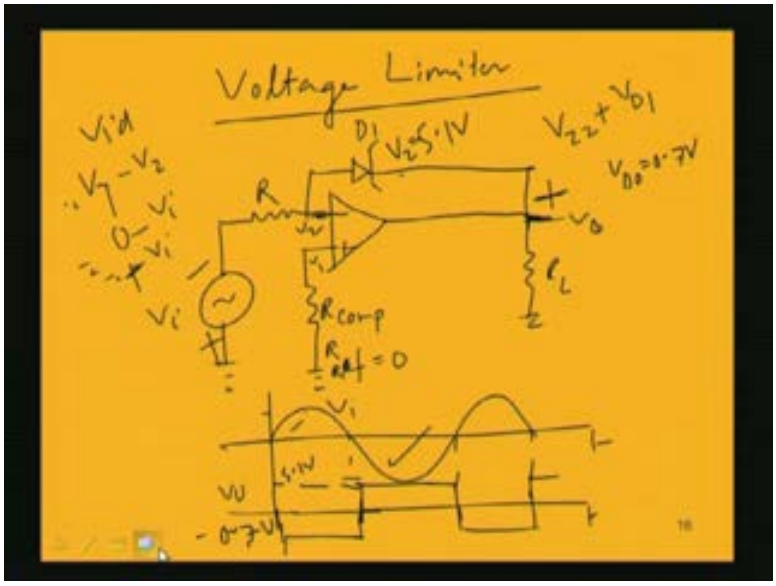

Then when it is in the negative half cycle, negative half cycle means this point is say negative, this point is positive. Then at this point we are getting a positive V_{sat} means 14 volt positive and suppose this Zener voltage is 5.1 volt, 5.1 volt V_z and V_{DO} is say 0.7 volt; then we will get 5.1. When this is positive, we will get this V_O as 5.1 volt. So, it will be like this one. This is 5.1 volt.

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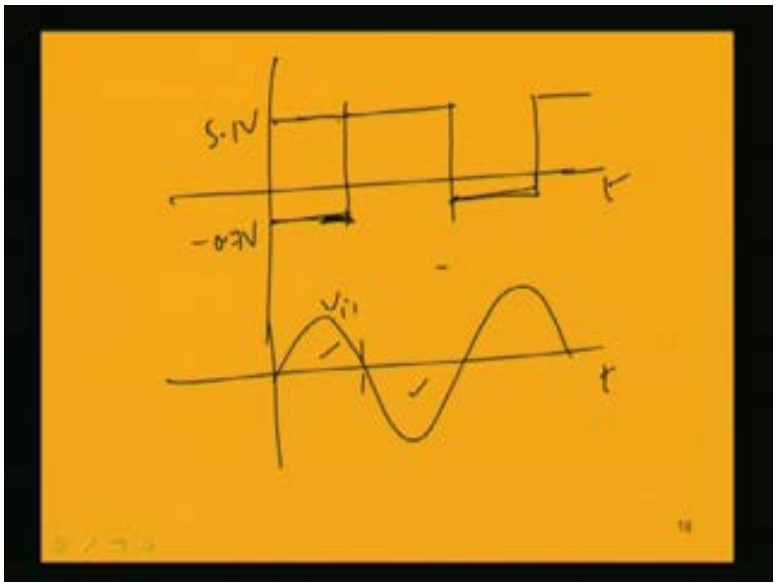

The two voltage magnitudes in the two halves are not equal. This is minus 0.7 volt, this is 5.1 volt; corresponding V input was this one. It is an inverting comparator. When this is positive we were getting a negative minus 0.7 volt. When it is negative we were getting a positive 5.1 volt. This is 5.1 volt. So, the overall voltage is like this. Here we are showing an example where we can reduce the output voltage or limit the output voltage which in the ordinary zero crossing detector we were getting around V saturation voltage of 14 volt or minus 14 volt, in the minus V saturation. But this is a too high voltage. In order to use it for digital circuit, we require a voltage which should not be beyond around 5 volt for 1 level or high level and the zero level is around zero voltage that we should get. That means whatever the zero crossing detector comparator was giving it was a voltage which was too high for use in the digital circuits.

Here in zero crossing detector we were having an example of the sinusoidal to square of conversion. That means we were getting an analog to digital type of conversion of the voltage. Given an analog input we were getting digital output in the zero crossing detector that we have seen. But that output was too high and it was almost not practical to use in digital circuits directly. We have to devise some other method and by using the Zener diode we could limit down the output voltage to an usable level of around 5 volt; we can limit it by using or choosing the proper Zener diode. Depending upon Zener voltage it will have the output value. If we choose around 5 volt Zener, we may not get the exact 5 volt, but near around 5 volt for using digital circuit we can get; by using that proper specification Zener diode that can be used for digital circuits.

This was an example where we have seen that an analog voltage or a sinusoidal voltage what we were using could be converted into a digital pulse and by using proper components like Zener diodes we could even get down to that usable digital voltage level and use it for our practical digital circuit. That is one use of comparator circuits which we can use in our digital devices. So, whenever we want to have a digital voltage from an analog sinusoidal voltage we can use that type of comparator like zero crossing detector.

In today’s class we have seen the basic circuit of comparators which compares the voltages at the two inputs of an op-amp and we have seen how the output voltage switches.