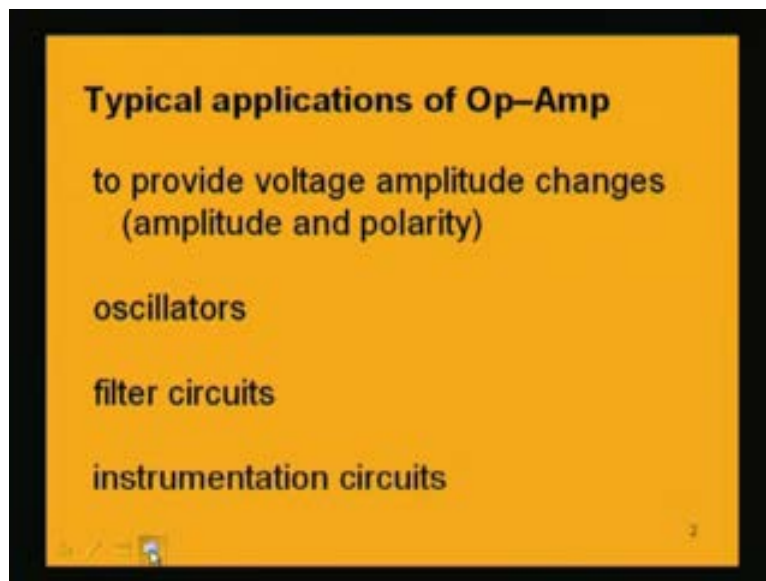


Basic Electronics
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Indian Institute of Technology, Guwahati

Module - 4
Operational Amplifier (Op-Amp)
Lecture -1
Operational Amplifier
(Introduction)

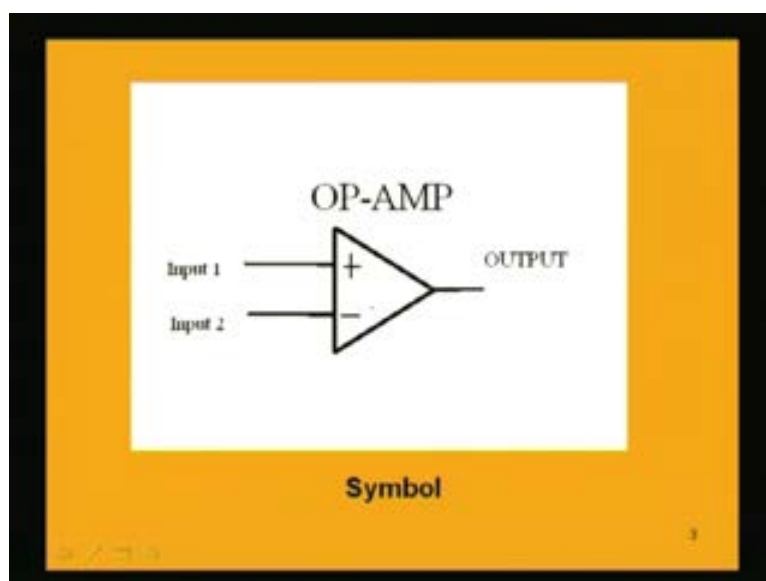
Today we shall be discussing about an important device known as operational amplifier or in short it is known as op-amp. The op-amp is basically a device where a number of differential amplifier stages are connected in series and the overall gain of the op-amp is made very high and the op-amp has very high input impedance. It is in the order of one or few mega ohm and its output impedance is very small. It is around say less than 100 ohm. The op-amp has a very high gain but low output impedance and high input impedance. This device is basically used in a number of applications. For example when we want to do mathematical operations in analog that is suppose we want to do summation, subtraction, integration, differentiation, etc, then this operational amplifier can be used to have its operation in such a way that we can effectively have these operations performed. That is why basically the name operational amplifier is coming from that, that it is used generally effectively to do a number of operations like in mathematical operations.

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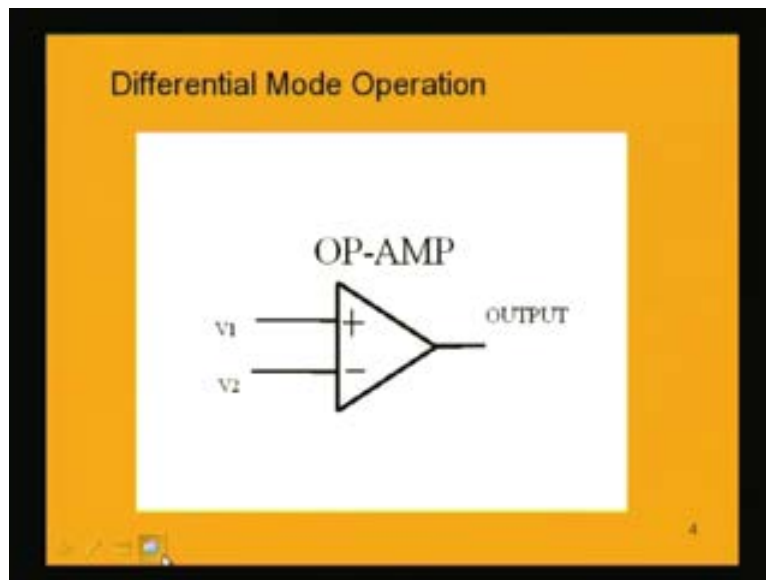
But apart from that the typical applications of op-amp is to provide voltage amplitude change and this voltage amplitude change as well as the polarity that means if we want to change the magnitude and polarity of an input voltage we can use this op-amp. Similarly if we want to use this in filter circuits for example we can use this op-amp to build filter circuits as well as in instrumentation amplifiers we can use this op-amp and also in oscillators. These are some of the typical applications of op-amp. Thus the op-amp symbol is having two input terminals.

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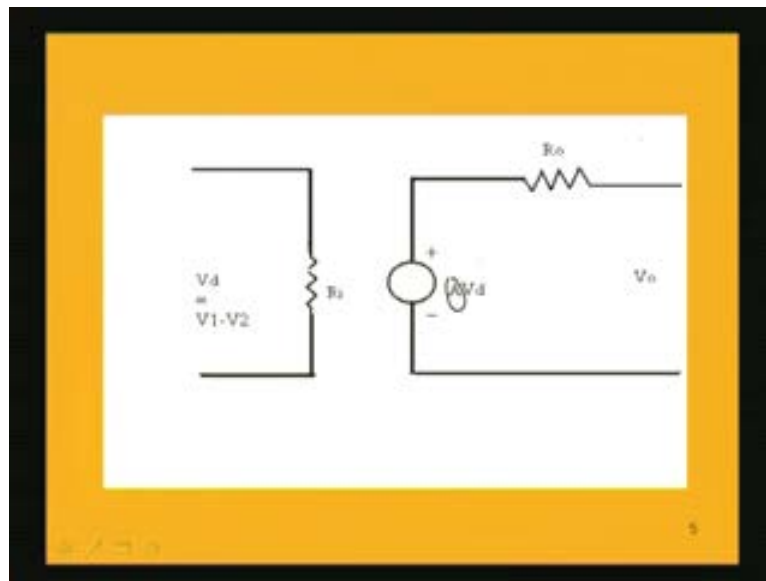
One is non-inverting and the other is inverting. The symbol of this op-amp is shown here. Here input_1 and input_2 , these two terminals are there in the op-amp. One terminal is non-inverting and the other is inverting and the output is obtained from the op-amp and this is the device symbol.

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As seen here, there are two input terminals. The voltages are applied at the two inputs. For example if we apply v_1 and v_2 at the two inputs, then the output voltage which we will obtain, will be dependent on the difference of the two voltages when we apply the op-amp in differential mode of operation. The output of the op-amp in differential mode of application will be dependent upon the difference in the two voltages v_1 and v_2 . If we want to find out the output voltage, we will have to take the circuit of this op-amp which is having an input impedance given by R_i and the output impedance is given by R_o .

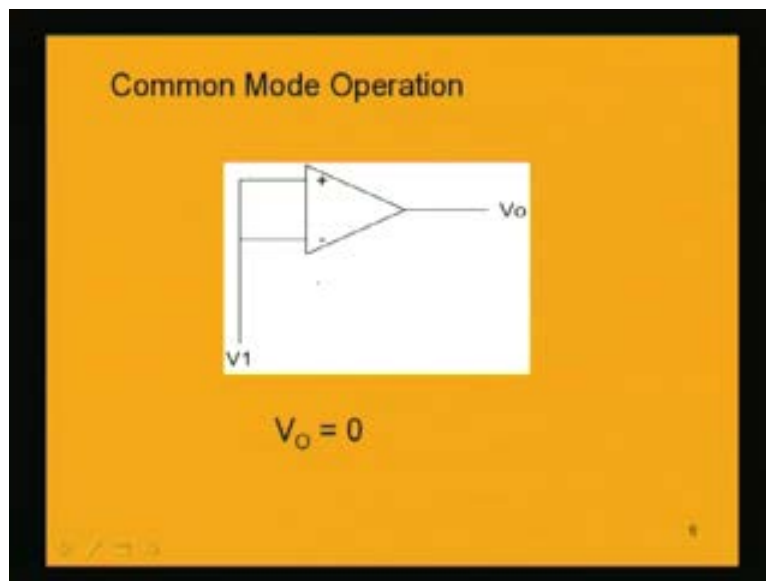
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Here basically they are resistances and the input voltage between these two terminals, which are the input terminals is the differential input given by difference between the two voltages at the input. That is v_1 minus v_2 is equal to V_d that is the differential input. If this is so then the output voltage which will be obtained at these two points will be A times V_d because V_d is the differential input. It is amplified by A times, A being the op-amp gain; this A being the op-amp gain. At these two terminals we get the voltage A times V_d . But then practically an op-amp has output impedance. Although it is very low, the R_o value will be the value of the output resistance.

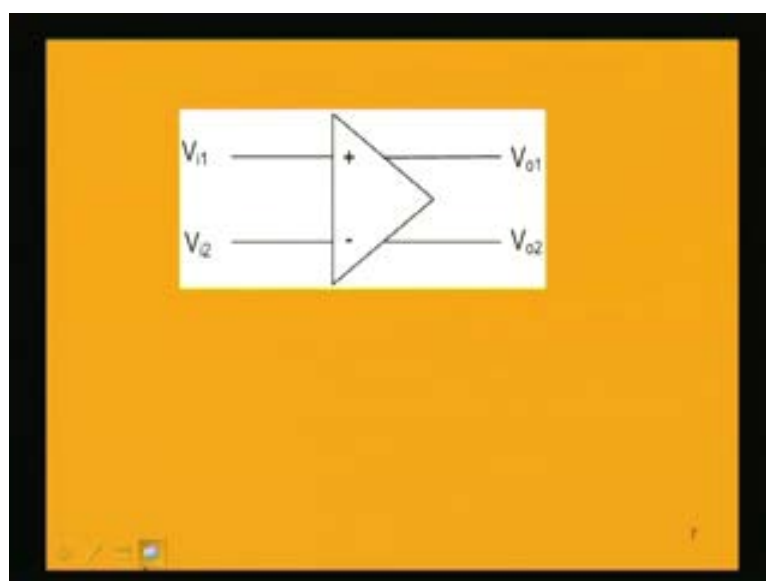
A part of this AV_d is dropped in this resistance and finally what we will get at the output v_o is AV_d minus this drop. But for all practical purposes since the op-amp is having very high input impedance and very low output impedance, we can ignore this drop in R_o . Practically we can say that the output voltage v_o is almost equal to A times V_d , where V_d is the differential input that is $v_1 - v_2$. That is the differential mode of operation of the op-amp. Now if we consider another mode which is known as common mode, the common mode of operation of this op-amp will have the input voltage v_i same to both the input terminals.

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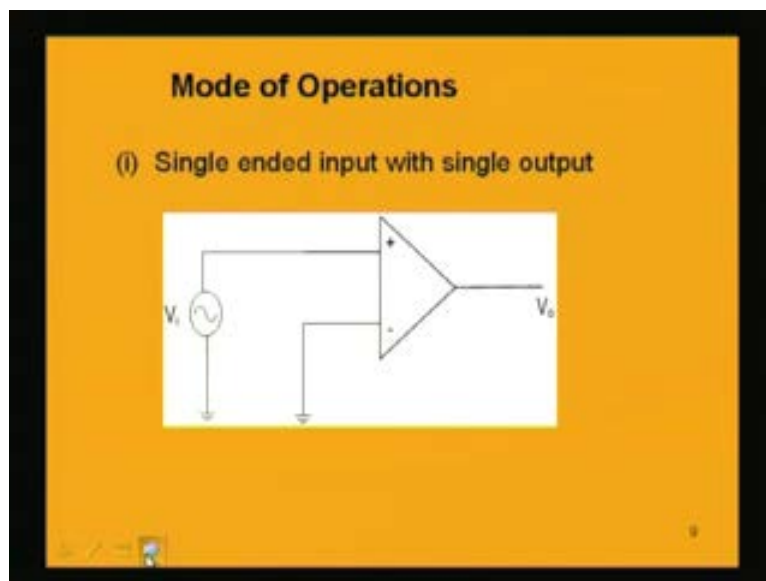
If this is so then output voltage will be zero because this v_1 minus v_2 is zero. Hence v_1 is same as v_2 ; same voltage is applied. So ideally in the common mode of operation, we should get a zero voltage at the output. These two are the basic modes of operations of the op-amp and differential mode of operation is that operation where we get a very high voltage at the output; that is the op-amp amplifies the differential input and in the common mode basically we get zero output if the op-amp is following all the ideal requirements in the circuit. We will discuss the basic structure of an op-amp.

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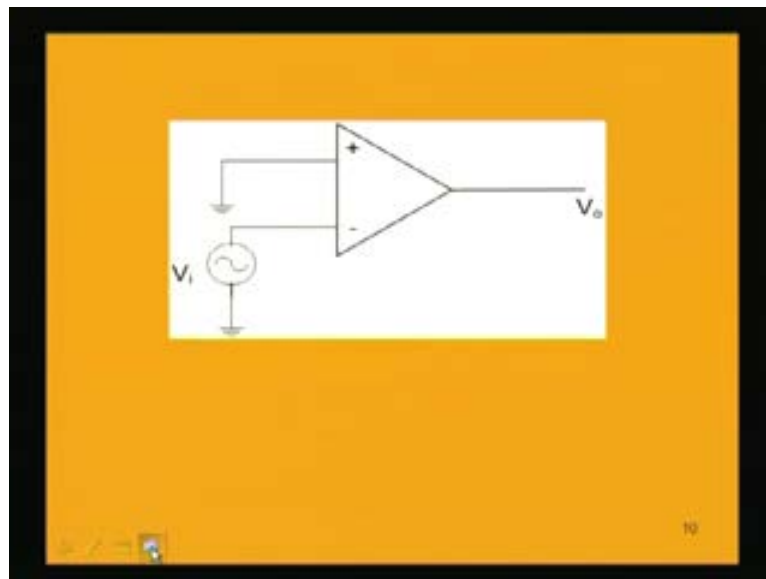
The op-amp has basically two input terminals and two terminals at the output where we can apply the voltage at the input side V_{i1} as well as V_{i2} and at the output side, we can get the output voltage at V_{o1} and also at V_{o2} . Another mode is that we apply differential voltage at the input between V_{i1} and V_{i2} . Suppose we are applying one voltage then at the output we can also have the voltage between these two terminals; that is in between V_{o1} and V_{o2} , we can have the voltage and we will explain the different modes of operations of an op-amp. There can be single ended operational, double ended operation both at the input and output.

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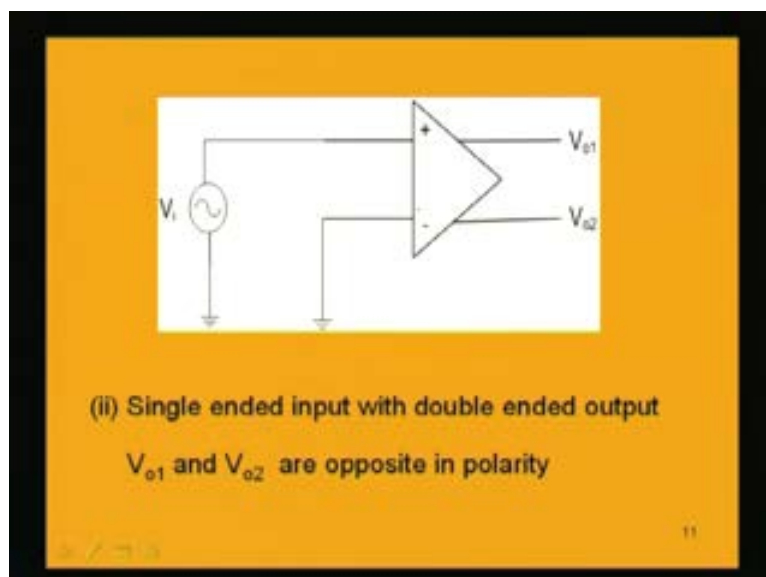
If we consider the single ended input and also consider the single ended output, then we are applying a voltage at the input which is non-inverting. For example this voltage is V_i . We are applying for example a sinusoidal AC input and other terminal which is the inverting terminal is grounded that means we are applying only a single voltage at the input and output obtained is at the single end; that is we are getting only at one end or we are getting a single output at the other side. We are having input one and output also one; single input and single output we are having here.

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Apart from this we can also have the other operation where we can apply the input at the inverting terminal. We can make the non-inverting terminal to ground and we get the single output. You can use one single source either at the non-inverting or at the inverting terminal and we also get a single output. That is one way we can operate the op-amp.

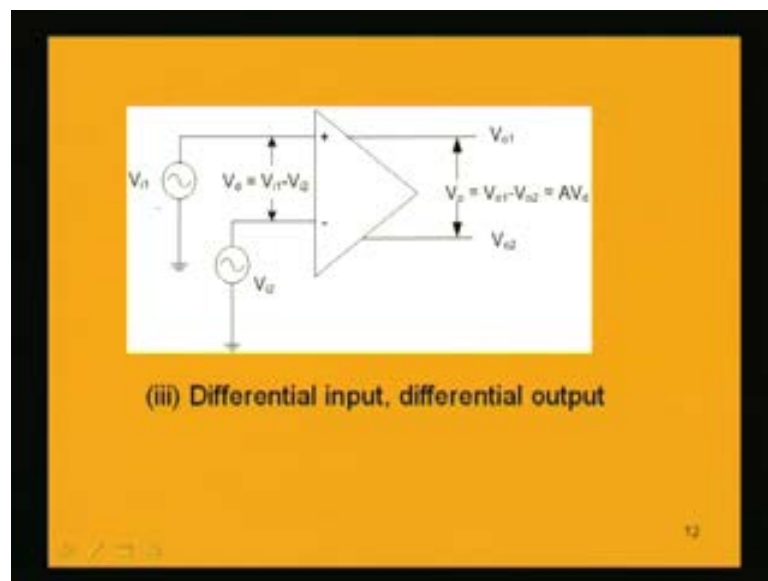
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Another way, we can have a single ended input, but we can get the outputs double ended. That means we can have two outputs V_{o1} and V_{o2} . This output V_{o1} and the

output V_{02} are opposite in polarity. That will be clear when we consider the internal circuitry but now we are just understanding in what ways we can connect the input sources and where we can get the output voltages? These are the ways. We can have a single source at the input either inverting or non-inverting, the other terminal being grounded and the output voltage can be obtained at a single point or we can have output voltage at both this output terminals V_{01} , V_{02} and in this case V_{01} and V_{02} are opposite in polarity. Also another way is that we can apply two sources at the two terminals which are non-inverting and inverting.

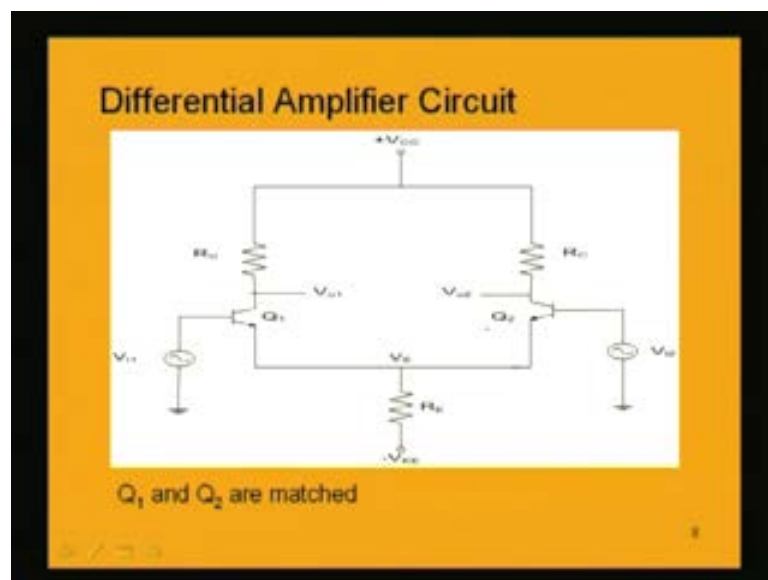
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Like in this case we are applying V_{i1} at the non-inverting terminal and V_{i2} at the inverting terminal. The differential voltage which is applied between plus and minus terminals of the input is V_{i1} minus V_{i2} ; that is the differential input which is applied at the input of the op-amp. Now the output of the op-amp we have two terminals V_{01} and V_{02} , where the V_{02} voltage, if we consider, that will be opposite in polarity with V_{01} . If we find out this voltage V_o in between these two terminals that will be equal to V_{01} minus V_{02} and that is nothing but A times V_d . A is the op-amp gain multiplied by the differential input. Here we are applying a differential input and getting differential output. The input is differential because we are having two voltages at these two terminals, non-inverting and inverting. Definitely the input voltage will be the difference between the two and that voltage we are denoting by V_d ; that is the differential input and that is nothing but the difference between the two input voltages

and output also we are getting differential, the difference between the two output voltages V_{01} and V_{02} . These are the different ways we can have the input sources connected to the op-amp and also get the output. What is the internal circuit of an op-amp?

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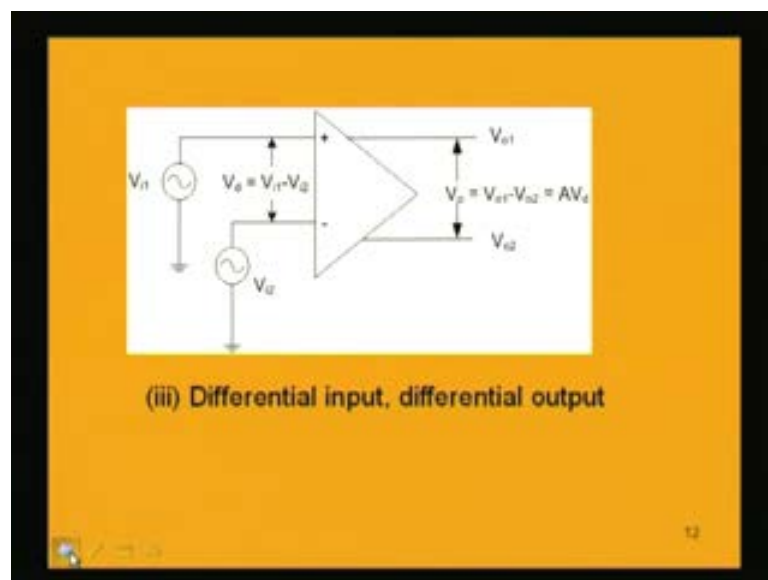
What is there in the inside of op-amp? For knowing that the basic building block of an op-amp has to be understood; that is nothing but a differential amplifier. A differential amplifier circuit is shown here. Let us consider this circuit and try to understand its details. There are two transistors in this differential amplifier circuit. One is Q_1 and one is Q_2 . These two transistors are perfectly matched. Their beta values must be exactly equal and the internal resistances R_e , etc, which are there inside this transistor must be also equal for both the transistors. That means the two transistors Q_1 and Q_2 must be perfectly well matched and this type of matched transistors are used in this differential amplifier circuit. We have this Q_1 and Q_2 which are two well matched transistors and the resistances which are connected in the collectors for these two transistors are R_C ; that is same value R_C is to be connected here and here.

There is another resistance R_e in the emitters of the two transistors which are connected. If we consider these two transistor emitters, this is the emitter of transistor Q_1 and this is the emitter of transistor Q_2 . These two emitters are connected and then it is connected to a resistance R_e and the biased voltages V_{CC} and minus V_{EE} is there

which is connected to R_c . These are two npn transistors which we are considering. In the op-amp internally this circuitry is present. When we are applying a voltage at the two input terminals these are shown here. V_{i1} and V_{i2} are the two input voltages connected to the two input terminals and the output voltages are obtained at V_{o1} and V_{o2} , at the points of the collector. Across the collector of the transistors we are having the output voltages V_{o1} and V_{o2} .

Basically this is the internal circuit and we will have a number of differential amplifier stages in the op-amp. That means we are considering only a single differential amplifier circuit but there will be number of stages of this differential amplifier circuits which are directly coupled and the overall gain will be very high because they are cascaded, they are in series. After all the cascading stages whatever we will get, that will be the gain of the op-amp. It is very high value.

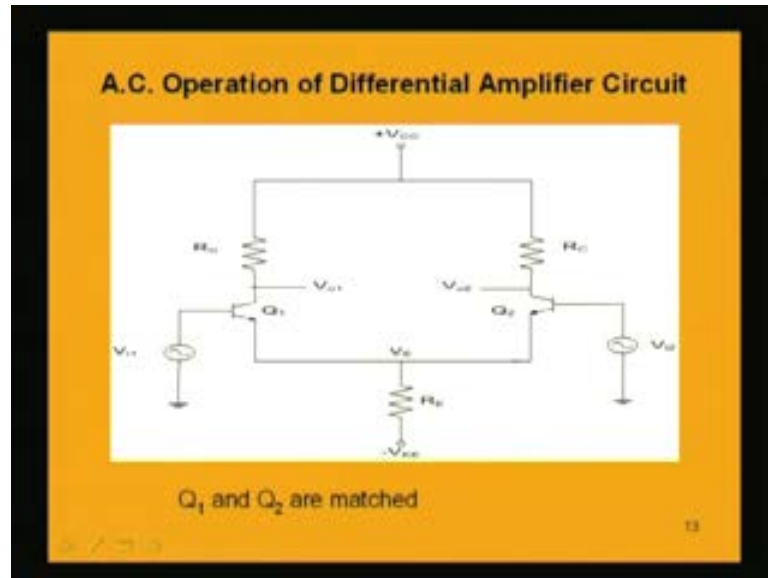
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If we want to know the operation of an op-amp, let us consider the operation of an op-amp in the differential mode because we have seen there are two modes of operations, differential as well as common mode. In the differential mode we have two input voltages and their difference is the differential input. That particular mode of operations let us consider now and we are considering AC operation, meaning we are applying AC voltages at the input side. These two transistors should be perfectly matched; that is the prime condition to be satisfied. That is why we will have the same

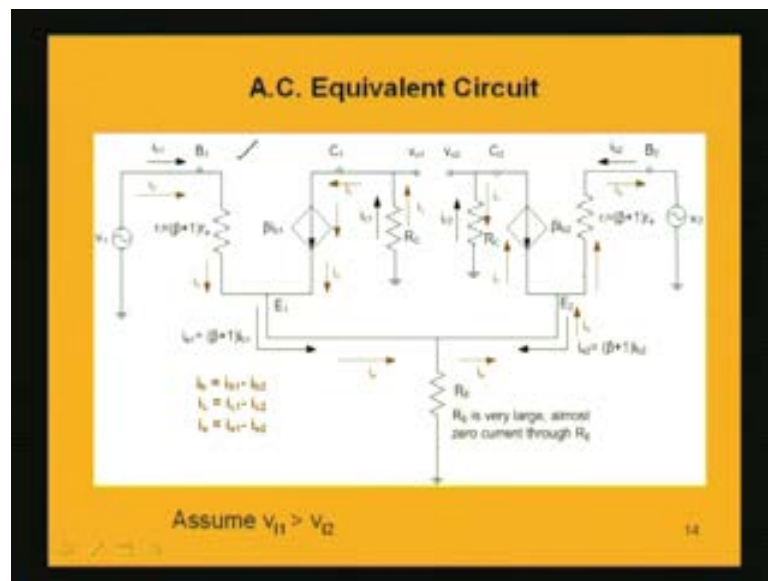
beta value for the two transistors as well the emitter resistance of the transistors in both the cases of the two transistors is same. Emitter resistance, R_e that is the resistance in the emitter base forward biased junction will have the same value.

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If we analyze this circuit under AC then we will have to draw the AC equivalent circuit for the whole amplifier. The differential amplifier circuit has to be analyzed under AC and that requires drawing the AC equivalent circuit. Following the procedure for drawing the AC equivalent circuit let us try to find out what will be the AC equivalent circuit for this differential amplifier.

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Starting from this input voltage V_{i1} if you proceed, then this is base, this is emitter and this is collector. The base emitter or emitter base junction will have the resistors and that is equal to r_i if you say, $\beta + 1$ into r_e will be the resistance between base and emitter. The input voltage V_{i1} , then consider the base terminal of the first transistor Q_1 . Then V $\beta + 1$ into r_e that is the resistance between base and emitter; that is emitter base junction is having the resistance $\beta + 1$ r_e that we have earlier derived while discussing the transistor model. We are just replacing that equivalent circuit or the model of the transistor. The first transistor model is this part; Q_1 is having B_1 , C_1 and E_1 corresponding to the base, collector and emitter terminals.

Between emitter and base this is the resistance, which is r_i . We are naming r_i just to denote that it is the input resistance of the transistor and that value is $\beta + 1$ r_e and we have derived that earlier. This is the emitter point and collector C_1 is having the current source which is β times of i_{b1} , i_{b1} being the current in the base terminal of the transistor Q_1 . i_{b1} will be dependent on the source V_{i1} and on this i_{b1} will be dependent the collector current i_{c1} . That is β into i_{b1} is i_{c1} and if we now consider the collector point and look back into this circuit, this collector is connected through R_C that is the resistance in the collector is R_C and as we are considering the AC equivalent circuit, the DC biasing V_{CC} will be grounded; that will be zero. That means the collector will be connected to ground through this resistance R_C in the AC

equivalent circuit and that is what is happening here. The collector C_1 through this resistance R_C is grounded.

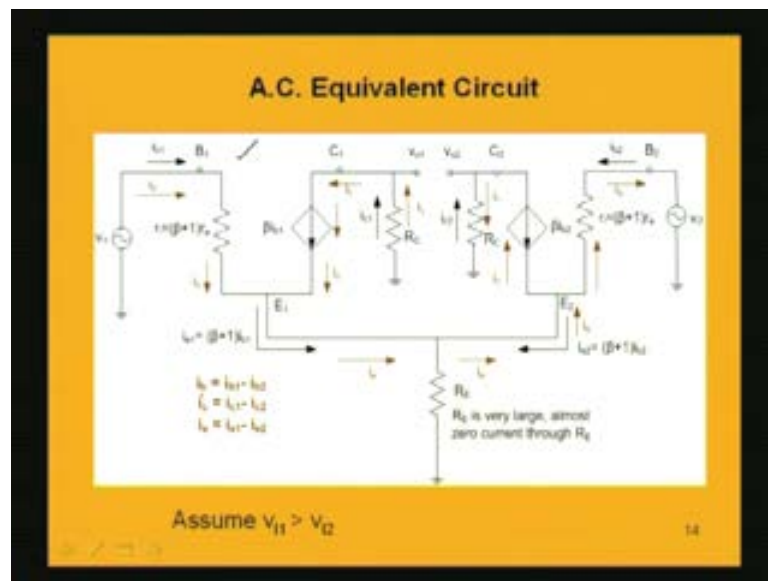
If we consider only this Q_1 circuit or transistor Q_1 model, then the B_1 , C_1 and E_1 points give you the model of the transistor Q_1 , which is having the input resistance r_i which is $\beta + 1$ into r_e and the current i_{c1} , this is the current i_{c1} , is β times of i_{b1} . If we consider the E_1 point that means emitter point of the transistor Q_1 , then this E_1 is grounded through the resistance R_e . That is clear here because this E_1 point is connected to minus V_{EE} and for AC equivalent circuit this will be grounded. That is why E_1 through R_e will be grounded and that is represented here; E_1 through R_e is grounded. If we look into the directions of current in the transistor Q_1 , i_{b1} and i_{c1} that is the current which flows through the collector resistance and it will be joined by the base current i_{b1} at the emitter point and the current flowing will be i_{c1} $\beta + 1$ into i_{b1} , which is equal to nothing but i_{b1} plus i_{c1} . These correspond to transistor Q_1 currents.

Similarly if we consider the transistor Q_2 , the transistor Q_2 is having the base collector and emitter points represented by B_2 , C_2 and E_2 and due to this source V_{i2} , you see here V_{i2} is connected as input to the second transistor Q_2 . This base is getting the current due to this source V_{i2} . This current in the base terminal of the transistor Q_2 is i_{b2} . That is shown here. i_{b2} is the base current in the transistor Q_2 and this current which flows in the transistor Q_2 at the collector terminal is denoted by i_{c2} and the current in the emitter is i_{e2} . The resistance in the emitter base junction for the transistor of Q_2 is same r_i . For transistor Q_1 also it was r_i ; so same value of resistance r_i . Since the transistors are matched same β value and that is why r_i is the resistance between the emitter and base and that is equal to $\beta + 1$ into r_e and the current which flows in the collector is i_{c2} , which is nothing but β times of i_{b2} and that is the current source which is i_{c2} and this current flows in this direction through this resistance R_C because if you look into this resistance, the collector current will be flowing through the R_C in this direction towards the transistor. It is an npn transistor and that is why the base current and collector current will be towards the transistor and the emitter current will be away from the transistor. That is why emitter current i_{e2} is shown by this direction which is $\beta + 1$ into i_{b2} .

Consider the resistance capital R capital E, which is connected to E_1 and E_2 . The current which will flow through this resistance is made zero by making R_E very high. In this circuit you assume that the resistance R_E is very large and that is why the current through this resistance R_E is almost zero. So that assumption is made or we have to basically make this circuit like this only. Then we can proceed further easily by making this R_E very high we are making the current through this resistance almost zero. If we look into the circuit as a whole we are having two sources V_{i1} and V_{i2} due to which there are currents flowing and so if we consider V_{i1} only making this V_{i2} zero, we will have only the currents due to V_{i1} and if I make V_{i1} zero and keep V_{i2} only then we are getting the currents due to V_{i2} only. As this circuit is a linear circuit, we have to maintain that condition intact that is it is a linear circuit. Only under the assumption of the linear circuit we will proceed to find out the impact of both the sources on the currents flowing in the circuit. That is why using the linear circuits property now we can combine the effects due to V_{i1} and V_{i2} and find out the currents which are flowing due to both V_{i1} and V_{i2} acting on the circuit. If both are present then we will combine the currents due to each of the sources individually. So the assumption which is to be made now is that the amplitude of V_{i1} and amplitude of V_{i2} which is greater because the directions of current when V_{i1} and V_{i2} both are applied will be dependent upon their magnitudes.

If we consider that V_{i1} is greater than V_{i2} , the value or magnitude of V_{i1} is greater than V_{i2} , then the unbalanced current will be flowing in the direction shown by the red colored arrows because now we are having the current which is flowing finally due to both V_{i1} and V_{i2} . We are having the currents i_{b1} due to V_{i1} and i_{b2} due to V_{i2} . These are the base currents; for example we are considering base currents due to the two sources. V_{i1} is having a base current i_{b1} and due to V_{i2} , the base current flows, which is i_{b2} . When they are acting at the same time, both V_{i1} and V_{i2} are acting at the same time, the unbalanced or the final current which we will be left with is denoted by say i_b which is nothing but i_{b1} minus i_{b2} .

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If we consider V_{i1} is greater than V_{i2} , as the transistors are perfectly matched, definitely the base current due to V_{i1} must be greater than the base current due to V_{i2} . That is why i_{b1} is greater than i_{b2} . The current which will flow in the base that is overall base current if we consider that is equal to i_{b1} minus i_{b2} which is shown by this red line and the direction is shown in this because as V_{i1} is greater than V_{i2} , finally the current will start from V_{i1} and it will flow in this direction. Similarly if we consider collector current, i_c is the unbalanced collector current, i_c is equal to i_{c1} minus i_{c2} . Similarly i_e is equal to i_{e1} minus i_{e2} and the direction of these unbalanced currents are shown by this red arrow; that is i_b will flow in this direction, i_c will flow in this direction. They meet together at this emitter point and total emitter current that is i_b plus i_c is equal to i_e . Then it will flow in this direction and then one part will flow which is i_b and the other part is i_c . The overall direction of these currents is shown by this red line.

Now we are denoting the final unbalanced current by the red line. The base current which is finally flowing will be i_b in this direction which is equal to i_{b1} minus i_{b2} and the collector current which will finally flow that is equal to i_{c1} minus i_{c2} is in this direction. Both are meeting to give i_e which is i_b plus i_c and that will flow in this direction. Again one part will be the base current i_b in this transistor and the other part will be the collector current. This will finally be the currents which will flow when both the V_{i1} and V_{i2} are there. We are interested in finding out the voltages at the

output. So V_{01} and V_{02} are the voltages that we need to find out. So what is V_{01} ? We can see that V_{01} is nothing but the voltage drop across R_c due to the current flow i_c . but it will be minus since current is flowing in this direction. So i_c into R_c with a minus sign will be V_{01} and V_{02} will be i_c into R_c with a positive sign because the direction of current is from top to bottom. So V_{01} and V_{02} are opposite in polarity but magnitude wise they are equal.

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Assume $V_{i1} > V_{i2}$

Using KVL,

$$v_{i1} - (i_{b1} - i_{b2})r_i - (i_{b1} - i_{b2})r_i - v_{i2} = 0$$

$$\text{or, } 2(i_{b1} - i_{b2})r_i = v_{i1} - v_{i2}$$

$$\text{or, } i_b = i_{b1} - i_{b2} = \frac{v_{i1} - v_{i2}}{2r_i}$$

$$i_e = i_{e1} - i_{e2}$$

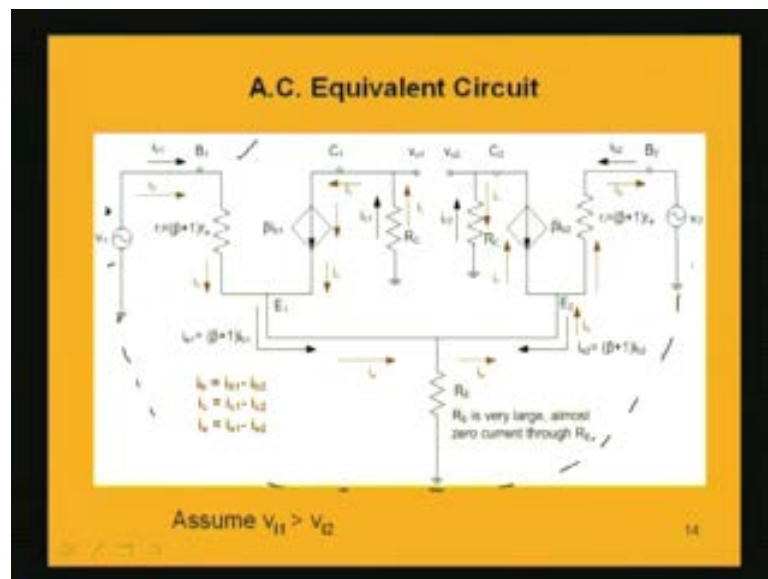
$$= (\beta + 1)(i_{b1} - i_{b2}) = (\beta + 1) \left[\frac{v_{i1} - v_{i2}}{2r_i} \right] = (\beta + 1) \left[\frac{v_{i1} - v_{i2}}{2(\beta + 1)r_e} \right]$$

$$= \frac{v_{i1} - v_{i2}}{2r_e}$$

$$= \frac{v_d}{2r_e}$$

First of all let us find out the base current i_b . As is clear in this circuit we need to apply Kirchhoff's voltage law. Applying Kirchhoff's voltage law we will find out the base current. So apply Kirchhoff's voltage law starting from this source V_{i1} . So what will it be? V_{i1} minus i_b into r_i is this drop minus these drop. We are starting from the source V_{i1} . So we will follow this loop up to source V_{i2} and then ground. We need to find the Kirchhoff's voltage law in this loop which comprises V_{i1} and V_{i2} and then ground. So this is one loop. This ground and ground they are combined so we will be basically having a loop.

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You need to find out the drop in this direction. This is nothing but V_{i1} . We are staring from this point say minus plus, so V_{i1} . Actually we are considering in this way minus to plus; this is a rising voltage V_{i1} minus this drop is i_b into r_i minus this drop is i_b into r_i again, minus V_{i2} is equal to zero.

What is i_b ? i_{b1} minus i_{b2} . That is what is done here. V_{i1} minus i_{b1} minus i_{b2} into r_i minus i_{b1} minus i_{b2} into r_i minus V_{i2} is equal to zero. Simplifying this equation we get two times i_{b1} minus i_{b2} into r_i . These two are equal to V_{i1} minus V_{i2} , transferring this to the left hand side. i_{b1} minus i_{b2} equal to i_b , unbalanced current, finally what is remaining in the circuit that is equal to V_{i1} minus V_{i2} by 2 times r_i . r_i is nothing but the input resistance in the transistor which is equal to beta plus 1 into r_e . r_e is the emitter resistance which is 26 millivolt by capital I capital E that we know and now what is the collector current i_c ?

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Assume $V_{i1} > V_{i2}$

Using KVL,

$$V_{i1} - (i_{b1} - i_{b2})r_i - (i_{b1} - i_{b2})r_i - V_{i2} = 0$$

$$\text{or, } 2(i_{b1} - i_{b2})r_i = V_{i1} - V_{i2}$$

$$\text{or, } i_b = i_{b1} - i_{b2} = \frac{V_{i1} - V_{i2}}{2r_i} \quad r_i = (\beta + 1)r_e$$

$$i_c = i_{c1} - i_{c2}$$

$$= (\beta + 1)(i_{b1} - i_{b2}) = (\beta + 1) \left[\frac{V_{i1} - V_{i2}}{2r_i} \right] = (\beta + 1) \left[\frac{V_{i1} - V_{i2}}{2(\beta + 1)r_e} \right]$$

$$= \frac{V_{i1} - V_{i2}}{2r_e} \quad V_{i1} - V_{i2} = V_d$$

$$= \frac{V_d}{2r_e}$$

Collector current i_c equal to i_{c1} minus i_{c2} and i_e equal to i_{e1} minus i_{e2} . The emitter current finally what is flowing in the overall circuit is the unbalanced circuit or final current i_e that is equal to i_{e1} minus i_{e2} which is nothing but beta plus 1 into i_{b1} minus i_{b2} that is equal to beta plus 1 into i_{b1} minus i_{b2} , which we have just now derived. This is V_{i1} minus V_{i2} divided by 2 times r_i that is equal to beta plus 1 into V_{i1} minus V_{i2} by 2 times r_i . Replacing this r_i by beta plus 1 r_e , we get this equation. We can very easily cancel beta plus 1 and beta plus 1. Finally we are left with V_{i1} minus V_{i2} by 2 times small r small e . Again denoting V_{i1} minus V_{i2} by V_d , differential input voltage replacing that by V_d we are getting finally i_e equal to V_d by 2 times r_e . After this derivation let us find out the output voltage.

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$$V_{o1} = -i_c R_C = -\beta i_b R_C = -\beta \frac{V_d}{2r_i} R_C$$

$$V_{o2} = i_c R_C = \beta i_b R_C = \beta \frac{V_d}{2r_i} R_C$$

$$V_o = V_{o1} - V_{o2} = -2\beta \frac{V_d}{2r_i} R_C = -2\beta \frac{V_d}{2(\beta+1)r_e} R_C \approx -\frac{V_d R_C}{r_e}$$

Differential Gain of Op - Amp

$$A_{v_d} = \frac{v_o}{v_d} = -\frac{R_C}{r_e} = A_d$$

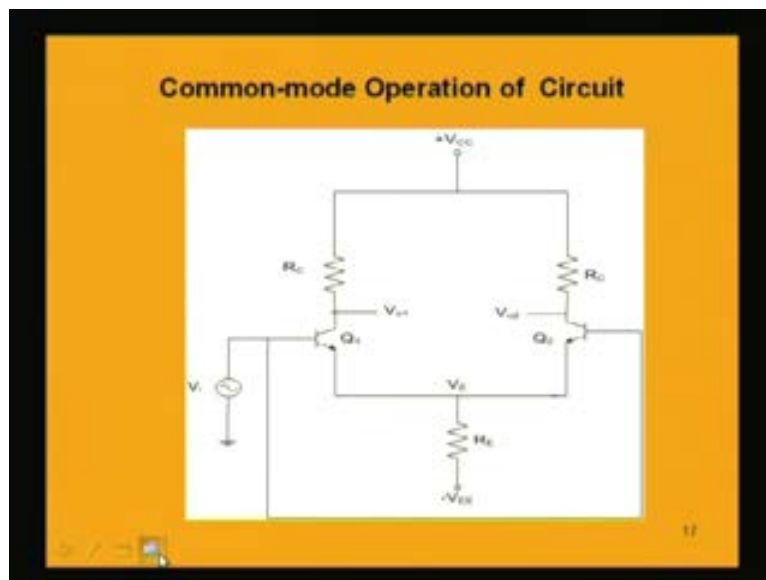
$\beta \approx \beta + 1$

What is this output voltage V_{o1} that is minus i_c into R_C and that is equal to minus beta times of i_b into R_C and i_b we have found out which is nothing but V_d by 2 times r_i . V_{o1} minus V_{o2} is V_d . So it is written in this way, V_d by $2r_i$. So V_d by $2r_i$ we are replacing and multiplied by R_C . This is V_{o1} . What about V_{o2} ? V_{o2} is equal to i_c into R_C with positive sign because the direction of V_{o2} is same as the direction of this drop $i_c R_C$. $i_c R_C$ is positive in this case, V_{o2} and which is equal to same in magnitude with this V_{o1} that is equal to beta times of $i_b R_C$ and that is equal to beta into V_d by twice r_i into R_C .

We want to find out the differential output voltage between V_{o1} and V_{o2} terminals. That is in between these two output terminals if we want to find out the difference in the voltages that is the output voltage, which is the differential output voltage and that is equal to V_{o1} minus V_{o2} which is equal to, simply replacing these values, minus beta times V_d by $2r_i$ into R_C minus this whole term. So minus minus it will be minus 2 beta times V_d by $2r_i$ into R_C . Now replacing r_i by beta plus 1 r_e we can simplify with a little approximation, the approximation being beta is almost equal to beta plus 1. Since beta value is typically a high value, we can very well approximately equalize beta and beta plus 1 and that assumption is effectively used here. So we are getting finally cancellation of beta and beta plus 1; 2 and 2 cancel out. What we get is that the output voltage which is the differential output voltage at the output terminals of the op-amp under differential mode of operation is equal to minus V_d into R_C by small r small e , this V_d being the differential input voltage.

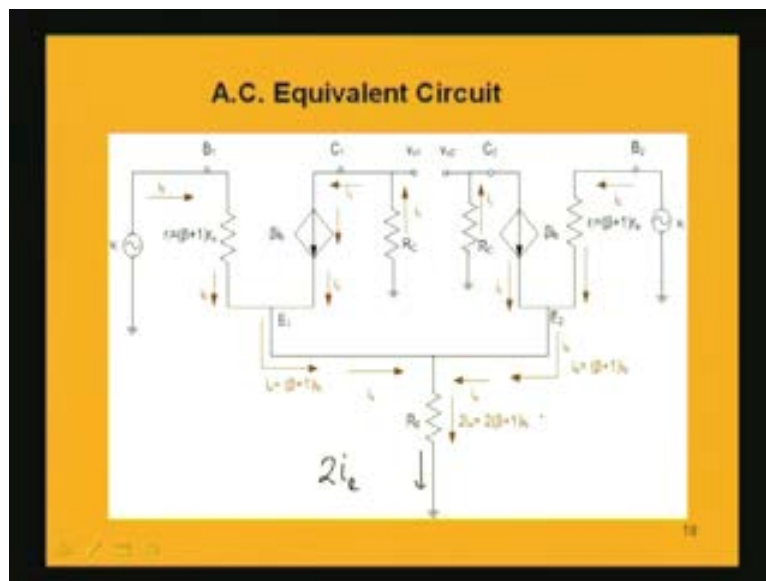
We can now determine the quantity, differential gain. What is the differential gain of the op-amp? AV_d is the differential gain of the op-amp or we can write A_d rather differential gain. This is the acronym used for the differential gain A subscript small d that is equal V_o by V_d . Take the ratio between V_o by V_d . It is equal to minus capital R capital C divided by small r small e . This is the differential gain of the op-amp and we can intuitively see that the value of r_e is very small; it is in the order of ohm but typically the value of R_C is high in the order of kilo ohm or even more than that. As a result of this division we are getting a very high value. Since the denominator is small compared with the numerator we are getting a high value. That is the op-amp is having a very gain in the differential mode of operation.

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Another mode of operation is common mode operation of the op-amp. In the common mode of operation we are connecting the voltage V_i common to both the input terminals. As you see here V_i is connected to both the input terminals of the op-amp. In the differential amplifier circuit if you see this V_i is connected to the base of Q_1 as well as base of Q_2 , thus being the same circuit.

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In order to analyze this under AC operation, the AC equivalent circuit if we draw the circuit will be similar to the earlier case of differential mode of operation. But here we are not making the assumption that r_e is very high. That is there is current flow in the r_e unlike in the previous example of differential mode of operation where we made r_e to be very high so that there is almost zero current in the resistance r_e but not in this case. What will happen is that you are applying the same voltage to both the transistor input. So V_i is input to the transistor Q_1 as well as transistor Q_2 . That means what? The base current which will flow in the transistor Q_1 and the base current which will be flow in the transistor Q_2 are same. Because the transistors are perfectly matched, we are having same beta value; same input source we are applying, so same base current is flowing. The resistance r_i between emitter and base is equal to beta plus 1 r_e ; that is also same in both the cases. R_C is connected in the collector. In both the transistors we are having the same R_C .

The current flow in the transistor Q_1 will be i_b . It will in this direction. i_c will be beta times of i_b in this direction. Total current in the emitter of the transistor Q_1 is beta plus 1 into i_b which is in this direction. In the second transistor Q_2 , similarly i_b will be flowing in this direction. i_c which is equal to beta times of i_b will be flowing in this direction. The total emitter current which will flow in the terminal e_2 or emitter terminal of the second transistor Q_2 will be beta plus 1 into i_b . This current is flowing in this direction which is i_e . Another i_e is flowing in this direction. They will combine

and they will together flow through this resistance r_e . So the total current flowing through this resistance r_e is equal to 2 times small i small e . i_e due to this part, another i_e due to this transistor. So total will be two times of i_e , flowing in this transistor R_E ; so that is nothing but 2 times beta plus 1 into i_e .

We want to find out V_{01} and V_{02} at the two ends of the output terminals. Let us find out the output voltage. What is this V_{01} ? That is i_c into R_C but with a negative sign. Similarly in this case V_{02} also will be same i_c into R_C with a negative sign. You mark the difference from the earlier example. Earlier V_{01} and V_{02} were opposite in polarity but now in this common mode of operation $i_c R_C$ is the output voltage which is present at V_{01} as well as in V_{02} and they are of the same polarities. That means this is also minus $i_c R_C$ and this is also minus $i_c R_C$; V_{01} and V_{02} are same. Let us apply Kirchoff's voltage law in this circuit. That is we apply Kirchoff's voltage law from V_i this source and the transistor Q_1 and travel through this resistance again, travel through the resistance R_E to ground what we get V_i minus i_b into r_i minus 2 times i_e capital R capital E equal to zero; so that is represented here.

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Using KVL,

$$v_i - i_b r_i - 2(\beta + 1)i_b R_E = 0$$

$$\text{or, } v_i - i_b(\beta + 1)r_i - 2(\beta + 1)i_b R_E = 0$$

$$\text{or, } v_i - i_b(\beta + 1)(r_i + 2R_E) = 0$$

$$\left(\text{or, } i_b = \frac{v_i}{(\beta + 1)(r_i + 2R_E)} \right)$$

$$v_o = v_{o1} = v_{o2} = -i_c R_C = -\beta i_b R_C = -\frac{\beta}{(\beta + 1)(r_i + 2R_E)} v_i R_C \approx \frac{-v_i R_C}{(r_i + 2R_E)}$$

$\beta \approx \beta + 1$

$$v_o \approx -v_i R_C / (r_i + 2R_E)$$

$v_o = v_{o1} = v_{o2} = 0$

We are getting Kirchoff's voltage law given by V_i minus i_b into r_i minus 2 times i_e is written as beta plus 1 i_b into R_E is equal to zero. This is actually V_i minus i_b into r_i minus 2 i_e into R_E that is equal to zero. Here this i_e is represented as beta plus 1 i_b . Simplifying it, we get V_i minus i_b into beta plus 1, we can take common; what we are

left with is small r_e plus 2 times of capital R capital E. Here we are representing r_i by beta plus 1 r_e . After that we are taking common beta plus 1 R_E into i_b ; that is common. From this equation we can get i_b . The base current is given by V_i by beta plus 1 into r_e plus 2 capital R capital E. So this is the base current. If this is the base current we can find out the output voltage at both the terminals V_{o1} which is equal to the voltage V_{o2} and that is equal to nothing but minus i_c into R_C in both the cases. Polarity of this voltage is plus with respect to ground. Current is flowing from bottom to top with a drop with this polarity plus to minus from bottom to top. So it is opposite. V_{o1} is minus i_c into R_C and here also same case; we get that is equal to minus i_c is nothing but beta times of i_b into R_C .

We can replace i_b from the previous expression. So we get minus beta into V_i by beta plus 1 into r_e plus twice capital R capital E into R_C . After assuming that beta is equal to beta plus 1, approximately we can write this is equal. If we approximately equalize then we can cancel these two terms. Finally we are left with approximately an expression which is minus V_i by minus V_i into R_C by small r_e plus 2 times of capital I. That is the final expression that we get for the voltage gain in the two terminals of the op-amp output under common mode of operation.

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Single ended Voltage gain of the Op-Amp

$$A_v = \frac{v_{o1}}{v_i} = \frac{-R_C}{r_e + 2R_E}$$

Double ended voltage gain of the Op - Amp

$$A_c = \frac{v_o}{v_i} = -\frac{v_{o1} - v_{o2}}{v_i} = 0$$

If transistors are not matched and $R_{C1} \neq R_{C2}$, A_c will not be 0

If we want to find out the difference in the voltage V_{o1} minus V_{o2} , then we can do that also. As this V_{o1} and V_{o2} are equal, V_o will be equal to zero. So under common mode

of operation the differential output will be zero. If we take the single ended voltage gain, we can find out V_{01} by V_i . If I find out single ended voltage gain what we have got is this expression. So V_{01} divided by V_i will be minus R_C by small r_e plus twice capital R capital E . This is the single ended voltage gain under common mode of operation and double ended voltage gain is zero because the differential output V_0 is V_{01} minus V_{02} and that is equal to zero. Finally we have got one important conclusion that if we want to find out the common mode voltage gain of the op-amp with respect to double ended output voltage that will be zero because output voltage between the two terminals under common mode of operation is zero. That is one important aspect of op-amp because if we have a voltage which is common to both the inputs then if the transistors are well matched and the resistance R_C is exactly same for both the transistors we ideally should get zero voltage. But that sometimes doesn't happen because it is very difficult to get exactly matched transistors having the same beta values and the input resistances etc and also the value of R_C in both the transistors which are connected at the collector side are rarely exactly equal. Because of this difference in the resistances in the two transistor collectors that is R_C is not exactly equal, the two transistors are not exactly matched because of this fact.

Practically we do not get a zero voltage under common mode operation; a very small voltage you get in the common mode of operation is because of this fact. If the transistors are not well matched and R_{C1} and R_{C2} is not exactly equal then A_C that is the common mode gain will not be zero. In this analysis whatever we have found today is differential mode gain and common mode gain and these two are the two basic gains which we will deal with very frequently. This analysis today what we have done is about a very important device in electronics that is operational amplifier which is a cascaded amplifier. The individual units of this cascaded arrangement are differential amplifier. A number of stages of differential amplifiers are cascaded to finally give a very high amplification or gain and this op-amp has very high input impedance value but output impedance is very small.

The op-amp is basically used in a number of applications starting from mathematical operations in analog computers as well as filter circuits and instrumentation amplifiers and oscillators and different combinations of the circuits are used to get our desired operation. Basically we apply op-amp's for a number of operations including

mathematical ones and those applications we will discuss in our next succeeding lectures. But the basic idea of the op-amp is that we have two operations or operating modes; differential mode of amplification as well as common mode amplification and in common mode amplification, ideally output voltage should be zero. In differential mode of operation we get a very high output voltage and we will see later that in practice we get a number of applications of this op-amp and we will discuss those applications and we will find out what mathematical operations can be performed with the help of this basic op-amp's.