Basic Electronics
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Module: 3 Field Effect Transistors
Lecture-8
Junction Field Effect Transistor (JFET) as an amplifier

In the last class we discussed about the JFET or the junction field effect transistor and we have seen the physical construction as well as the V-I characteristics of the device. In order to use it in a circuit we have to find out the small signal model and using this small signal model in the amplifier circuit we can then analyze and find out the voltage gain, input impedance, output impedance, etc. First of all we must know about the small signal model and for that let us first discuss about the transfer characteristic of the JFET. Transfer characteristic of the JFET means the characteristic between the drain to source current and gate to source voltage and here we are showing the V-I characteristic and the transfer characteristic side by side for easy understanding.

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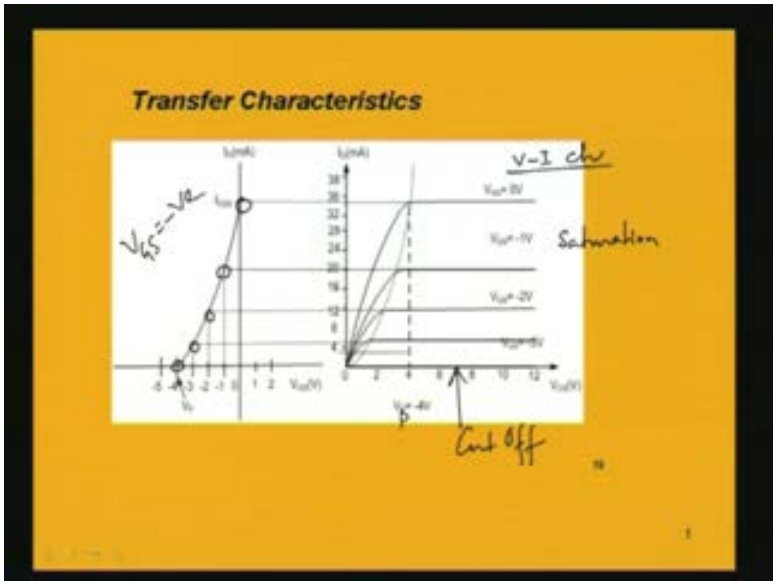

Here the V-I characteristic that is the characteristic between the drain current and the drain to source voltage, is shown for various values of the gate to source voltage. This is the V-I characteristic and from the V-I characteristic we can plot the transfer characteristic. This V-I characteristic is for various value of gate to source voltage from zero to negative because we cannot use gate to source voltage positive; we know that. There is no enhancement region in this JFET device. When gate to source voltage is zero, the corresponding saturation current in the drain is known as I_{DSS}. If we go on now increasing the gate to source voltage in the negative region that is we go on decreasing

the gate to source voltage from zero to -1 to -2 etc, then these are the different characteristics for the I_d and our important region is the saturation region. This region is saturation where we use the JFET as an amplifier and if we go on decreasing the GS, voltage between gate to source and reach the value which is known as the pinch-off voltage then your current in the drain is zero.

This is the cut off for this JFET and for a particular JFET we are considering this with the typical value of pinch-off as say -4 volt. This is the pinch-off voltage. At voltage below -4 volt between gate to source, the current is zero and at voltage between GS is equal to zero volt, we have this I_{DSS} as the saturation current. If we extend the current to the left or if we proceed this plots to the left and let it meet the ordinate from that particular gate to source voltage we get the corresponding points. That is for example when V_{GS} is equal to -1 volt, we have the saturation current of say 20 milliampere. If we extend this line to the left corresponding V_{GS} of -1 volt and this current of -20 will have this point. Similarly the points can be marked off with, the minimum point is -4 volt V_{GS} which is giving the zero drain current and the other maximum drain current is I_{DSS} which is at V_{GS} is equal to zero volt. You cannot go beyond this. You cannot increase V_{GS} in the positive direction. So the drain current is maximum at I_{DSS} and minimum at zero. In between if we mark 3 or 4 points and plot a curve through them, join these points and get a curve that is the transfer characteristic. The transfer characteristic is only in the region where V_{GS} is negative; not in the region where V_{GS} is positive.

We have earlier got small signal equivalent model for MOSFET. Now let us try to find out the small signal equivalent model for JFET.

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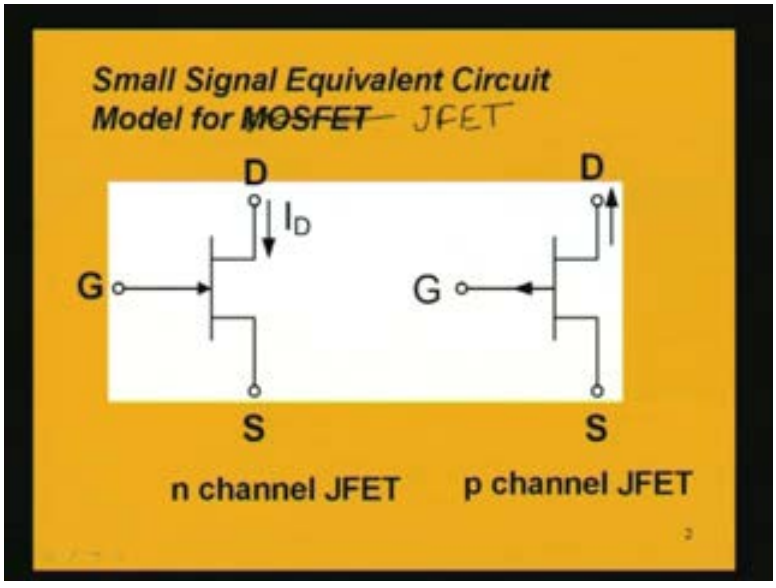

If we now focus on the symbol or symbolic representation of the JFET, here the three terminals gate, source and drain it is like the three terminals of the transistor BJT that we discussed earlier. Now we will have to fit in the small signal model which will represent the characteristic of the JFET device or the small signal model should reflect the behavior of the JFET device. From the characteristic curve between the I_D and V_{DS} which we have plotted here we see that I_D curves are almost horizontal. But in fact there is a little slope to the right; there is a little slope in the I_D curve to the right. The resistance between the drain and source is not exactly infinite but it is having a finite value, although this value is very high. That resistance let us name it small r small d and the drain to source current is given by current source. As we have seen in the earlier example of MOSFET it was g_m into V_{gs}.

Similarly if we now draw the small signal model it will be exactly same as the MOSFET device. But what is the g_m or the transconductance that we have to know.

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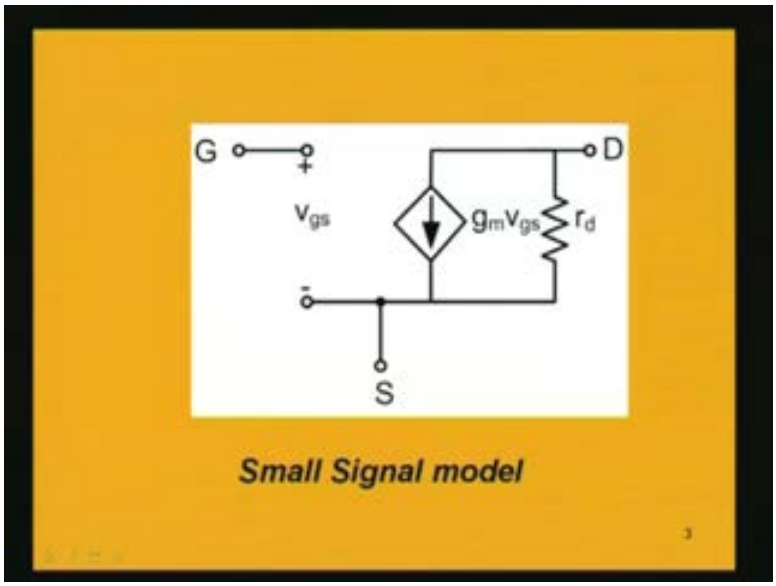

The transconductance is obtained from the transfer characteristic. It is actually del i_D by del V_{GS}. That is to be obtained or we can analytically or mathematically also proceed to find out this derivative which is nothing but di_D by dV_{GS} around the operating point. For a particular device under consideration if the operating point is given as say V_{GSQ}, I_{DQ} this is the operating point, means the voltage between gate to source at the operating point and the drain current is giving a particular point or operating point or it is called quiescent point. Around that operating point if we find out the slope of the transfer characteristic that is the characteristic between i_D and V_{GS} that is the g_m or transconductance. Here basically if we know the operating point, suppose the operating point is here say this is V_{GS}, this is I_D in the negative region only.

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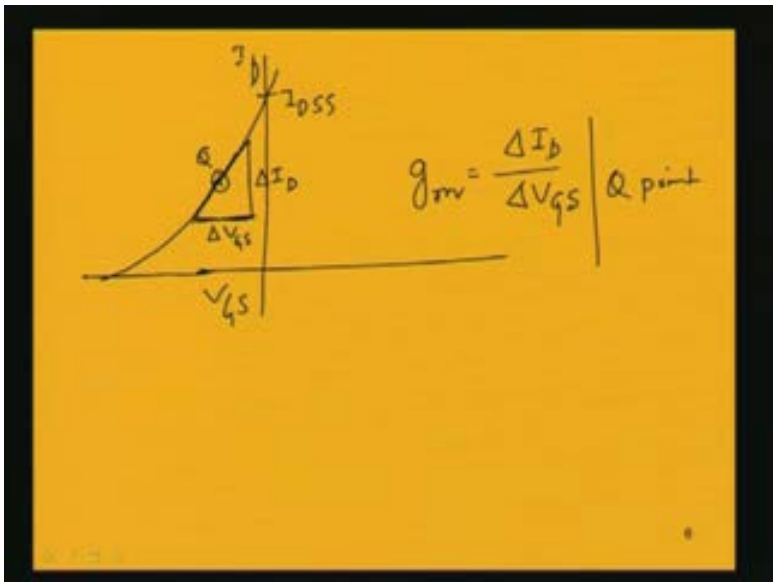

So it is like this. This is I_{DSS} and this is I_D zero. If this is the Q point, around the Q point we have to find out this slope. This is the small region around this Q point. You will have to find this del I_D by del V_{GS}. By changing the voltage between gate to source a little the corresponding change in the drain to source current that ratio between the del I_D and del V_{GS} around this operating point that will give you the transconductance. This is the transconductance around the operating point or at the operating point or Q point. That can also be found out analytically because we know the relation of the drain current with V_{GS}. What is that relation? That relation is i_D equal to i_{DSS} into 1 minus v_{GS} by v_P whole squared.

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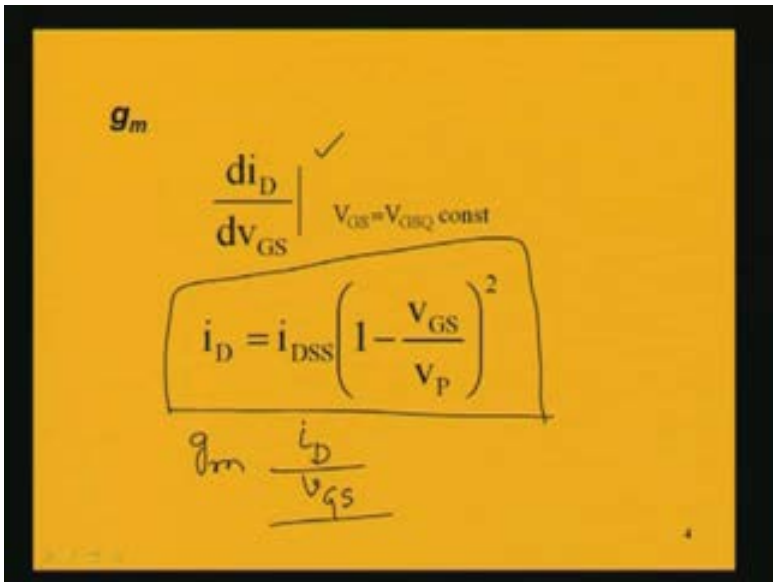

If we know the current relation we can find out the g_m from this di_D by dv_{GS} at the operating point or Q point. That means we will have to find the differential of the drain current with respect to the gate to source voltage and mind it this is the instantaneous value of drain current. We are now going towards the AC operation because we are using the JFET as an amplifier. All this discussion will consist of the instantaneous value of current and voltage because apart from the biasing voltage we are now applying a small signal and because of this both DC and AC, we will have the corresponding quantities in current and voltage as instantaneous values which is denoted by small i capital D small v capital GS. This is to be kept in mind. If we find out this derivative and find its value at the Q point or the operating point, that will give the transconductance.

What is the derivative of this i_D equal to i_{DSS} into 1 minus v_{GS} by v_P whole square? Find out the derivate of this i_D equal to i_{DSS} into 1 minus v_{GS} by v_P whole squared.

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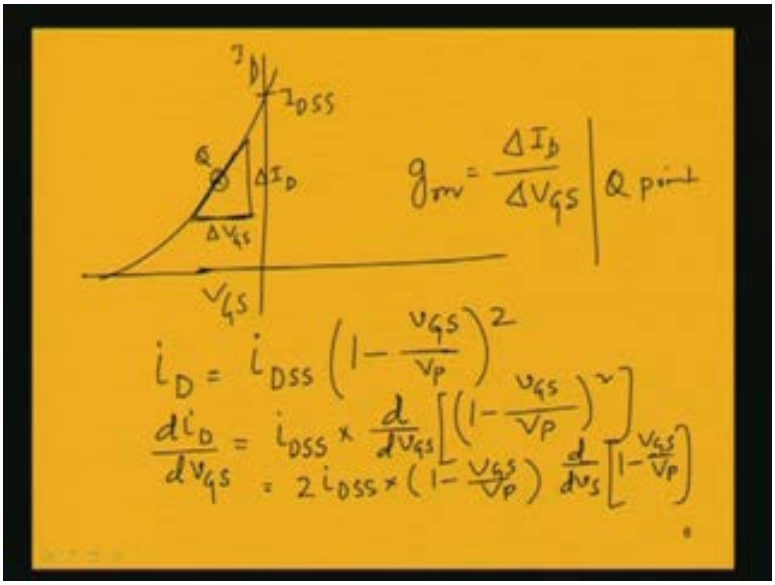

If we want to find its derivative with respect to v_{GS}, this is a constant term. The derivative of this term d_{iD} by dv_{GS} of this whole term. This 2 will come to i_{DSS}. Then the derivative of this whole term will give 2 into this will come into 1 minus v_{GS} by v_P. Derivative of this square term will give me 2 into this. Then derivative of dv_{GS} or this term 1 minus v_{GS} by v_P. It will be only -1 by v_P. We get 2 I_{DSS}. Basically this will be 2 I_{DSS} into 1 minus v_{GS} by v_P into minus 1 by v_P. But that has to be evaluated at the Q point and at the Q point we have the value of v_{GS} as V_{GSQ} and this I_{DSS} is a current which is the maximum drain current when v_{GS} is equal to zero. That value is a constant value we know from this specifications. It is written as capital I_{DSS} and at the Q point this will be simply capital V_{GS} by V_P.

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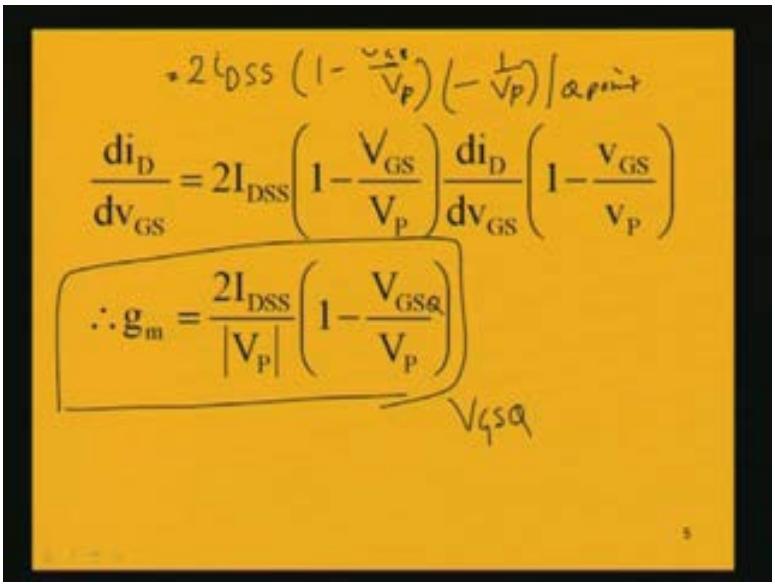

Finally we get 2 I_{DSS} by V_P with a minus sign; 1 minus V_{GS} by V_P. But as this transconductance will be positive we will use modulus of V_P term. Instead of writing V_P that is pinch-off voltage, we are writing a modulus. Because V_P will have a minus sign its modulus will be taken. This relation of this transconductance is important because from this relation if we know these values we can find out the transconductance of the device. If we know I_{DSS}, V_P and if the value of this V_{GS} that is the Q point V_{GS} is known, then we can know the transconductance. At the operating point we can write it as GSQ to make it clear that we are writing at the operating point. Once we know the transconductance we can fit it into the small signal model and draw the small signal model as we have drawn in the earlier cases of MOSFET.

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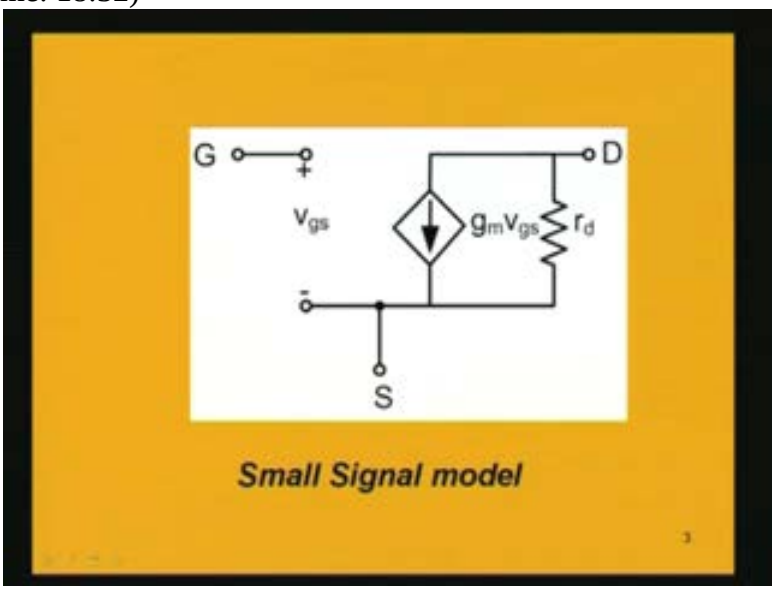

It is similar because the gate current is zero. High infinite input impedance, so gate current will be zero. Gate and source is like open circuit. This is the current source which is between drain and source. That is a current source which is given by gm vgs and this is the resistance between drain and source which is a high resistance value and conventionally the admittance between the drain and source is given in the data sheet or specification sheet. We will have to find out its reciprocal and that will be the resistance between the drain and source. This is as simple as that; we do not have a complicated small signal model. Now what will be done is that we will have to incorporate this small signal model into the amplifier.

JFET amplifier, as we discussed in MOSFET amplifier, will have a biasing scheme for properly choosing the Q point and then a small signal will be applied which we want to amplify without distortion. It should be small enough and then depending upon which configuration we are using for the amplifier we will have the corresponding network. Earlier we have found that we have three different configurations of MOSFET amplifier. Those are common source, common drain and common gate. Similarly in JFET also we have three configurations of amplifier which are common source, common drain and common gate. All these analysis are similar to the MOSFET amplifier that we earlier discussed. If we now consider the JFET as an amplifier say for example we will discuss common source JFET amplifier.

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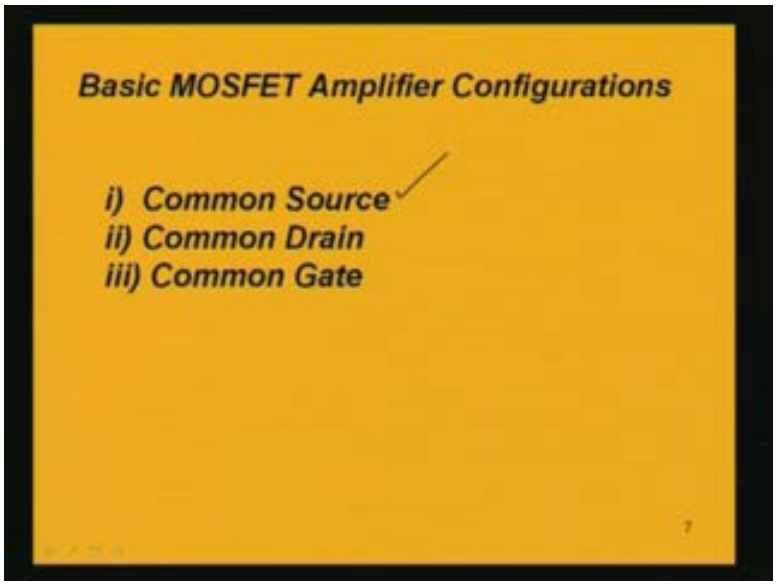

A common source JFET amplifier will have a biasing scheme and using a particular biasing scheme we use the amplifier.

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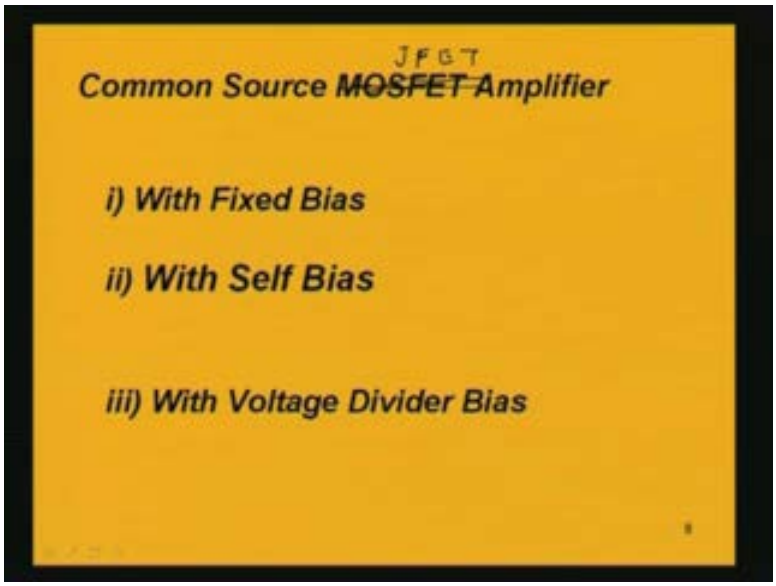

The common source JFET amplifier has fixed bias, self bias and voltage divider biasing schemes. As we are familiar with this biasing schemes which we also had in BJT amplifier that makes the study easier. But let us recall those biasing schemes that we have once used for BJT amplifier again. Let us discuss JFET amplifier biasing schemes briefly. Instead of going again into deriving all those parameters let us revisit those biasing schemes and quickly have a look into the use of these biasing schemes in the amplifier. Let us first discuss the fixed bias scheme for this JFET amplifier.

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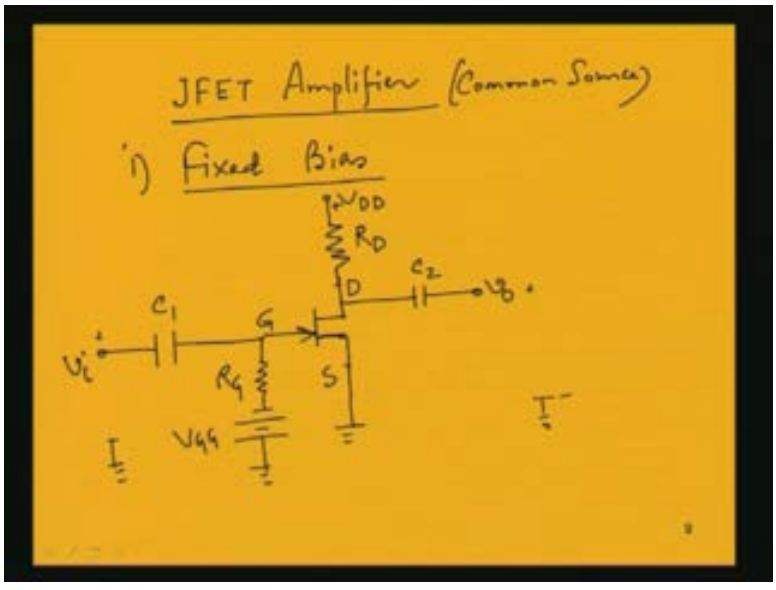

As the name suggests we have a fixed resistance and we are using common source JFET amplifier. Let us discuss common source JFET amplifier. The symbol for the JFET amplifier is like this. This is the gate, this is the drain and this is the source. For example we are taking an n-channel JFET. The direction of this arrow will convey the information whether it is n-channel or whether it is p-channel. Here it is an n-channel JFET device. We will have a biasing voltage and a resistance in the drain. This is say R_D, this is the drain terminal and this is the source terminal. This V_{DD} is positive. The source is grounded and in the gate we have a resistance R_G say to a negative voltage. Let us name it as V_{GG}. Basically this is the biasing scheme but we are considering an amplifier circuit. So we have to input a small signal and at the drain terminal we will get an output voltage which is also an AC signal. It will be in amplified form.

The input voltage is applied at a gate terminal through a coupling capacitor. The role of this capacitor is that it isolates the DC from the AC that is say C_1 and here we have another coupling capacitor C_2 and the drain terminal will have this output voltage say v_o. This is v_i. The polarities are shown as positive and negative lines. What will be the small signal model for this JFET device? That you can draw and and then we can draw the AC equivalent circuit for the whole amplifier.

If we recall the procedure for drawing the AC equivalent circuit the first step is that which make the DC sources zero, short circuit them. Second step, the capacitance has these values which are quite large. They are like short circuit path for AC. So short circuit those capacitances and then the resistances etc, which are by passed by the short circuited paths you simply remove them and then simplify the circuit. Following this procedure if we want to draw the AC equivalent circuit for this amplifier what we will do is we will make V_{DD}, V_{CC} zero. Then this capacitance will have a short circuit path. First let me draw the small signal model for the JFET.

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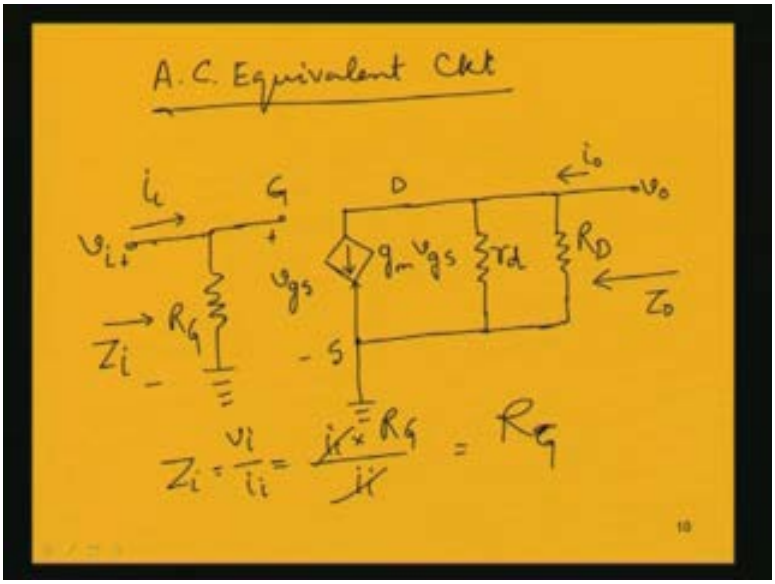

It will be $g_m v_{gs}$ between drain and source. This is the source. There will be r_d. This is the gate terminal. Between gate and source the small signal is v_{gs} and the drain and gate terminal will have the resistances R_G and R_D. This is grounded and this is also grounded. We have the input voltage here. This is the short circuit path through the coupling capacitor. This is v_i. This is v_o. This is the AC equivalent circuit for this network using the fixed biased scheme; fixed resistance is there R_G. If we want to find out all those parameters like input impedance we will look into the circuit at the input terminals. This is Z_i; this is your input current, this is the output current and the output resistance will be or impedance will be here looking into the device from the output terminals.

In order to find these out we follow the usual procedure. What will be the input impedance? This is nothing but v_i by i_i. The gate current is zero. The input current is nothing but this i_i which is flowing through R_G. What is this v_i? The voltage here at the input terminal is the voltage across this resistance R_G; i_i into R_G divided by i_i. The input impedance is R_G. For this fixed bias scheme, the input impedance is R_G. If we want to find out the output impedance, procedure is same. We have to make input voltage zero. If we make input voltage zero, v_{gs} is nothing but the v_i. So v_{gs} will also be zero. For finding out the output impedance, make v_i is equal to zero. Putting v_i is equal to zero means v_{gs} equal to v_i; that is also equal to zero.

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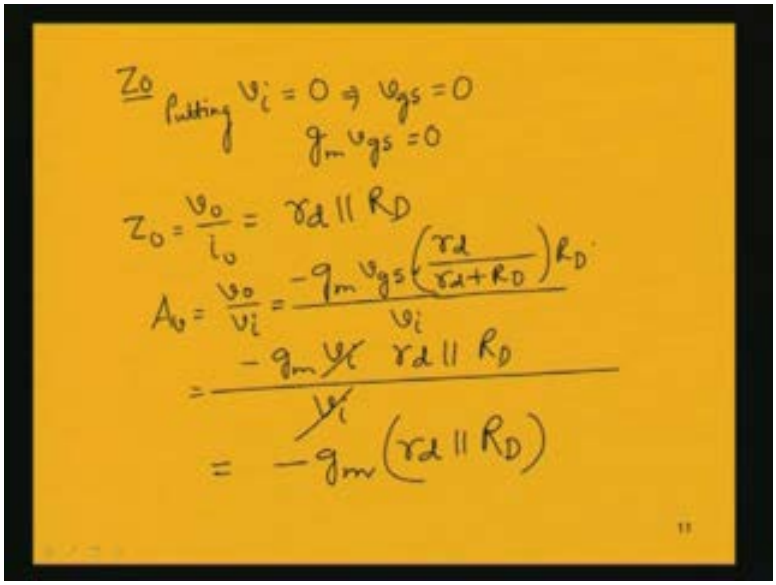

This current source $g_m v_{gs}$ will be equal to zero. This is zero means what? This is like open circuit. From the output side we have only two resistances which are in parallel; v_o by i_o. If we find out v_o by i_o that is equal to Z_O. What is v_o by i_o? That is nothing but the parallel resistance between these two R_D and r_d. That is equal to small r_d parallel capital R_D. That is obvious if you look from this circuit. This is just like open circuit and we have these two resistances in parallel. The voltage gain can be found out which is equal to v_o by v_i. Voltage gain is equal to v_o by v_i. Conventionally we are expressing the v_o as upper end is positive with respect to the lower end. But this current which flows through this r_d

is nothing but i_o because one part of this current flows through here, through small r_d and other part is through capital R_D which is nothing but i_o. This is actually i_o. This one is i_o. If we want to express that current by current division g_m v_{gs} into r_d by R_D plus capital R_D and multiply it by capital R_D with a minus sign; because your voltage v_o conventionally its upper end is positive but this current flow is from bottom to top. So, it is negative. This v_o is equal to minus g_m into v_{gs} into small r_d by small r_d plus capital R_D into capital R_D. This is the voltage drop v_o divided by v_i. But v_i is equal to v_{gs}. This input voltage is same as gate to source voltage. These two cancel out and this two is nothing but small r_d parallel capital R_D. What is this voltage gain? Minus g_m into small r_d parallel capital R_D. These are the parameters which we can find out from this AC equivalent circuit; for the fixed bias scheme we have shown. Similarly there is a JFET self bias scheme, JFET amplifier and we are discussing common source with self bias.

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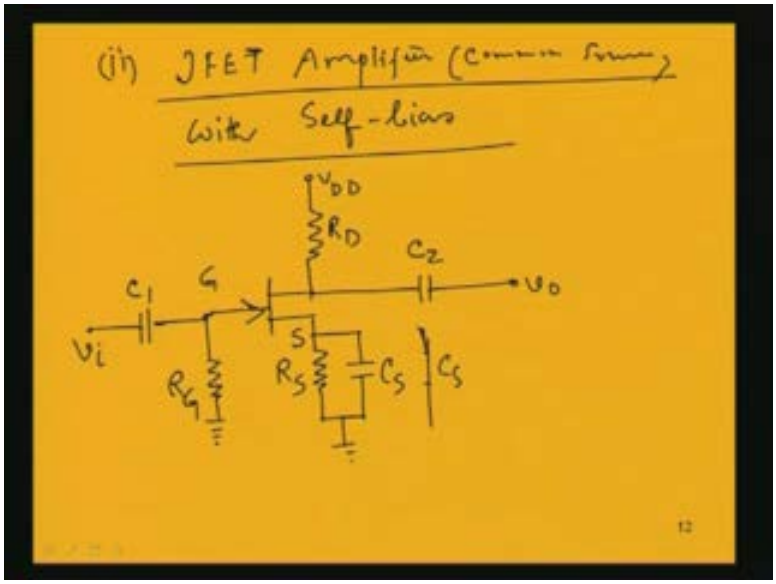

In BJT also we had self bias scheme and there the resistance was connected in the emitter and there was a bypass capacitor also. Even without bypass capacitor we may have a self bias scheme. Similarly here the resistance will be in the source. Analogous to that emitter in BJT we have the source here. Self biasing scheme will have the resistance connected in the source and we will have a bypass capacitor. In the circuit R_S is the self biasing resistor and this is the capacitance to the source resistance to the source. This is the source terminal and the rest is the V_{DD} having positive polarity through a resistance R_D. We are having this drain and the gate is having a resistance R_G. This is an n-channel and we have input voltage applied here.

In this scheme of self bias if we want to analyze drawing the equivalent circuit what we will do is we will follow the similar procedure and make the DC voltage zero, short circuit that capacitor. Next step after short circuiting the capacitor what happens is that this will be short circuiting path. This resistance C_S will have a short circuited path, so the resistance will be just bypassed. The current will take this path. This is the easiest path.

Because this is short circuited, the resistance will be avoided. This is simpler way. Because we do not have the resistance in the ammeter our circuit also becomes simpler. If we draw the AC equivalent circuit for this self biasing scheme, it will be like as shown here.

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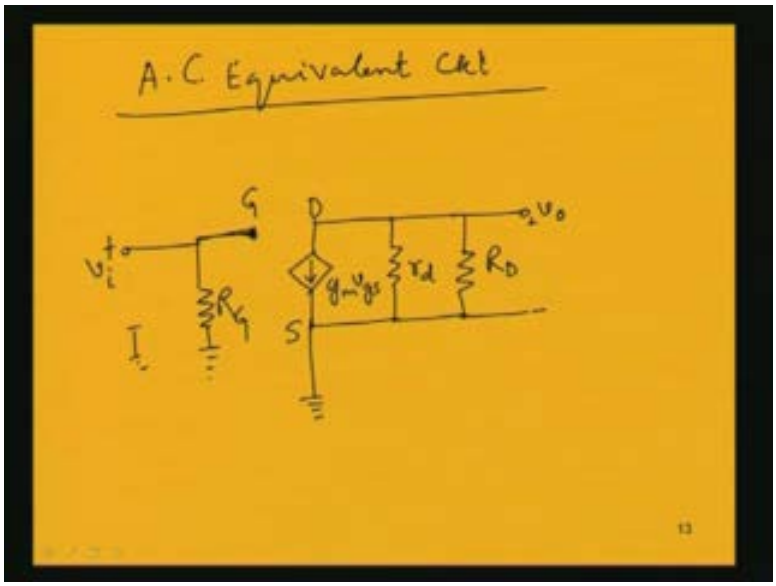

It will have the two resistances small r_d and capital R_D as it is and the source will have the path through the short circuited path by the capacitance which is short circuiting now. The resistance will be avoided. It will be simply grounded. It is a common source; source is grounded. It is a g_m v_{gs}. This is the gate terminal, this is the source terminal and in between gate and ground we have the R_G. We do not have a separate DC source here. Mind it in the gate we are not having the same source. V_{DD} is used for biasing and this is v_i. This is v_o, this is drain and this is the source. This is AC equivalent circuit for this self biasing scheme. Another popular biasing method is voltage divider biasing scheme. So let us consider JFET amplifier with voltage divider bias.

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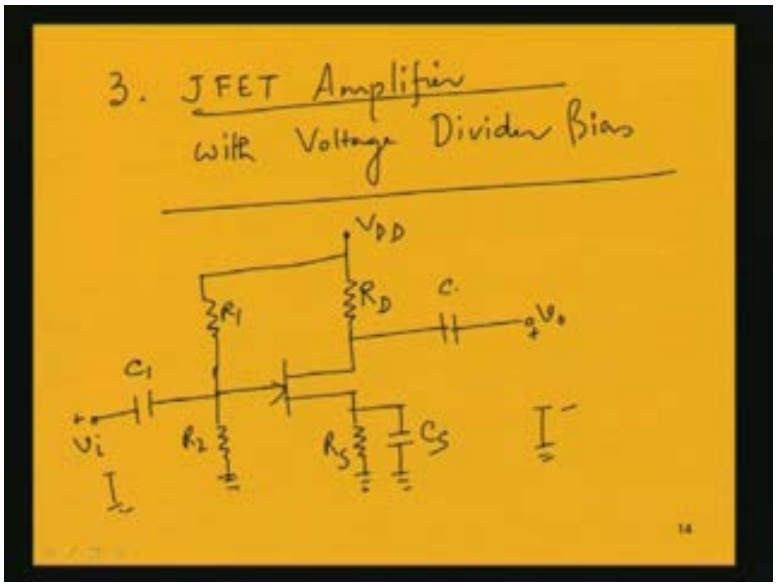

We have a voltage divider biasing scheme given by two resistances. Here will be one resistance to gate which is say R_1. Another will be there which is say R_2 and this is the source. Source is having the resistance R_S and the bypass capacitor is C_S. This is R_D V_{DD} and this is the coupling capacitor. We get the output voltage with the drain terminal v_o. This is the voltage divider biasing scheme. Now if we want to draw its equivalent circuit following the usual procedure we will have two resistances R_1 and R_2 which are connected to gate and the ground; two parallel resistances will be there R_1 and R_2. The AC equivalent circuit will have the small signal model as it is just the same.

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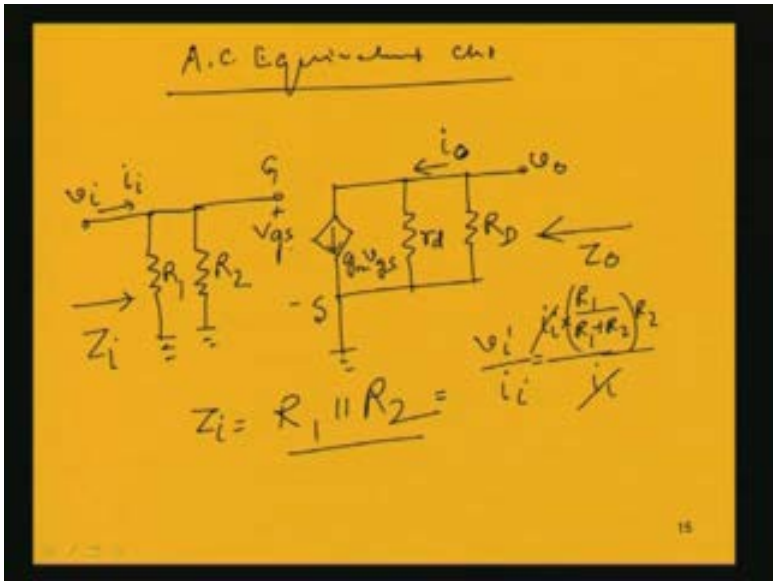

Right side is same small r_d capital R_D; g_m v_{gs}. This source is grounded. The gate terminal will have two parallel resistances R_1 and R_2 and this is the input voltage v_i. This is the gate to source voltage v_{gs} between gate to source. In this equivalent circuit we can find out the parameters like input impedance, output impedance, voltage gain, etc. In order to find out input impedance it is very simple because we have two resistances R_1 and R_2 parallel at the gate terminal. So it is simply R_1 parallel R_2. You can derive it following the usual procedure like v_i by i_i where i_i is this current. i_{io} is this current and mind it we are not showing till now any source resistance and load resistance. If they are there then we will have to include them also in the circuit. v_i by i_i if we do, the voltage across R_2 is the same voltage across R_1 in whatever manner you take. By current division it will be i_i into R_1 by R_1 plus R_2 into R_2 by i_i. We get R_1 parallel R_2.

Now the output impedance; make input voltage zero.

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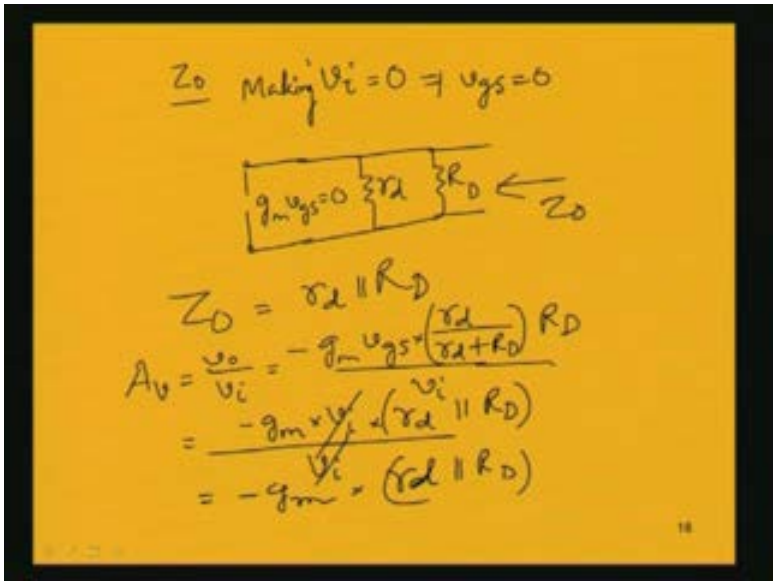

Then the circuit will be like this. We have two resistances. g_m v_{gs} will be equal to zero; because v_i is equal to zero means v_{gs} is also equal to zero. We have only two resistances which are in parallel small r_d parallel capital R_D and if we look from the output terminal what we will get? It is small r_d parallel capital R_D only. This is the output impedance. Similarly voltage gain if we find out, the voltage gain is v_o by v_i. Find out v_o. This is positive and negative conventionally. i_o current which is this one, this is i_o, the current flowing through this capital R capital D is equal to this current source multiplied by R_D by small r_d plus capital R_D because the current division law has to be applied. That current multiplied by this resistance gives you the voltage but in a negative way because current is flowing from bottom to top. Our voltage v_o is having top positive with respect to bottom. So minus sign will be there. g_m into v_{gs} into small r_d by small r_d plus capital R_D into R_D by v_i; v_{gs} is equal to v_i and this two parallel combination small r_d parallel capital R_D. Finally we get the voltage gain as minus g_m into small r_d parallel capital R_D. The minus sign is significant because it conveys information of phase reversal. The output

voltage is 180 degree out of phase with the input voltage like in common emitter amplifier that we observed in BJT. Common source is analogous to common emitter amplifier characteristics and other types of configurations which we have are common drain and common gate.

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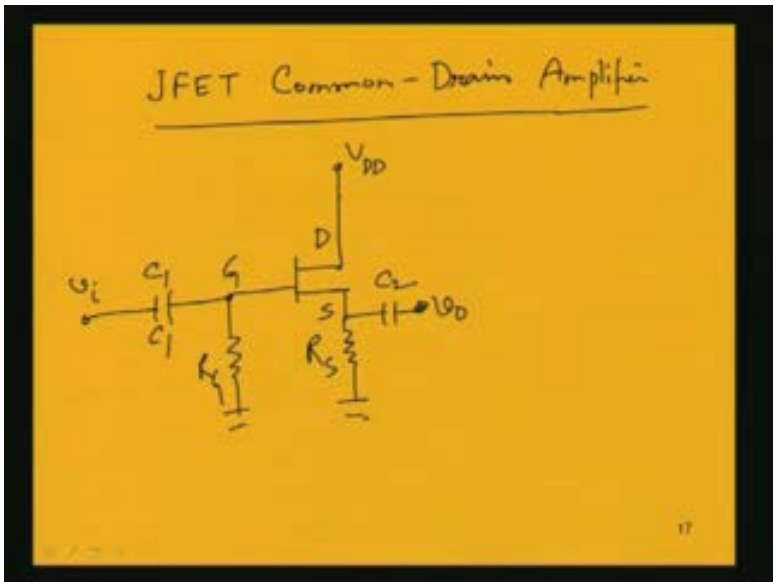

Common drain amplifier is also known as source follower because the voltage you obtain across the resistance at the source. The common drain means drain terminal will be grounded in the AC equivalent circuit. That is why it is the common drain. In JFET common drain amplifier, if we see the circuit of the common drain, the drain will be directly connected to V_{DD}. But the source will have a resistance R_S. This is the source, this is the drain, this is the gate and gate is having a resistance R_G and this is the coupling capacitor. This is the input voltage. This is absent here because we get the voltage across the resistance at the source. This is v_o. In between there will be a coupling capacitor. This is like this. One important thing to notice here is that we have the voltage across this source resistance, not across the drain terminal that we had earlier in common source. This is the common n-channel. If we want to draw this AC equivalent circuit for this common drain amplifier, this is the current source between drain and source. g_m v_{gs}, r_d will be there, small r_d.

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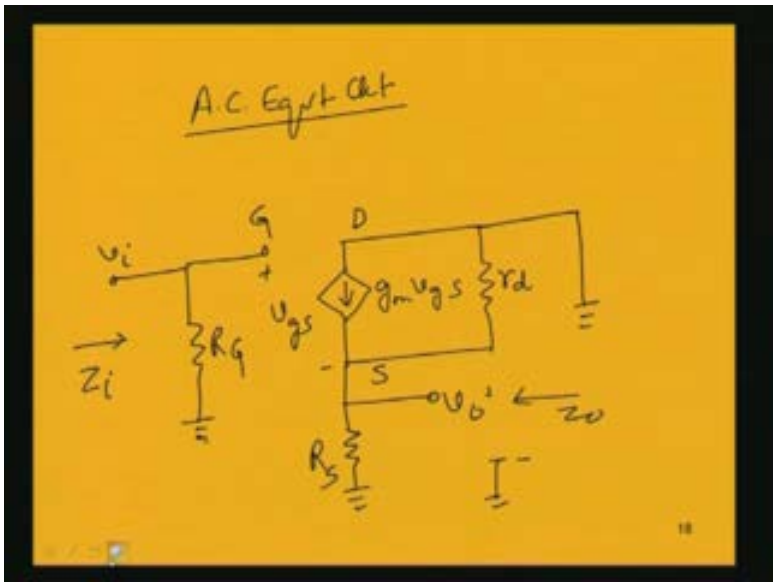

Capital R_D is not there. Drain is directly grounded. This is drain and this is source. This drain terminal is directly grounded; that is the important feature for this common drain amplifier and this is the gate terminal and source terminal is having the resistance R_S. We get the voltage across this resistance R_S, v_o. The gate terminal is having a resistance R_G and this is the input voltage. This is the voltage between gate and source which is v_{gs}. This is the AC equivalent circuit for the common drain amplifier. In this AC equivalent circuit you can try this; find out the Z_i, Z_O, A_V, etc. Let us also take the JFET common gate amplifier configuration.

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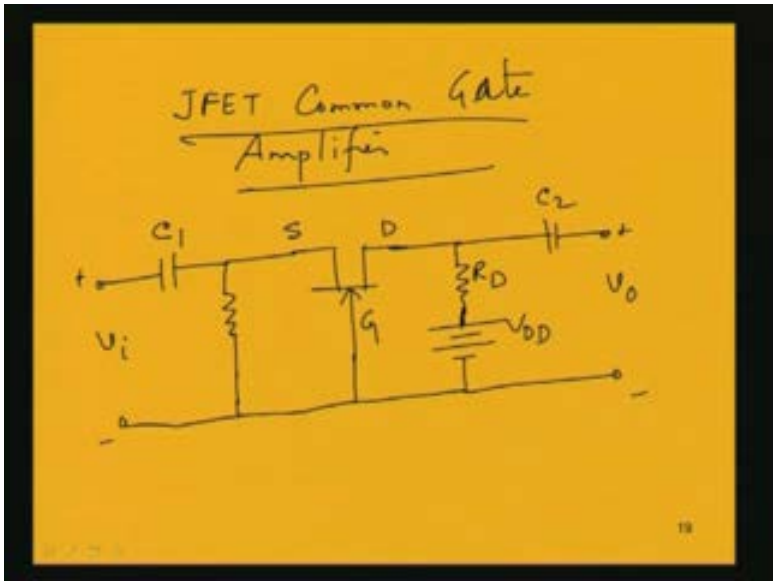

Common drain is similar to the emitter follower or common collector in the BJT and common gate is similar to common base amplifier in BJT. As the name suggests common gate means gate terminal will be grounded. This is gate, this is source and this is drain. We have the drain, R_D resistance and positive voltage V_{DD}. The gate is common between the two input and output circuits. A simple circuit is shown here. The voltage will be obtained here from the drain terminal. So this is common gate. If we now draw the AC equivalent circuit for this common gate amplifier we see that this is source, drain and gate. Gate is grounded so gate will be grounded.

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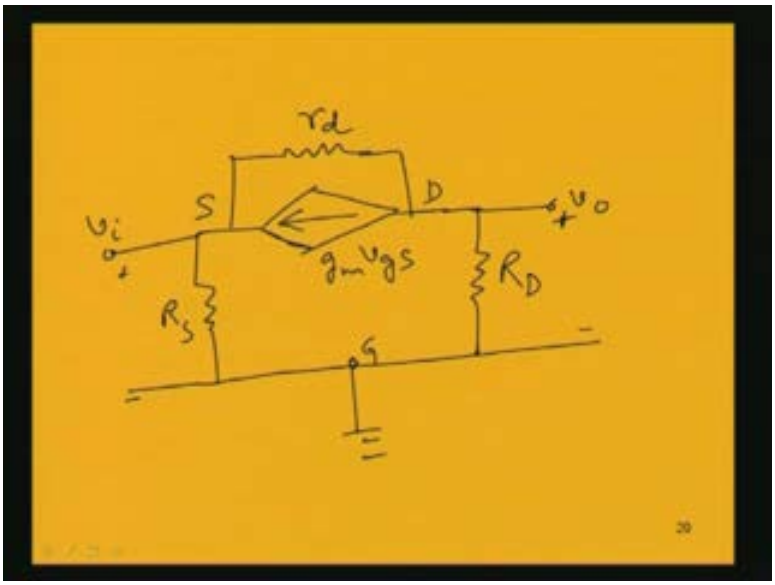

The current source is from drain to source which is g_m v_{gs} and the resistance r small d will be from drain to source. Drain will have this R_D and source will have this R_S and the gate will be grounded like this and we have this v_i; this is v_o. Here we can see that this R_D, the resistance will be between drain and source. For example if we take a fixed bias circuit as shown here we have V_{DD} is equal to say 20 volt, R_D equal to say 2 kilo ohm.

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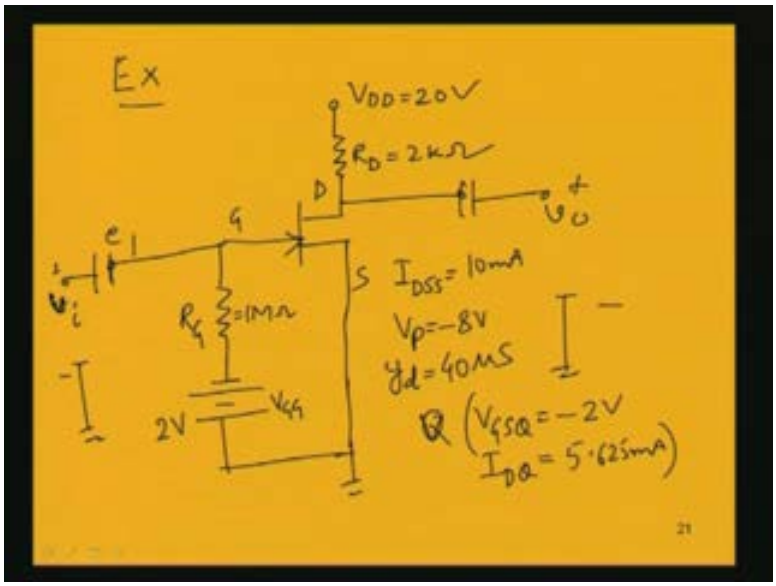

This is drain terminal, gate terminal and source terminal. It is n-channel. We have R_G equal to 1 mega ohm. This is the gate to source V_{GG} voltage 2 volt and voltages through this coupling capacitor are obtained here. Input voltage is given through another coupling capacitor C_1. This is the v_i. This is the fixed bias scheme JFET amplifier. You are given that Q point is given as V_{GSQ} equal to -2 volt, I_{DQ}; these are the Q point gate to source voltage current and drain current 5.625 milliampere and also given that the I_{DSS} equal to 10 milliampere. Then the pinch-off voltage is -8 volt and the drain to source admittance is 40 micro Siemens. These are given in the specification sheet and you are operating this JFET amplifier at this operating point. Now you have to find the transconductance, r_d, Z_i, Z_O and A_v.

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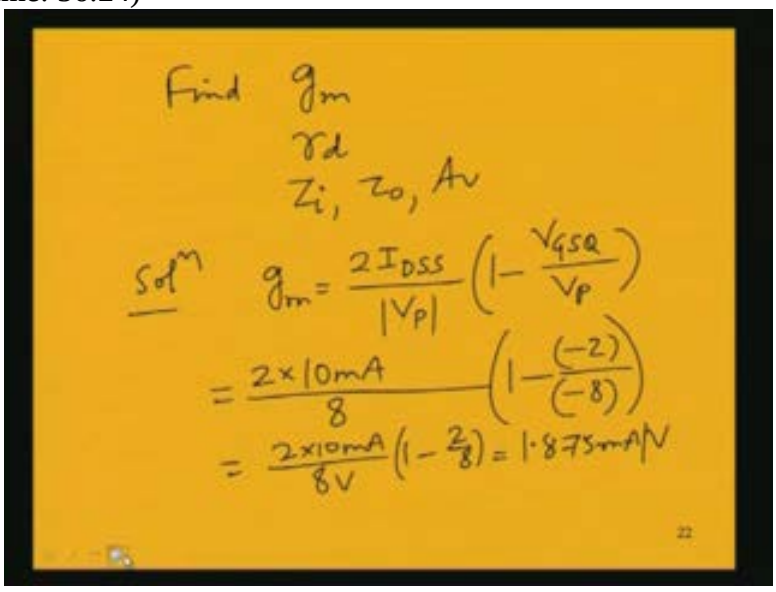

How to solve this problem? We have to find out g_m. g_m we know is equal to 2 I_{DSS} by magnitude of the pinch-off voltage into 1 minus V_{GSQ}, at the operating point gate to source voltage, by pinch-off voltage. By substituting these values I_{DSS} is given as 10 milliampere; pinch-off voltage is given as -8 volt. We will take the magnitude of the pinch-off voltage which is 8 volt and within the bracketed term V_{GSQ} that is the gate to source voltage for the operating point is given as -2 volt and the pinch-off voltage is -8 volt. As it is, it will be replaced with their polarities. Now what we get? 2 into 10 milliampere here both are in volt; 1 minus 2 by 8. If you calculate this it will come to, you check the value, 1.875 milliampere per volt because this is milliampere, this is volt and this has no unit. The unit volt to volt cancel; so it is equal to 1.875 milliampere per volt.

What is small r_d? It is the reciprocal of y_d.

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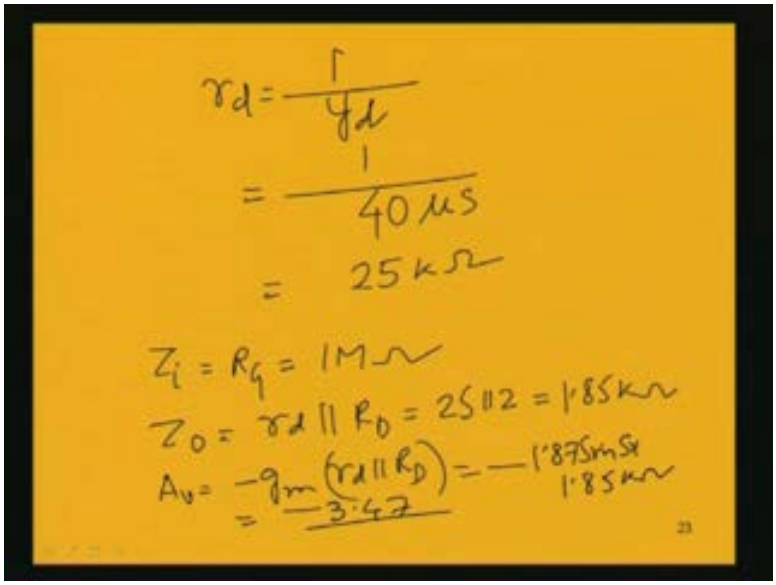

y_d we know. What is given? 40 micro Siemens. If we find out this value 1 by 40 is equal to 25 and unit will be kilo ohm because it is 10 to the power -6 and Siemens means ampere per volt. The reciprocal will give you volt per ampere and 10 to the power -6 will go up which will be 10 to the power 6, so 25 kilo ohm or 0.025 mega ohm, you will get. Similarly we can derive the input impedance from the small signal model or if we already know the input impedance because R_G we have found out. We can also proceed from the small signal model then you do not have to remember. You derive it from the small signal model by following the first principles. Then you will find that Z_i is equal to R_G and that is equal to 1 mega ohm and output impedance is small r_d parallel capital R_D means 25 parallel 2. Both are in kilo ohms. That gives you 1.85 kilo ohm and lastly voltage gain is minus g_m small r_d parallel capital R_D. Minus gm we have found out to be 1.875 and that is micro Siemens into 1.85 kilo ohm. That gives you -3.47 with a minus sign. That is the voltage gain. In this way we can solve these examples. If we proceed by drawing the AC equivalent network incorporating the small signal model, we can derive all the

parameters easily by following the first principle. Suppose we are to get voltage gain v_o by v_i, then we will have to find what is v_o? So in that way we can find out.

This discussion today helped us to know about the application of the junction field effect transistor which is a type of field effect transistor only and we have seen how the different biasing schemes can be used for designing the amplifier and three configurations we have discussed: the common source, common drain and common gate configurations just as in the case of BJT amplifier that we discussed earlier. Using the small signal model which is the same for the FET device that we have discussed so far be it MOSFET or be it JFET the small signal model is same. Only the transconductance computation will be a little different in JFET and by this small signal model incorporating the small signal model in the AC equivalent circuit for the amplifier we have found out all the parameters which are our interest in the amplifier.