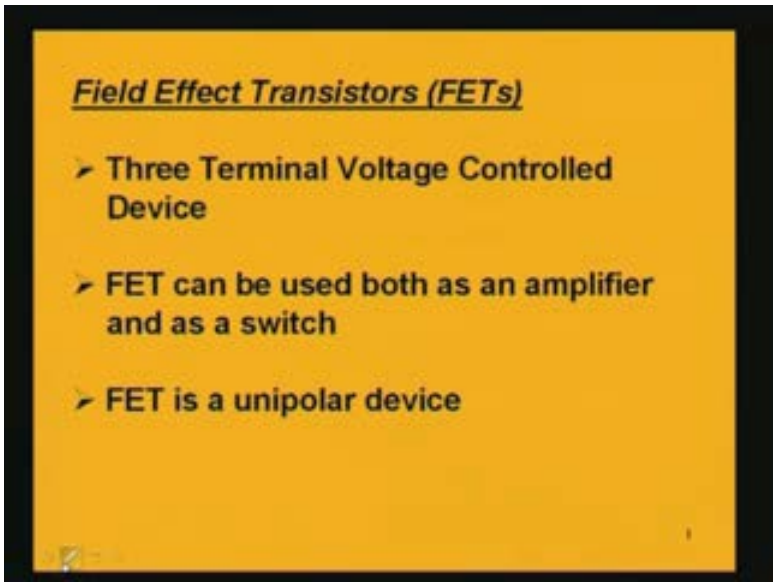
Basic Electronics
Prof. Dr. Chitralekha Mahanta
Department of Electronics and Communication Engineering
Indian Institute of Technology, Guwahati

Module: 3 Field Effect Transistors
Lecture-1
Metal Oxide Semiconductor Field Effect

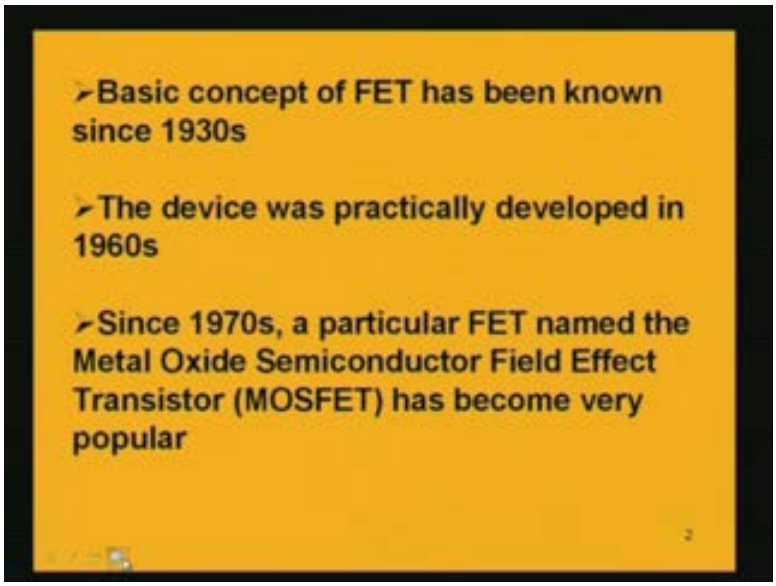
Today we will discuss about a different type of transistor which is known as field effect transistor. Earlier we discussed about BJT or bipolar junction transistor but today we will discuss a different type of transistor which is different from the BJT and this is FET. In short it is known as FET and its full form is field effect transistor. The field effect transistor is also a three terminal device and it is a voltage controlled device. Transistor, we have earlier seen that, is a current controlled device but the FET is a device which is voltage controlled and like a BJT the FET also can be used as an amplifier and as a switch and one important difference from BJT is that the FET is a unipolar device. Here the charge carrier is one type; either it is holes or the electrons.

(Refer Slide Time: 2:36)



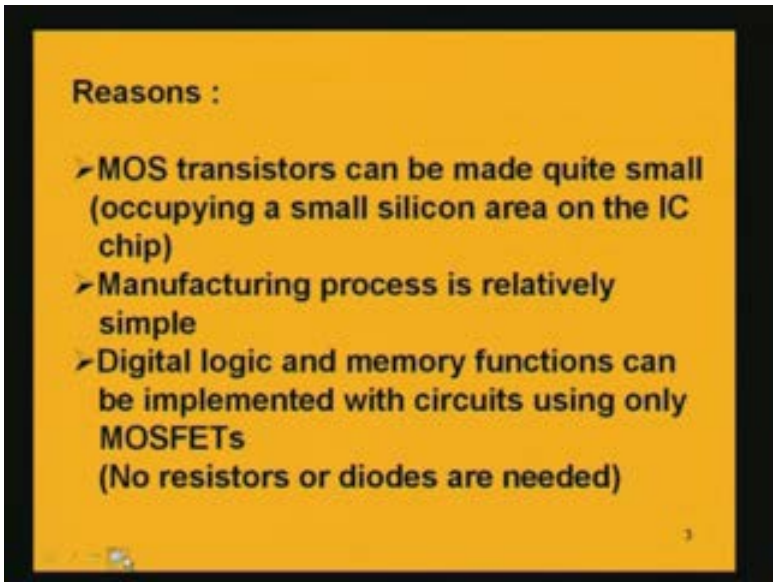
But in BJT we have seen there are two types of charge carriers. It is a bipolar device. The FET has been actually known since 1930's. The basic concept of the FET was developed in the 1930's but practically this device was developed in 1960's.

(Refer Slide Time: 3:02)



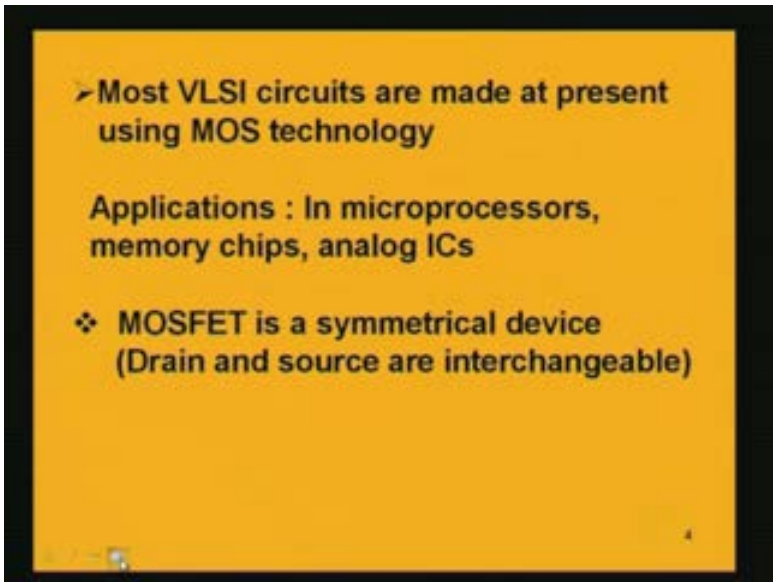
But since 1970's, a particular type of FET which is known as metal oxide semiconductor field effect transistor or in short known as MOSFET has been existing in a very popular way. Since 1970's onward this particular type of FET which is the MOSFET has been used immensely and ultimately nowadays we find its application in VLSI circuits, very large scale integration circuits where you can assemble hundreds and thousands of circuits in IC. We find the application of MOSFET tremendously and there are reasons for this ever growing popularity of the MOSFET. The first reason is the size.

(Refer Slide Time: 4:12)



The MOSFET transistors can be made quite small and basically it occupies a very small silicon area on the IC chip. As it can be made on a very, very small area it helps in reducing the size of the chip, so we can have a number of the transistors on a small area of the IC. This is one big advantage of designing smaller and smaller area devices which is nowadays very popular. It finds its application and from that point of view it is very popular. Another reason for growing use of the MOSFET is that its manufacturing process is also simple. Another important factor which contributes to the use of MOSFET is that the digital logic and the memory functions can be implemented with circuits using only MOSFETs and no resistors or diodes are needed. We can do away with the resistors and diodes and we can build the digital logic as well as the memory functions using only MOSFETs. These are the reasons for the tremendous use of MOSFET in ICs nowadays. That is why most of the VLSI circuits at present are using MOS technology and we see applications of MOSFETs in microprocessors, memory chips, analog ICs as well as integrated circuits using both analog and digital ICs.

(Refer Slide Time: 6:30)

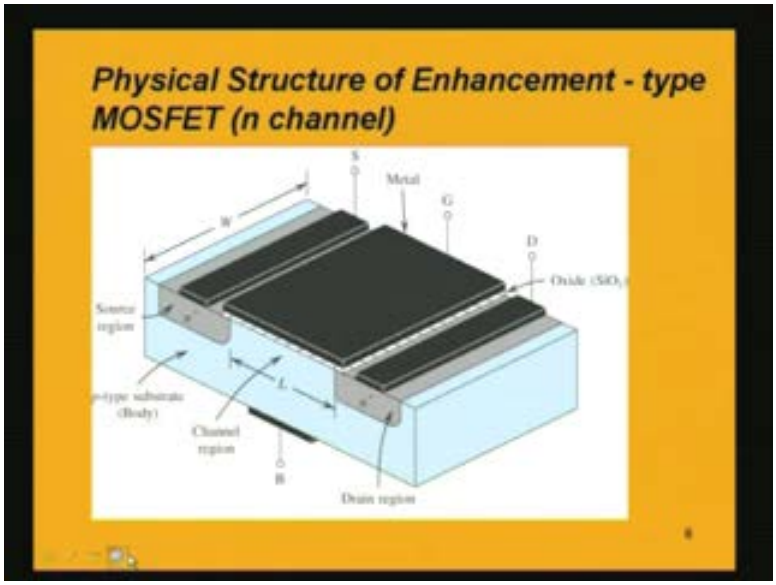


It is a symmetrical device. The MOSFET is a symmetrical device unlike BJT. In BJT we have noted that the emitter, base, collector regions are not symmetrical. That means we cannot interchangeably use an emitter and collector but that is not so in MOSFET. In MOSFET the two regions which are the drain and source, as we will find later on, can be interchangeably used and so it is a symmetrical device. Now we will discuss about the different types of MOSFET. First let us take up the enhancement type of MOSFET that is most widely used FET.

(Refer Slide Time: 7:35)

We will first discuss about the enhancement type MOSFET and then we will also discuss about the depletion type MOSFET and the junction FET. Let us first see the physical structure of an enhancement type of MOSFET and we will first take up the n channel MOSFET.

(Refer Slide Time: 8:04)



There are two types of enhancement type of MOSFET which are n channel and p channel. We will first discuss about n channel enhancement type MOSFET. Here we see the structure of an enhancement type of MOSFET which is n channel. Here as we see there is a p-type of substrate which is the body of the MOSFET and there are two n

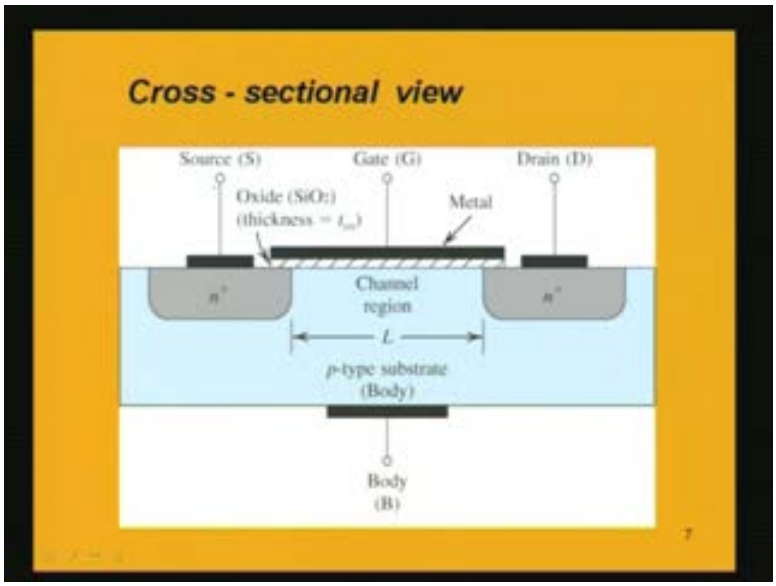
regions. Here they are shown as n plus and n plus. This plus is to mean that it is a heavily doped n region and we will use minus for lightly doped n region. These two n plus regions as shown in this block are two n-type doping materials. These are two n-type materials and the p-type and n-type semiconductors both are grown on a single crystal silicon wafer. Here actually the p substrate and the two n-type materials, these are n-type semiconductors. These are grown on the silicon wafer and as you see here there is a silicon dioxide layer which is grown between the two n-type semiconductors. We have an insulating material which is the silicon dioxide and this insulating material is there between the two n-type semiconductors and on this insulator there is the metallic contact which is the gate terminal.

As you can see here there is a gate terminal which is the terminal taken up from this metallic contact which is grown over this silicon dioxide. There are other metallic contacts over these two n-type semiconductors. These two n-type semiconductors are known as the source and the drain. We have another metallic contact over the source region as well as over the drain region and the two terminals which are taken out from this source and drain regions metal contacts are the source terminal and the drain terminal. There is another terminal shown from the body or the substrate which is shown here as B. B is for the body terminal and basically at this point we have four terminals but ultimately we will observe that this body terminal is connected to source terminal generally and finally we will have three terminals only. These are gate terminal, the source terminal and the drain terminal.

Here in between the two n-type of semiconductors which are source and the drain, we are denoting this length as capital L. Basically this L is denoting the length of the channel. We will study what a channel is? There is another term which is width of the channel and it is denoted by W. It means the width of this whole channel. In this diagram physically there are 3 regions. One is the p-type, the other two are the n-type regions. These are the main regions in the MOSFET and these two regions which are source and drain regions these are interchangeable as I have already mentioned. So this device is a symmetric device. We can use the source and the drain interchangeably. There is no particular region which should be source or the other should be drain.

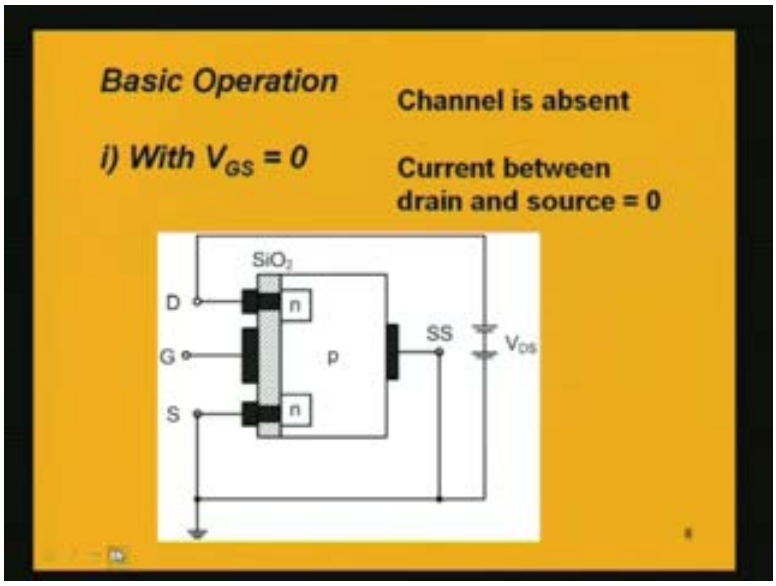
We now see the cross sectional view of this whole construction. We have this type of diagram where we have this p-type substrate having a body terminal taken out and the two n-type of semiconductors and in between these two n-type semiconductors is the p-type substrate and on this region between the two n-type semiconductors is grown the insulating material which is silicon dioxide as shown here and on the top of this silicon dioxide we will have the metallic contact which is the gate terminal. As shown here the gate terminal is taken out from this metallic contact which is grown over the top of the silicon dioxide and similarly in the two n-type regions which are the source and the drain we are having the two metallic contacts out of which the two terminals source and the drain are taken out.

(Refer Slide Time: 15:28)



So we have now the three important terminals gate, source and drain. This body terminal is just optional. That means we generally connect the body terminal to the source but here we are just showing all the four terminals. This is the cross sectional view and this oxide layer that is the layer of the silicon dioxide has a thickness which is denoted by t_{ox}. t subscript ox means it is the thickness of the oxide material. Let us go into the basic operation of this MOSFET.

(Refer Slide Time: 16:20)



It is an enhancement type MOSFET. Why it is called an enhancement type of MOSFET? We are redrawing the MOSFET here just simplifying the drawing by indicating the p-

type substrate and two n-type semiconductors which are the source and the drain. Here this is the drain, this is the source and we have these three metallic contacts. Out of these three metallic contacts we have three terminals drain, gate and source. You have notice here that this metallic contact from the drain is contacting to this n-type semiconductor. This is the drain. This is the source, so this metallic contact is contacting with the source and in the gate terminal which is having this metallic contact, we can notice that, there is no contact from the metallic contact of the gate terminal to the p substrate because in between there is this insulator. The insulator is the silicon dioxide which is in between the gate terminal and the p-type substrate. This region is having this insulator in between and we have this substrate terminal, SS for substrate, which is the p-type. It is p-type substrate. We have the substrate terminal or body terminal as earlier we have denoted it as the body terminal. This is the same thing, the substrate or the body terminal. Here this is connected with the source. Basically we have these three terminals.

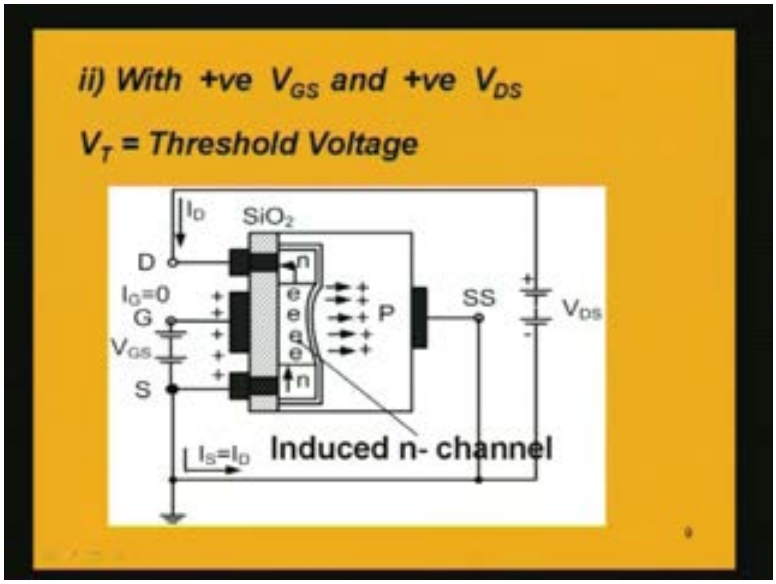
Let us have V_{GS} zero. That means we are not applying any voltage between the gate and source. We are keeping it open but we are having a voltage V_{DS}. Between the drain and the source a positive voltage is applied. Let us study what will happen if we have this type of arrangement. You have noted that these two regions are semiconductors which are rich in electrons. These n-type materials are rich in electrons. They are having the carriers which are electrons, so they have high concentrations of electrons. But we also have to note that in between these two n-types there is no channel although these two regions are rich in electrons. But still at this present arrangement there cannot be any current flow between this drain and the source because there is no channel present.

Although there is a voltage being applied which is V_{DS} what does this voltage do? Basically this is a voltage which is making the two pn junctions reverse biased. If we notice this junction between the p-type substrate and this drain which is an n-type semiconductor this is nothing but a reverse biased pn junction. That will have high resistance, so there will not be any flow of current. Since this pn junction is also reverse biased, these two back to back pn diodes are basically having reverse biasing junctions. From this end to this end through this p if we travel we have np and again pn. Both these diodes are reverse biased, so we will not have any flow of charge carriers or we will have zero current. There will not be any flow of current from the drain to the source. Under this condition that the voltage from gate to source is zero V_{GS} is zero and although there is a voltage which is positive between drain and source this does not help in establishing any channel between these two n-type semiconductors. That is in between drain and source there is still no existence of any channel, so channel is absent between these two n-type semiconductors and that is why there is no current flow or zero current at this stage.

Next let us see what happens when we apply a voltage between the gate and source and that voltage is positive. Now we have positive voltages between the gate and the source and the drain and the source. Both have positive voltages. That we are showing here by this V_{GS} having a source which is having positive to gate. That means with respect to source it is positive. So between gate and source we have a positive potential and

similarly from drain to source we have this V_{DS} that is also positive and typically this substrate terminal is connected to the source terminal. Now what happens?

(Refer Slide Time: 23:22)



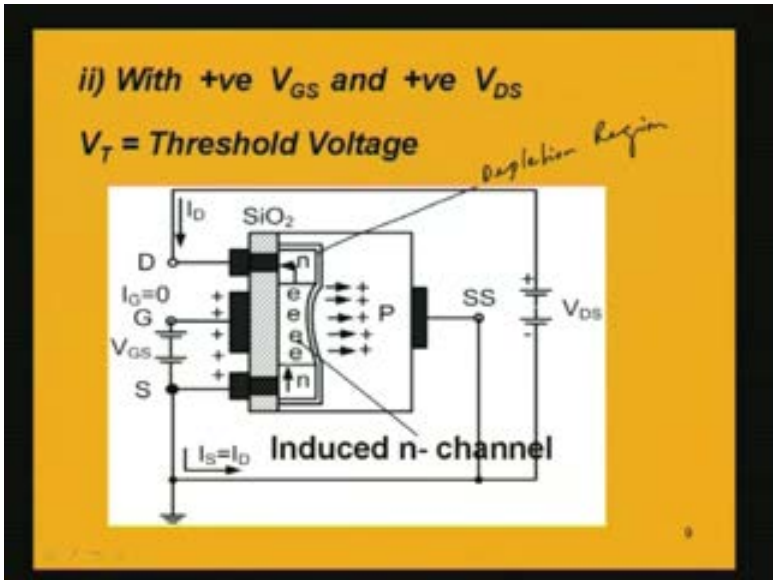
As there is this voltage between gate and source which is positive, this positive terminal will repel the majority charge carriers in the p-type of semiconductor. This positive potential at the gate terminal will repel the positive charges or the holes in the p-type of the substrate. In the p substrate the majority carriers are holes and the minority carriers are electrons. It is a p-type semiconductor. As we have a voltage which is positive at the gate terminal, they will repel these positive charges deep inside the substrate. That means it will repel to the right. It will be pushed deep into the p-type substrate and the electrons which are the minority carriers will be attracted by this positive terminal of the gate. So they will come to left and they will accumulate near the insulator, silicon dioxide. They will crowd just near to the insulating material which is present.

As the majority carriers which are holes are pushed deep into the p-type substrate away from the insulator, around this insulator their will be a depletion region because in this region the acceptor ions will be just surfaced out which are the immobile charges. If you recall in a p-type of semiconductor the holes are the majority carriers and here as these holes are being pushed away they will uncover the immobile charges which are nothing but the acceptor ions which are negative ions. That means there will be a depletion region near to this region from where they are pushed away. The holes are pushed away. This is denoted by this region that is the depletion region.

Here basically what will happen is that the holes are not there, so there will be uncovering of the immobile charges. This is the depletion region. The electrons which are attracted by this positive terminal will come towards the insulator material and what will happen now is that because of the presence of these electrons in the length between the

two n-type semiconductors. There is now an induced n channel. An n channel is induced. n channel means the channel having the negative charges or electrons.

(Refer Slide Time: 27:13)



What we are having now is that in between the two n-type semiconductors which are the drain and the source we are having now induced n channel because of the presence of the electrons which are attracted by the positive gate voltage which are the minority carriers of the p-type substrate. If the V_{GS} is having a magnitude enough to sustain the flow of the electrons from this source to drain then the current will start flowing and the voltage value of V_{GS} after which or above which the current starts flowing that voltage is known as the threshold voltage V_T. V_T is a specific voltage which is having typical value for a particular MOSFET. If we have V_T is equal to 2 volt that means that MOSFET has a threshold voltage of 2 volt. That is the gate to source voltage must be at least 2 volt positive if we are considering n channel after which only the current will start flowing.

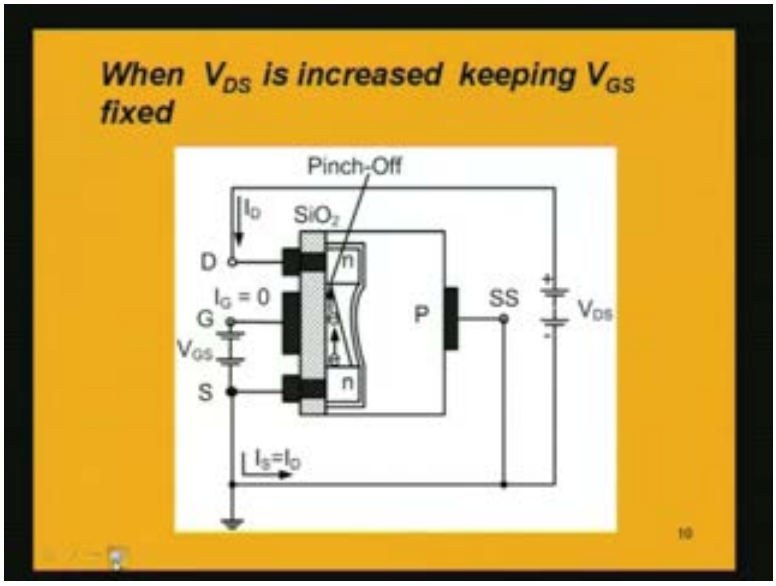
Up to V_T if V_S is less than V_T then there are will be no current flow from drain to source. Why current will flow from drain to source is because it is having a positive potential. As we observe here we are having V_{DS} which is a positive potential. These electrons will start to travel from the source through the channel to the drain and they will flow through this lead to the V_{DS} positive potential and the traditional or classical direction of current will be from drain to source and that current is I_B. I_B is flowing because of the existence of this induced n channel in between the two n-type semiconductors which are the source and the drain and this current will now flow through the source and the drain current is equal to source current; I_S equal to I_D and we also notice that I_G is equal to zero.

Although there is a voltage between gate and source, the current at the gate terminal I_G is zero because we have seen here that there is a layer of insulating material between the gate terminal and the substrate. Although electrons are now induced in the n channel these electrons will crowd near this insulator but they cannot come to the gate terminal.

They cannot be brought by attracting them to the gate terminal because there is an insulating material in between. These electrons will not reach this gate terminal. They cannot complete the travel through this insulting material, so there will be no gate current. The current which is entering into this MOSFET will be leaving this MOSFET also, so the drain current is equal to the source current. Here we have seen that there is existence of an n channel when you make the gate to source voltage positive which was not the case when we were having the gate to source open circuit. That means we did not have channel or induced n channel present earlier but now we have an induced n channel by making this gate to source voltage positive and that is why this device is called enhancement type MOSFET. That means we are enhancing the channel or the induced n channel. Earlier it was not there, now we have enhanced that channel. We are inducing or we are making the availability of this channel. That is why it is called enhancement type MOSFET. This is the length of this channel which is L. Earlier we denoted that by L and width of this channel is actually another important parameter that's also going to make a difference in the current. That is what we are going to discuss next.

Let us now go on increasing the drain to source voltage keeping V_{GS} fixed. We are not changing the gate to source voltage but we are increasing the drain to source voltage. What will happen?

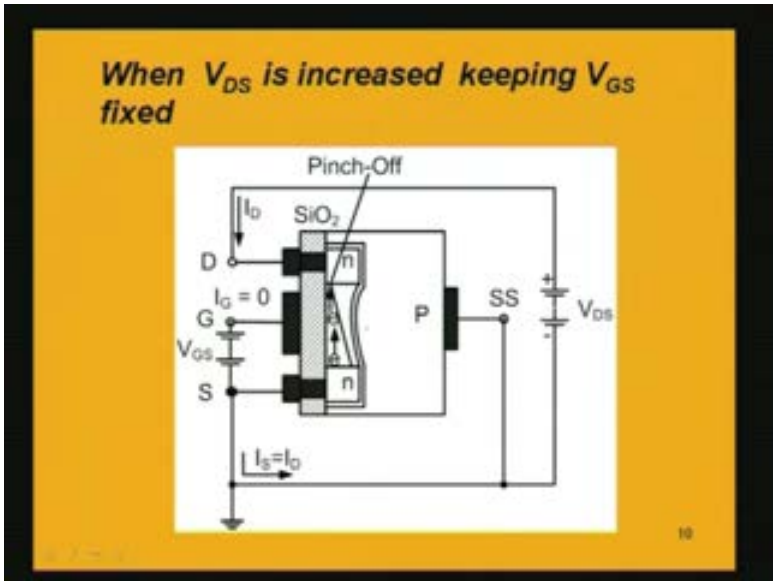
(Refer Slide Time: 33:06)



When you increase the drain to source voltage the width of the channel will change. Because at any point in the channel if we want to find out the voltage between the gate and that point then we see that this voltage is varying because if we are here at the source the voltage from gate will be V_{GS} gate to source voltage at this point. But if we go up, at any point if we want to find out what is the voltage between gate and that point then this is not same as the voltage which is here. If we go on towards up, finally reach the drain then the voltage between gate and that point on the drain will be equal to V_{GS}-V_{DS}.

The voltage between the gate and the point along the channel it decreases from the V_{GS} which is the voltage when the point is on the source and then if we go upward towards the drain the voltage will be V_{GS}-V_{DS}. If we now reach the drain end then what will happen is that the channel width which is between the drain and the source that channel width will not be same, it will be varying.

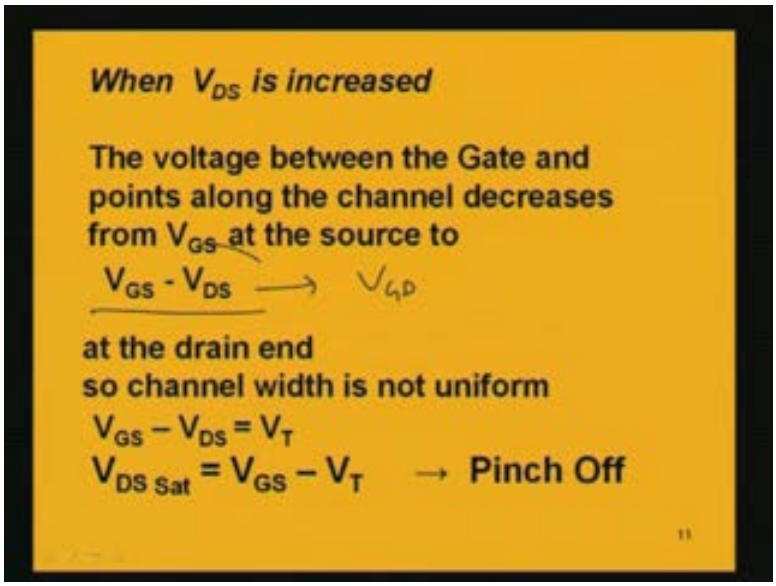
(Refer Slide Time: 35:02)



This width will be maximum when it is at the source and if we go up this channel, it will reduce. It will be tapering towards the drain because the width of the channel depends upon the available voltage between the gate and the drain. If the gate to drain voltage goes on reducing then the attractive force which it exerts upon the electrons to attract them will reduce. If we travel from source upwards and reach the drain at this point, when the point is on the drain this voltage V_{GD} that is between gate to drain, which is nothing but V_{GS}-V_{DS} that will be least at the drain when the point is at the drain. The width of the channel basically is dependent upon the attractive force on the electrons by the gate to drain voltage. If this gate to drain voltage reduces that means the attractive force on the electrons also reduces. That is why the width of the channel will reduce from source to drain.

If we go on increasing the drain to source voltage ultimately the channel width will so reduce that it will be only boiling down to a point and that is called pinching off. When the channel width is just a point only, this width is reducing and reducing as we are going on increasing and increasing the V_{DS} because increasing and increasing the V_{DS} will have an effect that this whole V_{GS}-V_{DS} will reduce. That is nothing but V_{GD}, gate to drain voltage.

(Refer Slide Time: 37:14)

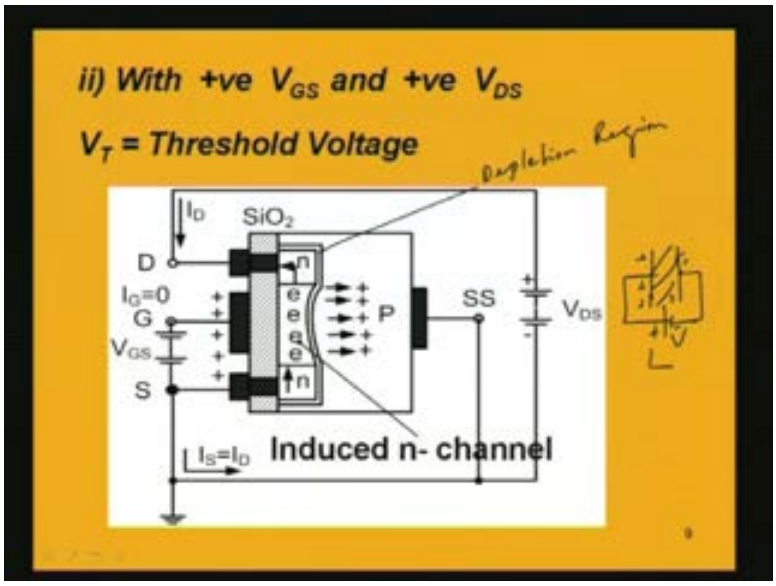


If we go on increasing this V_{DS}, the voltage between gate and drain will reduce and that is why the channel width will reduce and reduce towards the drain and if we go on increasing V_{DS} so much that ultimately the channel width boils down or reduces to a single point only that is called the pinch off and at that point the saturation of the drain to source current occurs. The increment of V_{DS}, if it is such that V_{GS}-V_{DS} finally become equal to the threshold voltage, then that is called the pinch off point or the saturation point. The voltage between the drain to source which causes that pinch off means the saturation that voltage is known as the saturation, the $V_{DS\ Sat}$ and that is given by V_{GS} minus threshold voltage and what happens then? Then the drain to source current becomes saturated and if you go on increasing V_{DS} beyond that value then it will continue to be on saturation. There will be no change. The drain to source current becomes maximum at that saturation point $V_{DS\ Sat}$ when this condition is met. We are increasing V_{DS} so much that the difference between V_{GS} and V_{DS} becomes the threshold voltage. That means gate to drain voltage becomes equal to the threshold voltage for that particular MOSFET, then we get a pinch off or saturation point and the drain to source current becomes saturated. After that even though if you increase the drain to source voltage even then it will continue to be in saturation.

We are having different regions in the drain to source current characteristic. We can now plot the VI characteristic for the MOSFET. Before that one important point is that the name of this device is field effect transistor, FET. Where from that name originates that also has to be understood from this operation because the V_{GS} which is a positive voltage when it is applied, there will be accumulation of positive charges on this side as is shown here. So we will have an effect of a parallel plate capacitor. We know that in a parallel plate capacitor in between the two metallic plates we have a potential being applied. There will be positive charges accumulated on this plate and on this side there will be negative charges accumulated. In between there is the dielectric or insulating material. That is the construction of a parallel plate capacitor. In this case also it is just analogous

to parallel plate capacitor because here we have accumulation of positive charges on this side and on the other side of this insulating material which is a silicon dioxide we have the electrons, which are like the negative charges. 4126

(Refer Slide Time: 41:26)



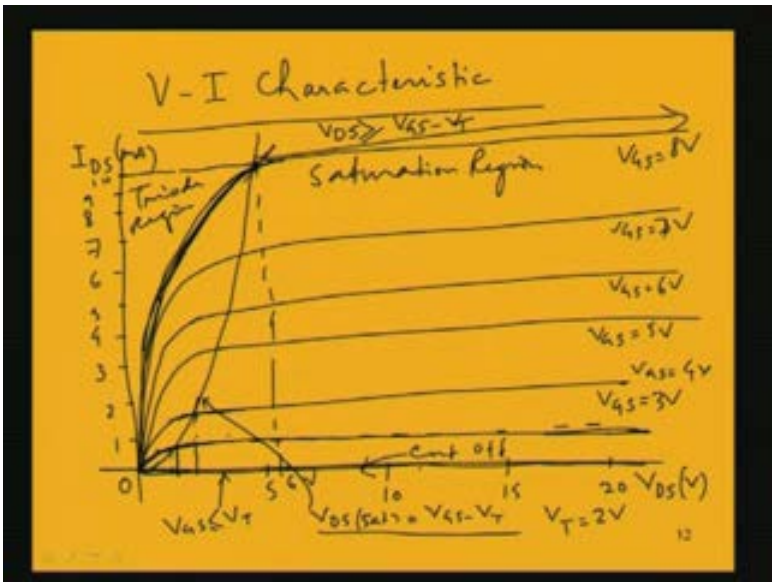
That means in between we have an insulating material silicon dioxide layer. On both the sides of this silicon dioxide we have positive and negative charges, so it is like having the effect of a parallel plate capacitor. There will be a field present which is vertical field. There will be a field. This field will now control the current flow through the MOSFET. The current flow from this drain to source which is because of the flow of electrons from the source to drain that will now be controlled by this field which is present in the parallel plate capacitor being formed on the two sides of this insulating material. The name of this field effect transistor is significant because that field is coming into existence which is not controlling the current flow.

After this discussion we can now proceed to draw the VI characteristic for this n channel enhancement type MOSFET. VI characteristic means basically it is the characteristic between the drain to source current and the drain to source voltage with different levels of V_{GS}. We have the V_{DS} voltage and I_{DS} is in the order of milliampere actually. For different values of V_{GS} we will be plotting the characteristic curve. We have seen that the value of V_{GS} is important for initiating the current in the MOSFET device. If the V_{GS} value is less than the threshold voltage for that particular MOSFET under study then the current between the drain and the source will be zero. For example let us take the threshold voltage for this case as 2 volt. We are dealing with a MOSFET device which is having a threshold voltage of say 2 volt and we will draw the VI characteristic with that assumption in mind. V_T is 2 volt. If V_T is 2 volt for gate to source voltage less than 2 volt there will be no current flow. We have set these as 5, 10, 15, 20, etc voltages and here we have 1, 2; these are the current magnitude in milliampere.

For this region where say V_{GS} equal to 3 volt and onwards we will raise the V_{GS}. Below V_{GS} is equal to 2 volt the current will be zero. This line basically denotes that V_{GS} is less than threshold voltage V_T. As we go on increasing the V_{GS}, when V_{GS} is equal to 3 volt, then there will be rise of current and it will be of this type. Initially the current rises. Then if we go on increasing V_{DS} then it will be saturation. We will get saturation and that saturation voltage V_{DS} is equal to V_{GS}-V threshold. We know that V_{DS} saturation equal to V_{GS}-V threshold. From this relation basically we can draw the locus of the saturation value of V_{DS} and as V_{GS}-V_T gives the locus at the point of this V_{DS}, when V_{GS} is equal to 3, we are considering V_T is equal to 2. It will be 1 volt, somewhere here. We will have basically a locus like this. That will give you this relationship of V_{DS} saturation equal to V_{GS}-V threshold. For a particular V_{GS}, the saturation value of V_{DS} is this much. It is 1 volt for V_{GS} is equal to 3.

For V_{GS} is equal to 4, we will get a saturation V_{DS} value of 4-2 which is equal to 2 volt. Here it will be 2 volt. We will get saturation at a value of 2 volt. So V_{GS} is equal to 4 volt. In this way if we go on increasing this to V_{GS} is equal to say 5 volt, we will get this and one thing to notice is that the gap between 3 and 4 is not equal to the gap between 4 and 5. In this way it will continue. Finally when V_{GS} is equal to 8, then you have 6 volt as the saturation and the current is at 10. Basically we will get V_{GS} is equal to 8 volt. This voltage is 6 volt which is the saturation. Saturation voltage means up to this voltage the current will rise but after that voltage is reached the current will be saturated. This is actually the saturation region for this MOSFET and this is cut off because below this value of V_{GS} is equal to V threshold, the device is in cut off. So this is the cutoff. Below this V_{GS} is equal to 2 volt it is cut off and this region is called triode region where the current rises almost nearly. This is the triode region. In this region of saturation we have the drain to source voltage greater than V_{GS}-V_T. When these are equal V_{DS} equal to V_{GS} minus V threshold, then we got saturation and beyond this point saturation continues. Below this region here V_{DS} is less than V_{GS} minus V threshold and here in the cut off V_{GS} is less than V threshold.

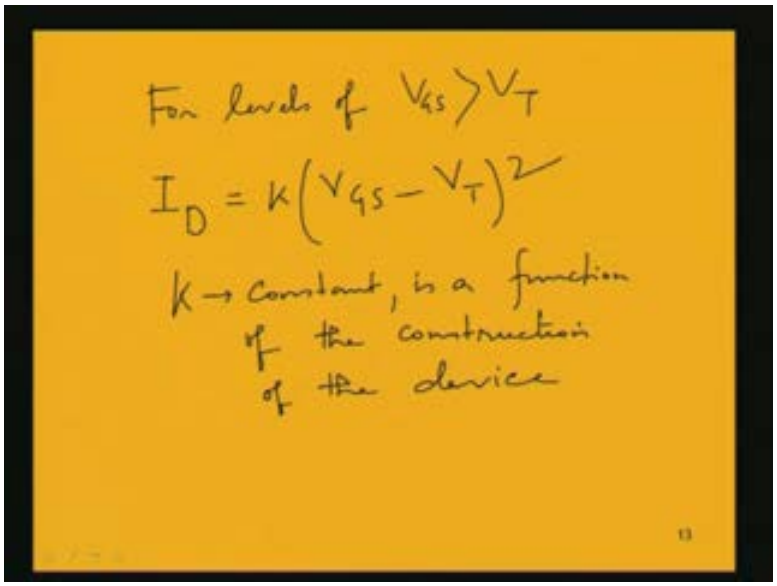
(Refer Slide Time: 50:55)



This characteristic curve gives you the idea about the the change in the drain to source current with gate to source voltage as well as drain to source voltage. If we keep one fixed, suppose we are keeping V_{GS} fixed we get a particular curve and that will give you the idea about the saturation when it occurs and we have seen that the saturation occurs when you have the drain to source voltage greater than equal to gate to source voltage minus V threshold.

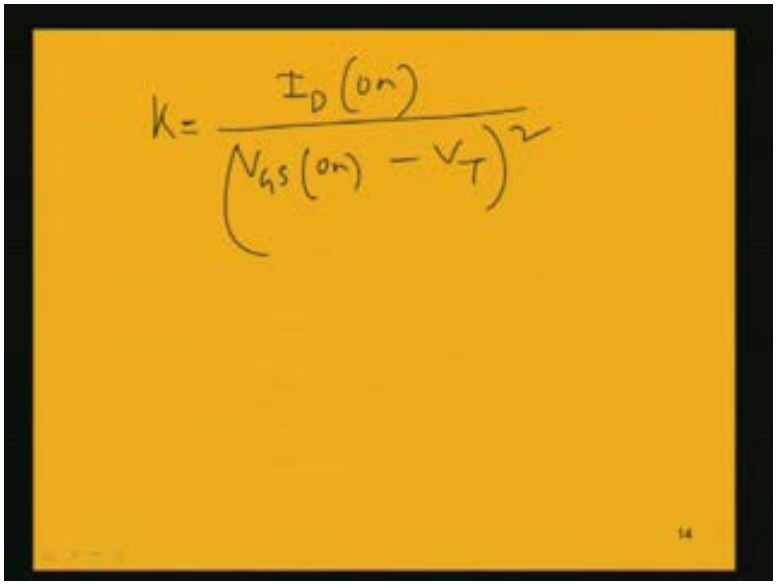
Another important relation actually which holds about the magnitude of the current is for levels of gate to source voltage greater than V threshold. If we look into this figure when we have V_{GS} greater than V threshold, then the current starts rising. This is the rise of current. This rise of current is not exactly linear. Basically what is happing here is that we are getting a curve which gives you the change of the drain to source current with the gate to source voltage. If we go on changing the gate to source voltage the current value can be obtained by a relation. What will be that relation? That is given by the drain to source current I_D is equal to k into V_{GS} minus V_T square. Basically this is a non-linear relationship as there is a square. k is the constant which is a function of the construction of the device.

(Refer Slide Time: 53:44)



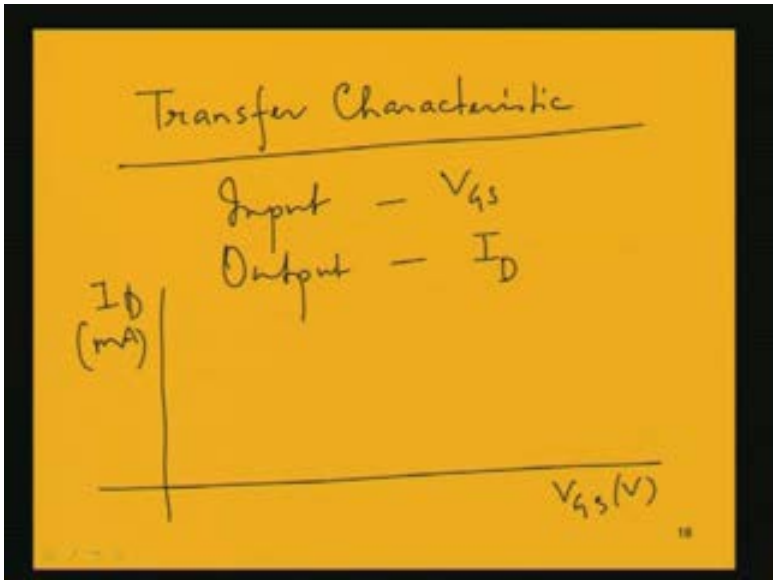
For a particular MOSFET device, the value of k we can know and for a particular MOSFET device the value of threshold voltage also we know. The relation between the drain to source current and VGS that can be found out from this relationship and how to find out the value of k? Suppose we have known the value of the current for a particular value of V_{GS}, then we can find out k by measuring this V_{GS} and I_D after it is on. This can be found out by I_D(on); from this relationship only we are finding. I_D(on) by this square term; V_{GS}(on) means once it starts to conduct after the threshold voltage has been overcome, after this threshold voltage is reached, it is minus V threshold. 5508

(Refer Slide Time: 55:08)



This gives you the value of the k. This relation is important to get the drain to source current. From this drain to source current characteristic versus V_{GS} we can also know about the transfer characteristics. Transfer characteristics are the characteristic between the input and the output. If we consider this MOSFET device a transfer characteristic is characteristic between input and output. What is input here? We are controlling with the gate to source voltage and our output is the drain to source current. Output is the drain to source I_D. Basically it is I_{DS} but generally we write it as I_D, the drain current. It is drain to source current, source is grounded. The characteristic curve between this V_{GS} and I_D gives important information which is known as transfer characteristic. If you are asked to find out the transfer characteristic for this particular MOSFET device which we are having with us then we will have to draw the characteristic between V_{GS} and I_D. How to draw this characteristic between the V_{GS} and I_D that is one important thing. 5708

(Refer Slide Time: 57:08)



This I_D characteristic is non-linear as we have seen here in this relationship. This is the non-linear characteristic curve. We will have to fit in a non-linear curve. It is not linear, it is not enough to find only two points and connect but we will have to know a number of points and connect them to get this transfer characteristic. That we will discuss later.

In today's discussion we discussed about a different transistor, different from BJT, which is a unipolar device known as FET, field effect transistor which has found tremendous use and is very popular in VLSI technology and the particular device which is having enormous use in VLSI technology is one particular type of FET we discussed that is called MOSFET. We discussed about one type of MOSFET which is enhancement type MOSFET and n channel enhancement type MOSFET we have discussed today. We have seen the characteristic curves and also we have known about the basic operation or physical operation of the enhancement type n channel MOSFET and in next classes we will discuss about the other type of MOSFET that is the depletion type MOSFET.