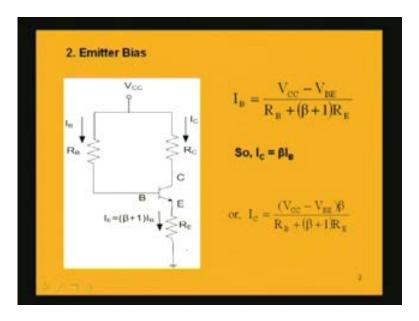
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Module: 2 Bipolar Junction Transistors Lecture-4 Biasing the BJT – Part 2

In the last class we discussed about fixed bias scheme and saw that this biasing scheme is highly sensitive to variation of beta. If beta changes, then the operating point will shift. Let us discuss some other scheme of biasing where this effect of change of beta on the operating point can be counted by designing the biasing scheme parameters specifically. One method of biasing which we will now discuss is emitter bias. In emitter bias scheme there is a resistance in the emitter. That is R_E this resistance in the emitter serves one particular purpose. That we will discuss.

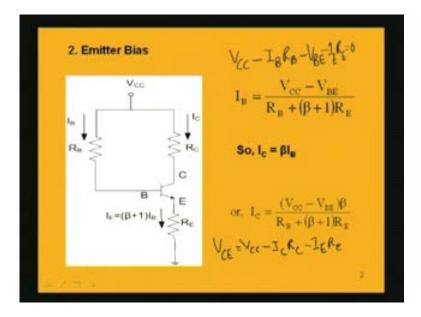
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But the difference between the fixed bias and this emitter bias scheme is that we have a resistance in the emitter circuit. Emitter to ground has a resistance R_E . In this scheme we now find out what will be the base current I_B ? Applying the Kirchoff's voltage law again in the loop from V_{CC} if we travel to ground through the base then we get V_{CC} minus this drop which is I_E into R_E minus I_B into R_B is equal to zero. V_{CC} minus I_BR_B minus base to emitter voltage drop we have to consider; you cannot forget that minus V_{BE} minus this drop I_ER_E equal to zero. This is the Kirchoff's voltage law in this loop. If we express this emitter current I_E is equal to beta plus II_B then we get the expression for the base current equal to V_{CC} minus V_{BE} divided by R_B plus beta plus 1 into R_E and the collector current I_C can be found out after finding out this I_B . We can multiply I_B by beta and we get the collector current.

In all these analyses we are ignoring the leakage current or reverse saturation current because it is in the active region. We can very well neglect that reverse saturation current part. It is a linear relationship that is I_C is equal to beta times of I_B . If you substitute the value of I_B from this expression we get the collector current as beta times this expression of I_B which is V_{CC} minus V_{BE} divided by R_B plus beta plus $1R_E$. This is collector current. If we know the collector current we can travel from V_{CC} to ground through the collector emitter loop. If we now look into the expression for V_{CE} , V_{CE} will be V_{CC} minus I_CR_C minus I_ER_E . We can write V_{CE} equal to V_{CC} minus I_CR_C minus I_ER_E . Once we know this I_C we substitute this I_C here and I is equal to I_C+I_B . I_B is already known, so we can find out the operating point.

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Here the inclusion of this resistance in the emitter serves one special purpose of selfbiasing. This circuit is also known as self-bias. That self-biasing can be understood if we see the consequence of increase of the collector current due to temperature increase. Suppose the temperature is increased then as temperature is increased, the reverse saturation current I_{CO} will rise. I_{CO} rises means the collector current I_C will rise. As a result of this, the operating point will shift because a rise of collector current means your operating point will shift towards the saturation region from the earlier operating point. If this shifting occurs then our biasing scheme whatever we have designed will now not be valid because we have a different operating point, shifted operating point. To counter effect that, that is taken care of by this emitter resistance. If we have a rise of I_C because of rise of I_{CO} what will happen? This drop across this emitter resistance will rise because this resistance drop is I_E into R_E . I_E into R_E will increase because of increment of I_C . As this drop increases the current in the base that is base current which is equal to nothing but V_{CC} minus V_{BE} minus $I_E R_E$ divided by R_B . That is the base current.

If we have a rise of I_C correspondingly I_E will rise and so this drop $I_E R_E$ will rise. As it is having a negative sign, increment of $I_E R_E$ means the whole numerator quantity will be

decreased. That means we are now having I_B lesser. Whatever increment has taken place in the I_C that will be balanced because of this increment of I_C resulting in the numerator quantity being decreased. I_B will again come down and coming down of I_B will in fact cause I_C to come down. It will bring the I_C down because beta times of I_B is equal to I_C . If you have I_B brought down then I_C will also be brought down. That means whatever increment of I_C has taken place is due to increment of temperature. Because of rise of the saturation current, this effect again dropped the I_B back. Because this dropping increased across this resistance, that in fact again brought down the collector current. Whatever effect was there, because of rise of I_C that is counter balanced by this method of selfbiasing. That is why it is called self-biasing.

This scheme is better than the fixed bias scheme in this sense and even if beta changes because of say replacement of the transistor during operation by another transistor which has a different beta then we see here in this expression that I_C is equal to V_{CC} minus V_{BE} into beta by this expression in the denominator which is R_B plus beta plus $1R_E$. As this I_C is sensitive to beta variation because beta is sitting both in the numerator and denominator if beta changes I_C will change. But if we see the expression of I_C carefully and maintain one particular criterion that the resistance R_B if it is very, very less then beta plus $1R_E$ times that can be designed accordingly. While designing the biasing scheme, we can design in such a way that if we make the value of the base resistance very, very smaller than the whole expression of beta plus 1 into R_E , then we can write down this expression approximately as V_{CC} minus V_{BE} into beta divided by this whole summation. If this term is very small than this term we can approximately write the whole denominator term as beta plus $1R_E$ because in comparison with R_B this factor is quite large if the design is done like that.

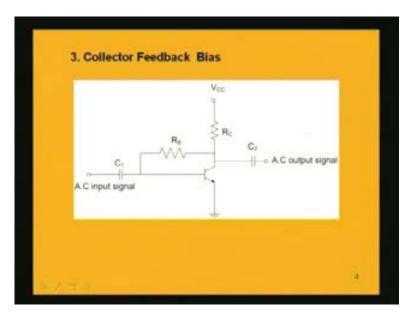
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Bias Stabilization If $R_p \le (\beta+1)R_p$, then Thus I_c is independent of β till << (B+1)R_e condition holds

We can write beta plus $1R_E$ and beta and beta plus 1 values are almost equal because beta is a high value. Suppose beta is 100; 100 and 101 can be assumed to be equal. So beta

and beta plus 1 can be cancelled out. In this expression of I_C , now we will be left with final expression V_{CC} minus V_{BE} by R_E getting rid of that term beta and that is the aim of our design because we should get rid of the term beta in the expression for I_C since beta variation then will not affect the I_C . I_C will not vary with beta. Finally in this expression of I_C we see that V_{CC} minus V_{BE} , V_{BE} is that constant drop of 0.7 volt for silicon, V_{CC} is a constant biasing voltage that we applied and R_E once we designed R_E we are not going to change it. This whole expression is now the expression for I_C and it is not affected by beta. I_C is independent of beta if we maintain this particular design criterion. Under this condition only I_C will be independent of beta. As long as this condition holds that we have designed the values of R_B and R_E in such a way that for that particular transistor with a particular value of beta this condition is maintained then we get almost constant biasing scheme. The collector current will not vary with beta that means we are a getting an operating point which is stabilized. This scheme is better than the fixed bias scheme.

Another scheme is there which is collector feedback bias. In the collector feedback bias this collector is having a feedback resistance which is connected to base. That means there is this feedback loop from collector to base through this resistance R_B . Here this is the biasing scheme. Along with the signal when you apply, for this common emitter amplifier, here the input signal we apply at the input between this point and the ground and AC input signal we want to amplify. At the collector point with respect to ground we are expecting an amplified signal without distortion at the output that is the AC output signal.

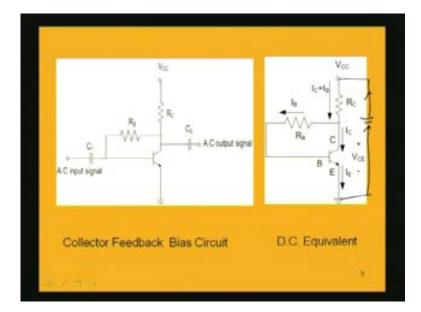


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The presence of these capacitances C_1 and C_2 are to couple the signal effectively and under DC condition when we only discuss the biasing scheme these capacitances are open circuiting because under DC condition capacitance offers infinite capacitive reactance. It is almost open circuit. The DC equivalent circuit for this whole amplifier if we draw we will be left with the circuit which is shown here. Here we are not having this capacitance of C_1 and C_2 and the other side R_C , R_B are there and here we are having a scheme for biasing which is not having a resistance in the emitter. First of all we are only having the capacitor to base biasing resistance R_B and there is no resistance in the emitter. This is a different scheme of biasing which is known as collector feedback bias scheme. In this collector feedback biasing scheme if we analyze the circuit and find out what will be the base current, what will be the collector current and correspondingly what will be the collector to emitter voltage that will define the operating point because operating point is defined by the DC collector current and collector to emitter DC voltage.

We need to find out for this biasing scheme the collector current, the collector to emitter voltage in order to know the operating point Q which is known as quiescent point or silent point means without any signal when we first find out the DC condition. When you apply the signal for amplification then we will have to analyze it in different way drawing the AC equivalent circuit and that we will take up later. For the time being now let us find out what will be the I_C current, what will be V_{CE} ? For this DC equivalent circuit, the current through this R_C will be I_C+I_B because here this base current is flowing into the base and emitter current is I_B+I_C that is the emitter current. The current which is flowing into the transistor must be the same emitter current because that is the current which is out going from the transistor. In order to validly follow the loop the incoming current into this transistor must be equal to the outgoing current. This collector to emitter ground circuit separately if we consider then we can write down this. We can see this whole circuit because V_{CC} is having positive and negative terminal, positive will be here and this is negative, this is ground. So the current which is coming out from the positive terminal of the source must be the same current which will be flowing into the negative terminal.

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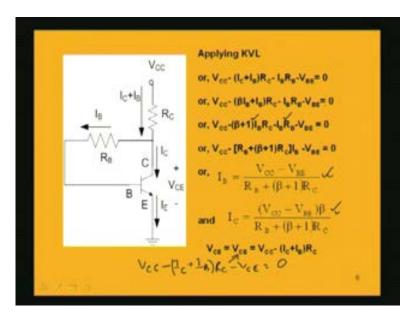
The current which is this current that is the current which is through this resistance R_C has to be then definitely same I_E current I_C+I_B because this current is I_E . This completes

this outgoing current from the source and entering current into the source. So that two are equal. That is why the current which is seen here is I_C+I_B or that is equal to I_E . One part of this current will flow to the base. That is the base current. The other part will flow into the collector and then this collector current and this base current will meet in the emitter that will be together flowing. That is summation of this collector and base current is equal to the emitter current. If we want to find out the collector current then we must first find out base current and then we will multiply it by beta.

What is the base current? In order to know the base current we have to follow the travel from V_{CC} through R_B , through base to ground and apply Kirchoff's voltage law. If you apply Kirchoff's voltage law then from this point, it is positive point of the V_{CC} and it will be V_{CC} minus this drop which is equal to I_C plus I_B into R_C minus this drop which is equal to I_B into R_B minus V_{BE} base to emitter voltage; that is equal to zero. Because this point emitter and ground that is the same point we are not having any resistance there. This is the ground potential, emitter is ground potential. We can further simplify this expression by putting I_C equal to beta times of I_B . I want to find the expression in terms of I_B because then we can easily find out what is the value of I_B . Whatever $I_C I$ can write it as beta times of I_B and then I have the unknown which is I_B only.

Now we get the expression as V_{CC} minus beta plus 1 into I_B into R_C minus I_B into R_B minus V_{BE} is equal to zero or we can further simplify it by writing it as V_{CC} minus R_B plus beta plus 1 into R_C whole into I_B . Taking I_B common between this term and this term I am getting this expression minus V_{BE} is equal to zero. Now I can very easily find out what is the value of I_B ? What is the value of I_B ? I_B is equal to V_{CC} minus V_{BE} divided by R_B plus beta plus 1 into R_C . This expression of I_B will lead us to find out I_C by simply multiplying I_B by beta. Beta times this expression V_{CC} minus V_{BE} by denominator, R_B plus beta plus 1 into R_C , this is my I_C . I have found out the value of I_C by putting the values of corresponding resistances and the value of beta for the particular transistor that we are using as well as the applied biasing voltage V_{CC} because here one voltage source is used that is V_{CC} and we can easily find out the value of I_C .

What is the value of collector to emitter voltage that is required to be known? V_{CE} can be found out if I travel from V_{CC} towards ground through the collector emitter part. Starting from this point V_{CC} minus I_C plus I_B into R_C minus V_{CE} equal to zero. That is the Kirchoff's voltage law in this output circuit. That is V_{CC} minus I_C plus I_B into R_C minus V_{CE} equal to zero. From here I can find out what is V_{CE} ? V_{CE} is equal to V_{CC} minus R_C plus I_B into R_C . We are having the operating point defined by I_C and V_{CE} . (Refer Slide Time: 21:21)



Having known the operating point now let us see whether the bias stabilization is satisfied here or not meaning in what way the change of beta will affect the collector current? Here we are considering change of beta which is actually more prominent than the other changes which may also occur like temperature change. But we are considering beta change which has a dominating effect on this change of I_C corresponding to the shifting of the operating point Q. Let us find out how the change of beta is going to affect the collector current. In this expression it is very clear that beta is there in both the numerator and denominator for this expression for I_C . So definitely it is very sensitive to beta variation.

If we can design the biasing scheme in such a way that we can have the expression for I_C getting rid of the term beta in the limiting condition of some limiting design specification being made then we can achieve that. For that intuitively we can see that in the denominator of this I_C expression we are having R_B plus beta plus 1 R_C . Like as we have done earlier in emitter base configuration if we now can make the value of R_B to be very, very small in comparison with the other term in the denominator that is beta plus 1 R_C . Then we can write this whole expression as having in the denominator beta plus 1 R_C . That's actually possible if R_B is very, very less than beta plus 1 R_C . Then we can write the expression for I_C as V_{CC} minus V_{BE} into beta by beta plus 1 R_C and then we can cancel beta and beta plus 1 which are nearly equal because beta is a high value and then we will be getting an expression which is not having beta. That is what is obtained here. Finally if this condition is met that is R_B is very, very less than beta plus 1 R_C then we can get that I_C is approximately equal to, exact expression it is not so; but after satisfying this design criteria we can write approximately I_C equal to V_{CC} minus V_{BE} by R_C and here it is independent of beta.

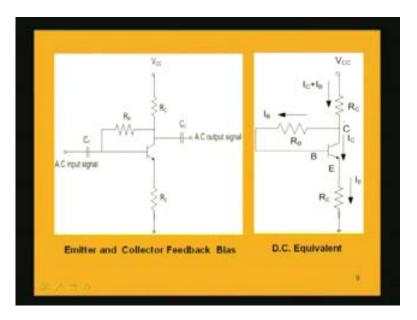
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Bias Stabilization	
If R _g << (β+1)R _c , then	
or, $I_c \approx \frac{(V_{cc} - V_{BE})}{R_c}$	
$I_{\rm c}$ is independent of β	

That means we are making this I_C independent of beta after meeting the design specification in this way. This is a key expression or the key design condition we have to meet while designing this biasing scheme and then we can achieve that I_C being insensitive to beta.

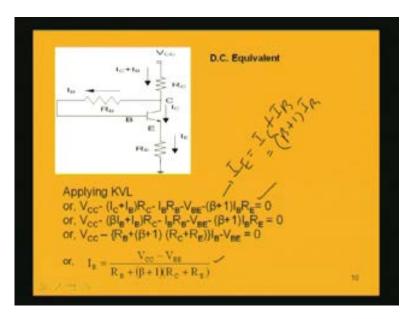
This collector feedback bias can be actually combined with the emitter bias which we discussed earlier in order to give a biasing scheme which is emitter and collector feedback bias scheme. Here collector feedback resistance is there which is at the collector to base resistance and this emitter is also having a resistance. Basically this scheme is having both the aspects of collector feedback bias as well as emitter bias or self bias. This is the biasing scheme that when you apply to a common emitter transistor amplifier, the whole circuit for this amplifier will be like this. Here we are applying the AC input signal and we will be getting the AC output signal at this point at the output and in order to analyze the circuit in the biasing condition, we have to find out the DC equivalent circuit and the equivalent DC circuit for this amplifier is this one. C_1 and C_2 being open circuited under DC condition, we are getting this collector emitter feedback bias. Here there is this resistance in the emitter; others are same as the scheme that just now we discussed that is the collector feedback bias scheme. Here also we can find out the insensitivity of I_C to beta condition.

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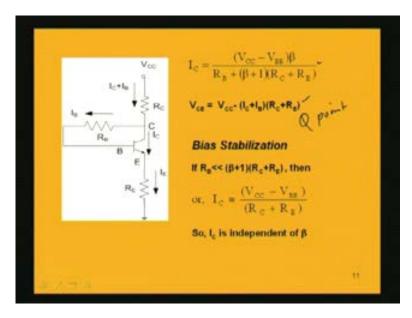
First of all in order to find out what is the collector current we must find out base current. KVL being applied to the circuit having this collector base loop, we will apply the KVL in this loop. It will be V_{CC} minus I_C plus I_B into R_C minus I_B into R_B minus V_{BE} minus beta plus II_B into R_E is equal to zero. Here we will have to be careful that R_E is the resistance in the emitter. It is not simply grounded it is through a resistance that is grounded. We have this equation; here instead of writing I_E it is just written in this way. For easy calculation of I_B we have written down I_E is equal to I_C+I_B that is equal to beta plus $1I_B$.

Using this we are getting the final expression of I_B from these equations after simplification. First step simplification is we have to write down I_C is equal to beta times I_B . All the ICs we will be writing down as beta times of I_B . Then we get beta times I_B plus I_B into R_C minus I_B into R_B minus V_{BE} minus beta plus II_B into R_E is equal to zero or taking I_B common we get V_{CC} minus R_B plus beta plus 1 into R_C plus R_E minus V_{BE} is equal to zero. What we get in the expression for I_B is this one. V_{CC} minus V_B by R_B plus beta plus 1 into R_C plus R_E . In the earlier collector feedback bias scheme we had here R_B plus beta plus $1R_C$. But in this scheme R_E term will come. R_E will be coming in the denominator in extra with R_C . (Refer Slide Time: 28:43)



If we know I_B we can find out I_C by multiplying with beta and correspondingly we can find out V_{CE} which is equal to V_{CC} minus this drop minus this drop. That means V_{CC} minus I_C plus I_B into R_C minus I_B plus I_C into R_E . Combining I_C+I_B , taking it common we can write this expression. This is V_{CC} expression. This is I_C . So we know what will be the Q point which is defined by I_C and V_{CE} ?

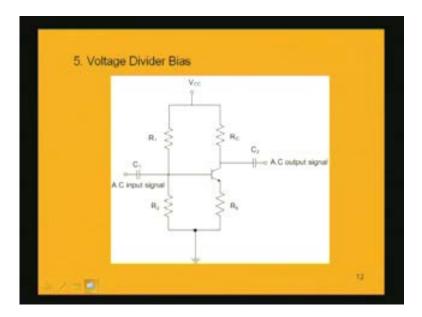
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What about the bias stabilization under this circuit? The condition is if R_B is very, very less as compared to beta plus 1 into R_C plus R_E then we can write approximately I_C equal to V_{CC} minus V_{BE} into beta divided by beta plus 1 R_C plus R_E . We can cancel out beta

and beta plus 1 and final expression will be I_C almost equal to or approximately equal to V_{CC} minus V_{BE} by R_C plus R_E . Here we are getting rid of the beta term. So we have made I_C independent of beta provided we maintain this design scheme of making or keeping R_B very less as compared to beta plus 1 into R_C plus R_E . You have to design it like this; design the circuit like this. That means keeping in view this criterion that only if this is met then the I_C , collector current can be made insensitive to beta.

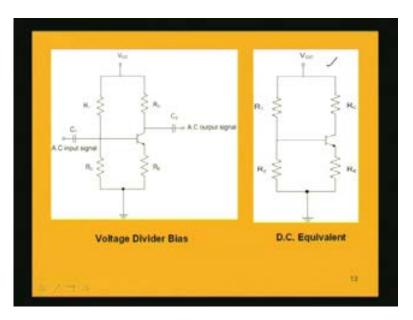
Finally we will discuss a scheme which is most popularly used having advantages which is known as voltage divider bias scheme or potential divider bias scheme.



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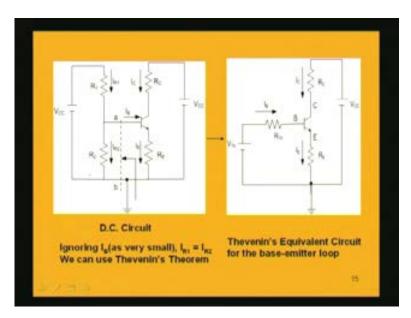
In this scheme apart from using a single resistance R_B there are 2 resistances R_1 and R_2 being used in this fashion. Others are similar to the earlier schemes. That means R_C and R_E are there and we do not have a single R_B but we are having R_1 and R_2 . That is a potential dividing scheme like this one is used for this bias scheme and this is the whole amplifier circuit. In this circuit if we analyze the DC condition that means we open circuit C_1 and C_2 under DC condition. It will be this circuit which is the DC equivalent circuit for this amplifier. Here R_1 , R_2 , R_C and R_E are the resistances in the collector and emitter.

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For easy analysis I have divided or separated out the resistances R_1 and R_2 with V_{CC} and the other is R_C and R_E . This is also sharing this V_{CC} . This scheme I am drawing to easily understand the circuit and this is the base point. Collector point is here, emitter is here. In this circuit we have to find out base current.

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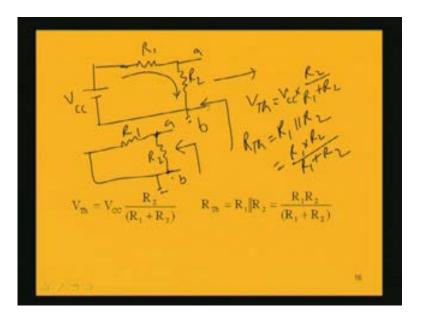


What we can do is that we can simplify the circuit or we can make it more easier for analysis if we concentrate on this base to emitter circuit and try to find its equivalent Thevenin's circuit. Then we can easily analyze it and that will be clear. We look from this point into AB terminal and find out what will be this equivalent circuit by Thevenin's theorem. We replace this V_{CC} , R_1 and R_2 by its Thevenin's equivalent at this point. That means we look into the AB terminals from this side. We are trying to find out the equivalent Thevenin's circuit from base to ground. We will look from these two points and find out what is the Thevenin's equivalent. We know Thevenin's equivalent circuit consists of two things. One is the Thevenin's equivalent voltage and the Thevenin's equivalent resistance that we have to find out first.

In order to find out Thevenin's equivalent voltage we have to open circuit these two points and find out open circuit voltage across these two points and in order to find out the Thevenin's equivalent resistance you kill the independent source V_{CC} , find out the equivalent of these two resistances. In order to do that we will have to find out what is the Thevenin's equivalent? We have this V_{CC} and we have this R_1 and R_2 ; basically across these two points A and B. The right side of this circuit is having all those base and collector circuit, etc but then we are finding out Thevenin's equivalent looking from this point. That is across AB we are looking at to find out the Thevenin's equivalent.

Thevenin's equivalent voltage across these two points $V_{Thevenin}$ can be found out. It is a voltage division provided this base current is ignored. If base current is ignored then only we can find out Thevenin's equivalent like this. Because if base current is not ignored, there is a base current flowing and then this IR_1 and IR_2 will not be equal. Exactly IR_1 and IR_2 are not equal but conveniently we will ignore this base current since its value is very small and approximately we can replace this whole circuit by its Thevenin's equivalent provided this I_B is ignored. It is very small, so we can neglect it. That means this current and this current are same if we neglect base current. Then we can find out this equivalence. Here this point is to be noted. Same current should flow otherwise you cannot find out Thevenin's equivalent in this way.

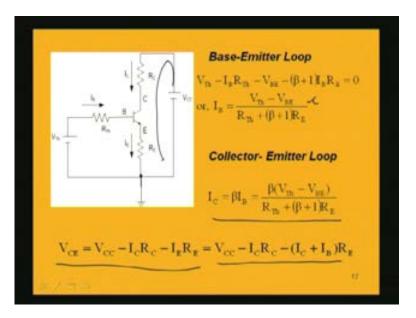
What is Thevenin's equivalent voltage across these two points? V_{CC} into R_2 by R_1 plus R_2 and while finding out Thevenin's equivalent resistance we must kill this voltage source, independent source. So it will be this one. Across AB we are finding out what is the equivalent resistance. Looking from this terminal that is nothing but you have this point ground; mind it this point is ground. So this is R_1 parallel R_2 . These two resistances are in parallel R_1 parallel R_2 . That means it is R_1 into R_2 by R_1 plus R_2 . (Refer Slide Time: 36:46)



That's what we get for this circuit to the left of this base to ground. That means across this AB we are getting this Thevenin's equivalent circuit. Now we can replace easily this by V Thevenin in series with the R Thevenin resistance. The left part is taken care of by this V Thevenin and R Thevenin and this right side is exactly same. We are not doing anything. Now it is easier for us to find out the base current in this loop. If we find out the base current, what will be the base current? This is the equivalent circuit after replacing the base to ground circuit by its Thevenin's equivalent to the left.

If we consider the base emitter loop V Thevenin minus I_B into R Thevenin minus V_{BE} minus I_E into R_E or beta plus 1 I_B into R_E is equal to zero. We can find out what is the base current? Base current is equal to V Thevenin minus V_{BE} by R Thevenin plus beta plus 1 into R_E . This is the expression for I_B finally. Once you know I_B we can find out I_C . I_C is equal to beta times of I_B . So beta times into this whole expression and what is the collector to emitter voltage V_{CE} ? Again we have to go by this loop, apply KVL; V_{CC} minus I_C into R_C minus this drop which is I_E into R_E . That is equal to V_{CE} . Then V_{CE} is equal to V_{CC} minus I_C into R_C minus I_C plus I_B into R_E also you can write or you can directly write beta plus 1 into I_B into R_E and I_C we have already found out and we can also find out by writing it beta times of I_B . Finally we get V_{CE} and we get I_C . This determines the operating part or the quiescent part

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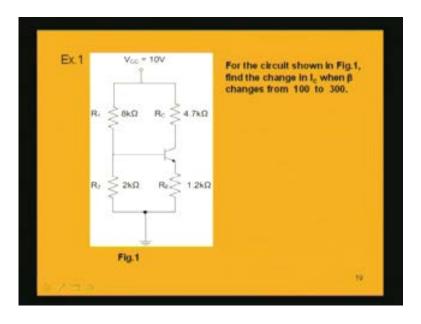
The bias stabilization can be done or the I_C current can be made insensitive to beta if the denominator term R Thevenin that is Thevenin's equivalent resistance can be made very, very small as compared to beta plus 1 R_E. Then this expression will be boiling down to I_C is almost equal to V Thevenin minus V_{BE} by R_E because beta by beta plus 1 will cancel. Since we are writing R Thevenin plus beta plus 1 into R_E approximately equal to beta plus 1 into R_E ignoring this R Thevenin since it is very, very less than whole term beta plus 1 into R_E and V Thevenin and R Thevenin we can calculate. We already know V Thevenin; V_{CC} into R_2 by R_1 plus R_2 . R Thevenin we know R_1 parallel R_2 .

We have made I_C insensitive to beta which will be equal to V Thevenin minus V_{BE} by R_E . There is no beta here. It is made independent of beta by choosing this properly. These resistances should be chosen properly and here one thing is to be noted that since we are having two resistances R_1 and R_2 we can very well find that combination of R_1 and R_2 ; the value is small, R_1 and R_2 will be small and the parallel combination of R_1 and R_2 will be still smaller. That can be made small in comparison with beta plus 1 R_E and it is more flexible in the sense that when we had only R_B , one resistance, in earlier cases then to make R_B very small it was difficult because other criterion will also be there. You cannot have R_B very small because I_B will be increasing and there is a limiting condition for every transistor which is very much specified in the data sheets. What will be the limiting conditions, limiting power, etc. Actually we are not free to choose any value but within the limitations we can choose better values to make this happen, this condition to be satisfied and it is better to have two resistances R_1 and R_2 . We can very well choose the combination in order to meet this specification than deciding on a single resistance R_B that was done earlier. (Refer Slide Time: 41:35)

Bias Stabilization $I_{c} = \frac{\beta(V_{m} - V_{H})}{R_{m} + (\beta + 1)R_{H}} \begin{bmatrix} V_{1h} + \left(\int_{C} \frac{1}{\beta(1)} \int_{C}$		
So, I _c is independent of β	12	

Let us try one example. In this potential divider circuit biasing scheme we have to find out the change in the collector current I_C when beta changes from 100 to 300.

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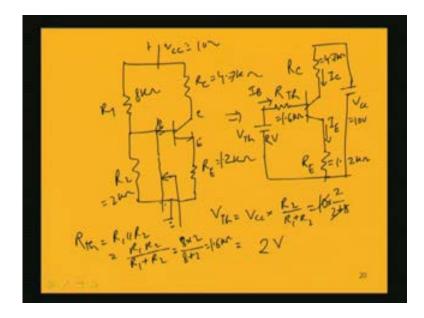


That is in one case beta is 100 and in the other case beta is 300. We have to see the change in the current I_C . In this circuit the potential divider biasing scheme has the resistances as 8k R_1 , then R_C is 4.7k. V_{CC} is 10 volt and this is an NPN transistor and then this resistance R_E is 1.2k and this R_2 is 2k. This is ground and beta is also given whose value is changing actually. One is 100 first case another is 300. I will first draw the equivalent circuit using Thevenin's. This whole circuit can be written down as the circuit

using the Thevenin's equivalent like this. This is V_{CC} . V_{CC} is 10 volt, R_C is 4.7 kilo ohm. R Thevenin and V Thevenin we have to find out. R_E is given as 1.2 kilo ohm. What is V Thevenin? That is equal to V_{CC} into R_2 by R_1 plus R_2 .

If we look from this base this is collector, this is emitter. You have to look from base to ground these two points. You look at the circuit to the left. I want to find out across these two points. V_{CC} into R_2 by R_1 plus R_2 and that is equal to 10 into R_2 is equal to 2. R_2 is 2 kilo ohm; 2 by 2 plus 8 is 10. 10 and 10 cancel; it comes to 2 volt. V Thevenin is 2 volt and R Thevenin is R_1 plus R_2 . That is $R_1 R_2$ by R_1 plus R_2 . Multiplying these two, 2 into 8 by 8 plus 2; 16 by 10 is 1.6k. I get 1.6k R Thevenin and I get 2 volt as V Thevenin. This is the base current I_B , this is the collector current I_C and this is the emitter current.

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I will find out I_B . I_B is equal to V Thevenin minus V_{BE} by R_B plus beta plus 1 R_E . Putting down these values here V Thevenin we have found out to be 2 volt. V_{BE} is standard 0.7 volt for silicon. I should not use R_B here. R Thevenin should be proper. I should write R Thevenin. R Thevenin we have found out to be equal to 1.6k. I am keeping all this in k and this voltage is in volt so that finally current expression will be coming in milliampere. 1.6 plus beta; first case beta is 100. Let us take that 100 value and find out the current. R_E is equal to 1.2k into 1.2k. This value will come to be 0.01059 milliampere or 10 to the power 3 in order to write down in microampere. This is milliampere; 10 to the power 3 if we multiply, it will be 10.59 microampere. This 10.59 microampere current is flowing in the base. Corresponding collector current is beta times of I_B . Beta value are 100 into 0.01059 milliampere and that is equal to 1.059 milliampere. This is the first case when beta was 100.

Second case when beta has risen to 300 let us find out. For that case when beta is equal to 300 here I_B will be now changing. I_B value will be 2-0.7. Only beta is changing others are same. I write down for that value of beta 300 plus 1. Here I am only substituting. V

The venin is 2, V_{BE} is 0.7, R The venin is 1.6, beta plus 1 is 300 plus 1 into R_E is 1.2k and this value comes out to be 0.003583 milliampere. I_B is now 3.583 microampere.

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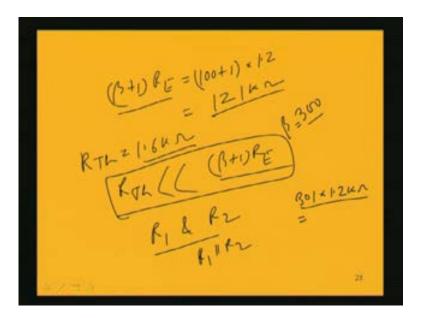
 $I_{B} = \frac{V_{R} - V_{6E} t}{R_{R} + (B+1)R_{E}} \frac{2 - 0.7}{1.6 + (100 + 1) \times 1.2}$ = 0.01059 mA = 10.59 MA $I_{C} = 0 I_{R} = \frac{100 \times 0.01059 \text{ mA}}{1.059 \text{ mA}}$ (11)\$= 300 IB= 2-0.7 1.6+ (300+)

This different value of beta gives different I_B . I_C will also be different. In this case I_C is equal to beta times of I_B equal to 300 into 0.003583. That will be equal to 1.075 milliampere. In the first case collector current was 1.059 milliampere for beta is equal to 100. When beta is 300 that is 3times it has increased. The corresponding I_C value we get is 1.075. In the first case I_C was 1.059. This is 1.059 and now we have got 1.075 milliampere. Even though beta has increased 3 times, percentage value of increase if we see from 100 to 300, 200% times increment of value of beta that will be still giving a rise of I_C which is very, very marginal. That is you can find out this change of del I_C percentage; 1.059 minus 1.075 or if I do this other way round that is 1.075 minus 1.059 by 1.075; that can be found out. The percent has changed. That will come to only 1.5%. When you change the beta, for 200% change of I_B still we get only 1.5% change of I_C . (Refer Slide Time: 49:41)

 $L_{C} = \int I_{B}$ $= 300 \times 003563$ = 1.059 mA $I_{C_{1}} = 1.059 mA$ $I_{C_{2}} = 1.075mA$ $I_{C_{3}} = 1.075mA$

That is actually possible because in this design if we cross check the values of R The venin and beta plus 1 into R_E the design specification that is to be met is R The venin should be very, very less than beta plus 1 R_E. Is it so here? It must be there because otherwise you would not have got such a marginal increment of I_C. Let us see what is beta plus 1 into R_E? In first case beta is 100 plus 1 into R_E is 1.2k; 101 into 1.2 is 121 kilo ohm and the value of R Thevenin is 1.6 kilo ohm. R Thevenin and beta plus 1 R_E if you compare then you see one value is 1.6k, other is 121k. This whole term is very, very less than this. That means our design specification has been already met. That is why the I_C is almost insensitive to beta. Even though beta is changing so much, 200% change but still we are not having corresponding high change of $I_{\rm C}$ and that is the beauty of this design scheme. Here we are making it possible by this design criterion being satisfied. That is why we have the potential divider biasing scheme or voltage divider biasing scheme being used very, very popularly in transistor amplifiers and we basically find its applications in amplifiers. Mostly this potential divider biasing scheme has advantages over the other biasing schemes that are already discussed like the different variations of emitter bias like collector emitter feedback bias. Then earlier we have also discussed collector feedback bias without the emitter resistance. As compared to the all the schemes this voltage divider biasing scheme will edge over the others because of this flexibility in designing. We can design the biasing scheme very effectively by choosing properly the values of R_1 and R_2 to be quite small. R_1 and R_2 values actually have to be made small so that you can maintain this condition. R Thevenin which is nothing but R_1 parallel R_2 should be less than beta plus 1 into R_E. In the other case for this example if you consider, the change of beta as it is 300, new value of beta is 300 for that case still it will be maintained. That can be also checked. It will be even further met because if beta is equal to 300, beta plus 1 is 301. 301 into 1.2k; this value if you consider it will be still higher as compared to this Thevenin resistance R, 1.6 kilo ohm. 5325

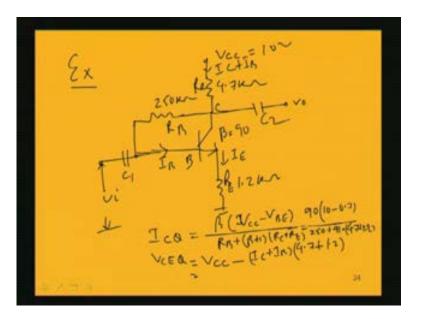
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Both the cases if we see our design specification is met. That is why we have seen that this scheme is very, very effective from the point of view of beta change. Here we are discussing the beta change predominantly. There are other factors that may be present for change of the operating point, one being the leakage current change. That is the temperature at which we are working with the amplifier if that temperature changes suppose it is increasing then corresponding value of I_{CO} will also increase and that value of I_{CO} when it increases, it is increasing the I_C value. Again the operating point shifting will be there but still the effect of beta change actually will be very, very dominant than that I_{CO} change and that is why we are mainly focusing on this change of I_C due to beta.

This is the potential divider biasing scheme and we now consider the collector feedback bias scheme. Suppose we have a scheme which is using the collector emitter feedback bias. That is this transistor is having this 4.7k, here 250k and this is fed back. This collector point with base is fed back to this 250k resistance and we have this 1.2k. In this case V_{CC} is 10 volt. Here we will be applying this input signal and we will be getting the output here but with a capacitor which will be there. It will have a coupling capacitor C_2 and there also it will have a coupling capacitor C_1 . If we consider the DC circuit then this will be removed. We can find out I_C and V_{CE} . Find out I_{CQ} and V_{CEQ} which is the value of I_C and V_C for the operating point. For this particular case using this expression beta into V_{CC} minus V_{BE} by R_B , R_B is this one; R_C is this one and R_E is this one. So R_B plus beta plus 1 into R_C plus R_E ; putting these values we will be getting the I_{CQ} .

Similarly V_{CEQ} can be found out. This is I_C , this is I_E and the I_B is flowing in this loop. V_{CC} minus I_C plus I_B . Here this I_C+I_B current is flowing and this has to be taken care of. I_C+I_B into 4.7 plus R_E is 1.2. If we put these values we can find out I_C first. Beta is 90. Putting the values, 90, 10 minus 0.7, all these values, R_B is 250 plus beta plus 1 being 91; R_C plus R_E , R_C is 4.7 and R_E is 1.2. (Refer Slide Time: 57:39)



With these values we get finally I_C is equal to 1.06 milliampere and V_{CEQ} is equal to 3.68. We can check this calculation and this will be the operating point Q. The Q is written in the subscript meaning that these are the values for that operating point condition; that is the DC condition. That is the Q point. You can find out the Q point on this load line where it will be either here or here or here. The location of the Q point is important.

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L CQ [.06m] VCEQ = 3.68 Q.

In this whole discussion we have discussed about different biasing schemes. We have seen that the potential divider biasing scheme has more flexibility as well as it is insensitive to beta after maintaining or till we maintain a particular design consideration with respect to the resistances being connected. Till that limiting condition is satisfied we can make the operating point insensitive to change in beta.