CMOS RF Integrated Circuits
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Module - 03
Passive IC Components
Lecture - 07
Resistor, Capacitors

Welcome to CMOS RF Integrated Circuits, this is going to be 3 module, we are going to start the third module on passive components. Today's lecture I will try to cover Resistor, Capacitors and if possible more, what are the different passive components

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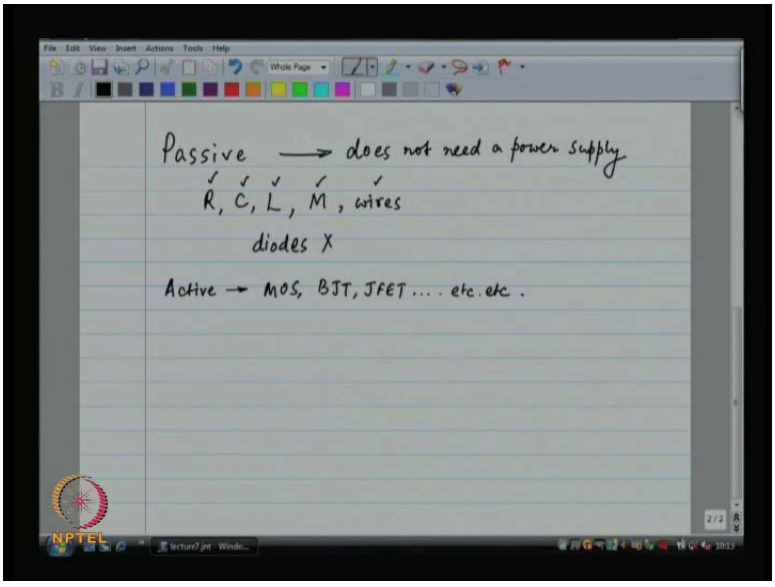

What is passive, passive is something first of all, it does not need a power supply, mostly these components are linear as well, under passive components we have resistors, capacitors, inductors, mutual inductances, even transformers. There is one more new thing over here, and these are wires, I am going to treat wire as components, let us basically study the wire as well. And the in addition you might also consider diodes as passive components, we are not going to study diodes here, in this module.

Not passive components, active components these are transistor, so these could be MOS transistor, BJT transistor, JFET whatever you want over here, so these are passive and active components. We are going to study in this module R, C, mutual inductions, wires

and will not study diodes, will take it up later on. So, first resistor, how do you make a resistor on an integrator surface, not all integrator circuit technology directly offers resistors, but most RF process is do of our resistance.

So, modern resistor are made out of poly silicon, material called poly silicon, the same material which is used for the get of MOS transistor is also used to built resistors, you can also use metal to make a resistor, or in any case, let us just see a what is done.

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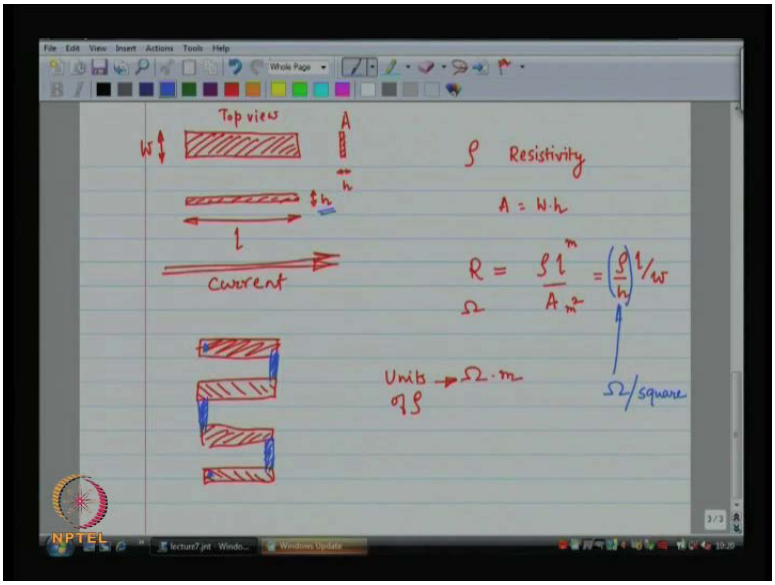

So, this is what is done, a track made out of material which has a resistivity row, I am trying the top view, the side will like this, so these are the side views. It is made out of material which has a resistivity of row, what are the units of resistivity, let us come to the units little later, which made of resistivity row it has a cross sectional area A, it has a length l, height is h and width is w. So, cross sectional area A is equal to w times h and let say you want current to propagate in this direction.

So, in that case I am sure you are familiar with this, the resistance of this track, the resistance are is inversely proportional to A, it directly proportion to the length and it is proportion to row. So, what are the units of row, here we have got ohms here, here we got meters, here we have got meter square, so the units of resistivity row is ohm times meter, now is that fine.

So, you will be told by the foundry that the resistivity of the material that you are going to use, is so many ohm meters, you can use anything, let us say a metal, piece of metal can also be used to make a resistor. How will you do that, all you need to know is the resistivity of the material, and you are done usually we make the resistivity is not enough to make a large enough resistor, I mean with a track like this, we can probably make a 100 ohms, we can probably make 200 ohm. If you want 1 kilo ohm, if you basically want a larger resistor, we usually make lot of tacks and put them in a snake like fashions.

So, now you have got a resistor between this point and this point, which is four times the resistance of each track assuming the tracks are the identical. If you draw it like this, it is a also easy to ratio to resistor, so if you want r and you want 5 by 4 R, then all you have to do is split R into four pieces like I have done, for resistor number 1. And for resistor number 2 you use the same piece and make 5 pieces, so you have got resistor and 5 by 4 times resistor.

Now, typically the height, this height is defined in the process technology, you have no control over the height the foundry decides, what the height is going to be. So, when that is the case, the foundry does not really give you row it gives you row by h, because the height is define by the foundry. So, what is are the units of row by h, row has units of ohm meter, row by h has units of ohm only, now it is funny that the foundry tells you that the resistivity is so many ohm.

So, it is a little funny to relate a ohms over there, they give you a little additional information, they tell you it is so many ohms per square why the I tell you that.

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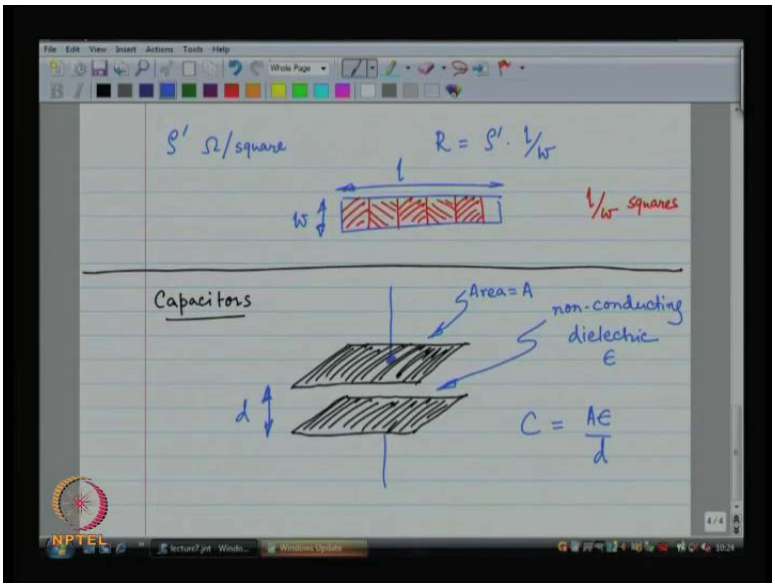

Suppose, it is row prime, the resistant's is row prime times the length divided by the width, so if I have a track of length l and width w, then how many squares are there in this track, there is 1 square, 2 squares and then, a little more. So, the number of squares is l divided by w, so that is why the usually gives the units as ohm per square and then, whatever the width is does not matter, you just count a number of squares in the track and that gives you the resistant of the track.

This is as much as I am going to talk resistors next, let us start talking about capacitors, how do you make a capacitors, what is the easiest capacitors you can think of, any ideas. Two parallel plates, so whenever you see two parallel plates, anything remotely looking like plates which are parallel to each other, separate by non conducting dielectric. If they are not separated by non conducting dielectric does not look like a capacitor any more, it is look like a resistor or something closer to that, a wire short circuits.

As long as there is non-conducting dielectric between the two plates, anything remotely looking like plates looks like a capacitor. And what is the capacitance, this is your high school physics, d, so C is equal to A times epsilon divided by d, that is the capacitance of this parallel plate capacitors. Now, this particular formula which you learn in your high school is valid for two infinitely large parallel plates, otherwise this formula is an approximation.

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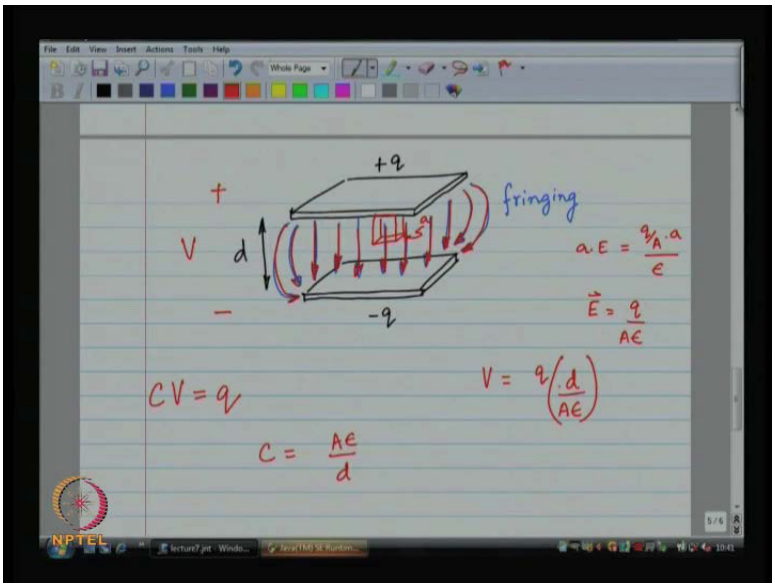

So, what I am talking about here, you have two plates, how was this derived, suppose these plates are infinitely large, they are separated by a distance d, they are infinitely large, you place plus q on the top plate, minus q on the bottom plate. And then, you use gauss law to find out the electric field in the neighborhood of the capacitor. If you put plus q on the top plate, minus q on the bottom plate where will the charge is result with a recede, which surface will reside on, the plus q attract the minus q the minus q attracts the plus q.

As a result all the charge recedes on the bottom side of the top plate, and the top side of the bottom plate, that is where all the charge resides, there is no volume charge inside the plate. Once you understand that, it is easy to compute the field, there is no reason for the field go here and there, the field will go straight to the field lines will go straight someone plate to the other plate. There is no reason for the fields line to go here and there, remember this these two parallel plates are infinity large and then, once you realize this just construct small Gaussian surface around the piece of charge.

So, let us say you construct the Gaussian surface, around this charge it is a surface 3 D, the fields lines are all going straight is the area of the surface is A, and the electric field is E. Then the total area times the field that is coming out is A times E and that is equal to the charge and close divided by epsilon naught. So, let us say this has an area of small

a, so that is basically gives you that the electric field is q by A epsilon, so that the electric field.

The distance between the two plates is d, so the potential different is the field times the distance, the field is constant, so it is fields times the distance, and you relate this to your capacitance, so the capacitance of this objects is A epsilon by d. Now, what is the biggest assumption here, the biggest assumption here is that the size of the plates are infinitely large. That makes the fields line perfectly the straight, they do not have reason to go anywhere else, they keep coming straight perfectly, these are huge plates, so the fields lines come straights.

Now, if you confine the area, if you say that no the size of the capacitors is not infinitely large, then how at the fields line now going to look, well there is going to be something called fringing. So, when you confine this area, the field lines now do not have to go straight anymore, the curve towards the other plates especially at the edges, this effect is called fringing, you might have heard of this. So, along the border of the area of the capacitors there is fringing, so the fringe electric field curves to the other capacitor, so this are also I am sure you are familiar.

So, under this circumstances, what do you think is going to be the capacitance of the structure, so what do you think is going to be the capacitors now, some filed line are still most of the field line still coming, straight down from one plate to the other. Is still have more or less strength, some new filed lines have come curving from one plate to the other, these are the new fields line, this were not there before.

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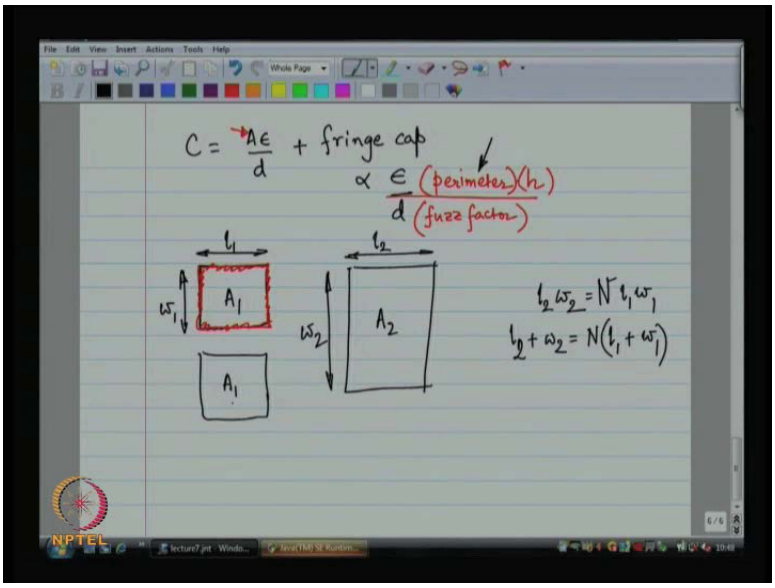

So, the net capacitance, now is proportional to the area, and there is some additional capacitance, because of the fringing. Now, this fringing capacitance is going to be proportional to what, is it going to by proportional dialectic constant, yes is it going to be inversely proportional to the distance between the two plates yes. What else is going to be proportional, is it going to be the proportional to the area no, take a look or let me draw the top view.

So, if this is the top view of the capacitors, this is the top plate this is the bottom plate, I looking from the top over here, fringing happens in this marked reason only at the borders, that is where the fringing happens. So, what is the extra fringe capacitor going to be proportional to the parameter, so can my formula look like epsilon times parameter divided by d is it possible, dimensions it cannot write, this has dimension of epsilon. Whereas you want dimensions up ends epsilon time length A epsilon by d, instead you got parameter epsilon by d you cannot be.

So, this got to be another factor over there which is units of meters, what else could it be proportional to take a look, it is now proportional to the height, charge will also come on to the side remember, there is no bulk of the area, but they could be charges on the walls. So, charge will not only resign on the lower wall the roof, the ceiling charge will mostly resign in the ceiling it will also reside on the side walls; so it is also going to the proportional to height, this not height this thickness.

Now, could this be a formula, well the dimensions are right, the proportionality is right intuitively however, it is not really the case see, in this case the fields line curving, they are not coming straight this put have be correct to the coming straights, this things the fields line are curving towards the other plate. So, on top of this there is going to be the effect of the factor they are curving, so effective distance between the two plates, is more than the distance, so there is going to be some first factor over here.

So, this is the capacitance that extra capacitance that you get because of fringing, so if you want to match two capacitors, you want to make sure the two capacitors are equal. Then what have to you do, you have to makes sure that there areas are equal, you have to make sure that they parameters are also equal. If you want to make one capacitors double the other, then you have to make sure that the area is double. as well as the parameter is double, it is not easy to make sure that both area and parameter are double.

So, if I have l 1 and w 1, then for the second one this is the area relationship, there also need to be a parameter relationship which basically tell you that l 2 plus w 2 twice of that is equal to twice of l 1 plus w 1. So, you have got two equations, two unknowns you can solve for l 2 and w 2, this is unique answer to do this, so if you want a one capacitors to be n times the other capacitors, then there is the unique relationship. And it might not be easy to make this, but be where you can also just put two of them, you can put two capacitors each of size A 1. And then, you get basically get that advantage of both are dabbling and parameter dabbling, that is also possible way to constant, now how do we need capacitors on an IC.

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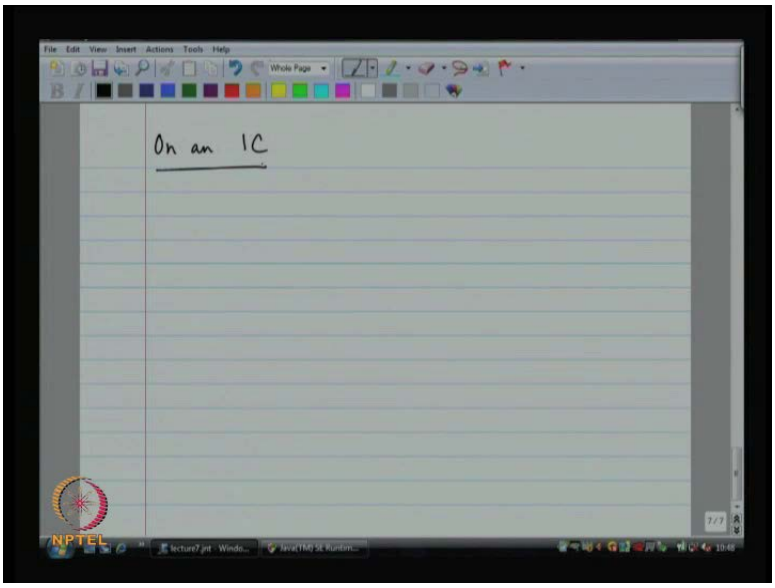

So, what we have learn so far is that the area of the capacitors is important, the fields lines now do not have to go straight anymore, the curves towards the other plates specially at the edges, this effect is called fringing you might have heard of this. So, along the border of the area of the capacitor there is fringing, so the fringe electric field curves to the other capacitors, so this also I am sure you are familiar with.

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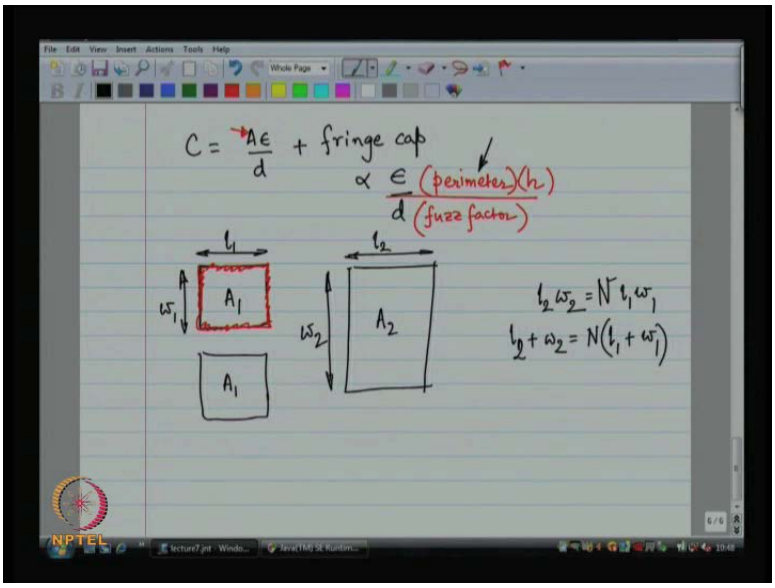

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So, this got to be another factor there which has units of meters, what else could it be proportional to ((Refer Time: 31:56)), take a look it is now proportion to the height, charge will also come on to the sides, remember there is no charge in the bulk of area, but there could be charge in the walls. So, charge will not only resign on the lower wall, the roof, the ceiling charge will mostly reside in the ceiling, it will also reside on the side walls. So, it is also going to be proportional to height, this not height this thickness.

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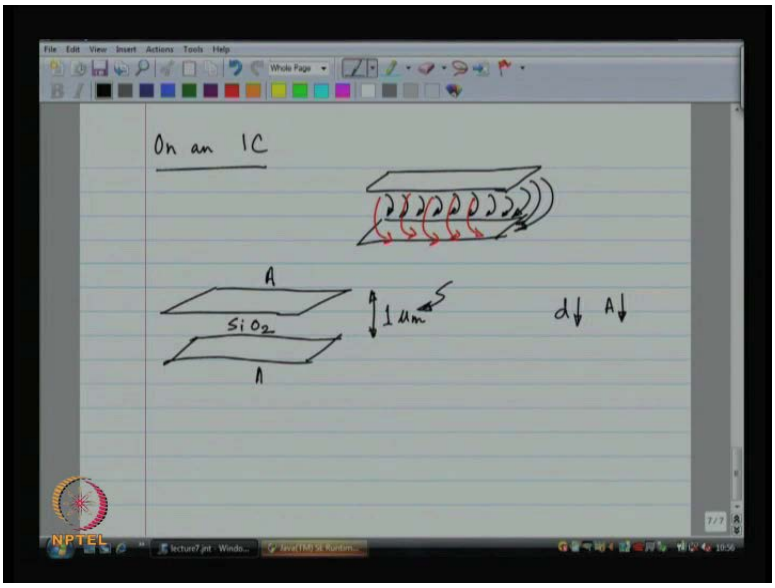

So, what we have learn so far is that, the area of the capacitors is important, the distance between the two plates is important, the perimeter of the capacitor is also important. One more important thing of note over here ((Refer Time: 37:02)), when do you think the frenzy capacitor is more important than the other A epsilon by d, so let us say this is the normal capacitors.

When is the fringe capacitance, more important than the normal capacitors, look at this when you think it is more important than the normal capacitors, when the height the distance between the two plates is comparable to length and weight of the capacitance. That is when the fringe capacitance becomes very important, if the distance is much much smaller than the length and width, then it is like the frenzies really little bit extra.

Otherwise, when the length and width are comparable to the distance between the two plates, then the frieze capacitance is going to be huge, so if I make a wires, suppose I make two wires. And the distance between the two wires is comparable to the width of the wire, then there is going to be huge amount of frenzying on the sides, there is going to be some, actually not this. Suppose, so there is going to lot of fringing in this case, if you just place two tracks parallel to each other, so usually want a large area.

Now, let us start giving you some numbers, we can use some the distance between two metal layers on an IC, and this could be the two plates of my capacitor. The distance between the two metals layers is a kind of controlled, distance could be as large as 0.1

microns in your latest 28 nanometer process could be as largest 0.1 microns, little older process is it could big as big 1 micron that is a say you are talking about a 0.13 microns process.

The gap between two metals layers could be as largest 1 micro meter, what is the material in between, what is the material in between two metal layers on an integrated circuits, it is silicon dioxide class. So, silicon dioxide is known material, that usually use to insulate all the different material layers, and it has a none dielectric constant the 3.5 also. And you basically make the area, you create area on the top metal layer, you create the area on the bottom metal layer, and you have created capacitors.

Unfortunately this distance between the two plates is not in your hand, it is in the hands of the foundry, so there could be errors in that distance also. So, between process to process, this distance could change between wafer to wafer, this distance could change and as a result the value of capacitance will have errors. I mean it would not be appreciates value, the area is more or less what you want, but the distance need not be what exactly you want, they could also be a gradients in the distance.

So, maybe the foundry did not do what terrific job, and these two plates are not exactly parallel to each other tilted, it still work as the capacitors, so side may be going to like this, I am drawing quite extractor, still works at a capacitor. You will now have to think about the medium distance, between the two plates that how it is, you get what you get, cannot ask for more. Now, some of the modern processor they offer some capacitor called MIM capacitor, so these are special capacitor which are offered in the top metals layers.

And they give you this, they have a controlled distance much lesser distance between the two plates, so if you want to make the capacitor of one pick of ((Refer Time: 43: 29)) let say, if the distance are lesser you would have used lesser area to make it, am I right. If d is lesser, then the area you need to make the given capacitor is also going to be lesser. So, I would like my foundry to give me two layers as close to each other, as possible that will give me the most are efficient capacitor, and area is money in terms of silicon. So, that is why a some foundry, they offer two specially created metals layers, which have lesser area between them, as oppose two regular metal layers. You have to pay extra for that, so I do not know if you are gain in terms of money or not effectively.

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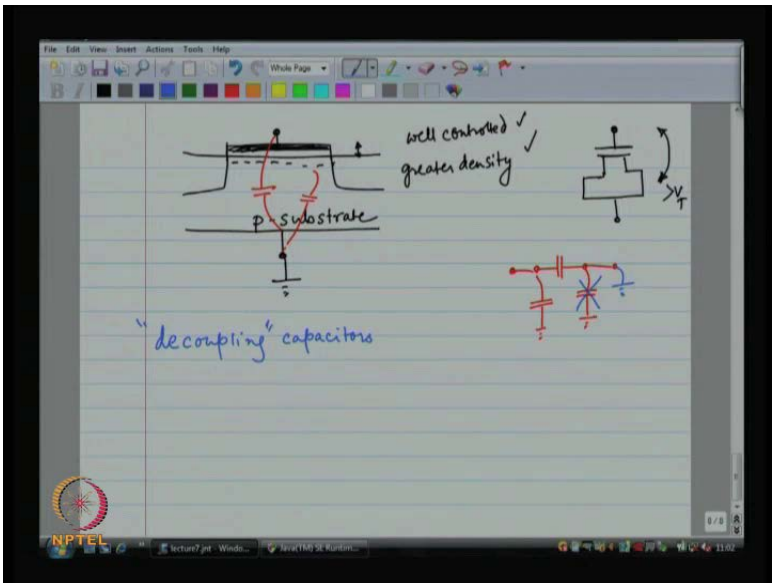

The other well known capacitor is the gate oxide of a Mosfets, so can I use the gate oxide of a Mosfets to create a capacitor, this is actually something which is very very popular. And the reason behind it is that gate oxide, the thickness of the gate oxide of a Mosfets is well controlled and very small, so you get extremely high capacitance density, and you get a much better controlled value of the capstone.

Then, you would get otherwise get if you take two metal layers, so what you have to do is you have to make a Mosfets, you have to use for the gate of the Mosfets as one plate. And the source and drain need to be connected together, and they are the other plate together, this will work only the Mosfets is strong inversion, so this will work when the voltage between this two nodes, is more than V T, roughly speaking more than threshold voltage of Mosfets.

Then the Mosfets goes to strong inversion, then there is an inversion layer of charge basically the second plate, the bottom plate of the capacitors is created only then. And then, you have a nice controlled capacitor between two points, so the drawback of this is that, the advantage are well controlled much greater density. The disadvantage is that you need more than V T is there any other disadvantage, there is the second disadvantage, the second disadvantage is the ground plane.

The bulk of the Mosfets is going to be connect to ground, suppose Mosfets, M types Mosfets, so the bulk is connected to ground it is speech type subtract is connected to

ground. And as a result you get a parasitic capacitance between the top plate and ground, basically you get the parasitic capacitance between top plate and the bulk, which happens to be the ground. So, if you are planning to make of floating capacitors between two points, this is not to way to go, because now unfortunately you are trying to make this, unfortunately you got some parasitic capacitance from the get to the substrate.

You also got some patristic capacitance from the bottom plate to the substrate, so this is what you have built and all of this are reasonably, this patristic are reasonably comparable to the capacitance between the floating capacitance basically, between the gate and the channel. So, this is a drawback of this technique you agree, if one of the naught was ground, if this was indeed ground, then this capacitor does not matter you got a little more capacitance, then you want then you desire.

So, we usually make a lot of d coupling capacitors, we usually make a lot of d coupling capacitors where want large capacitors value, therefore we want great density, because know we do not waste huge amount of area. We also want d coupling capacitors one side of the capacitors is going to be either ground or a constant fixed potential, is small signal it is ground, fix potential is ground in the small signal.

So, therefore, this kind of capacitors is advantages, this disadvantages not there, because capacitors to ground the value of capacitance is not very critical, because it a d coupling capacitor you just want some large massive capacity over there. And you get great density, you just have to make sure that you have more than V T between the get and the drain and source. So, this is very routinely use in d coupling capacitors for other application you, if you want the floating capacitors d where.

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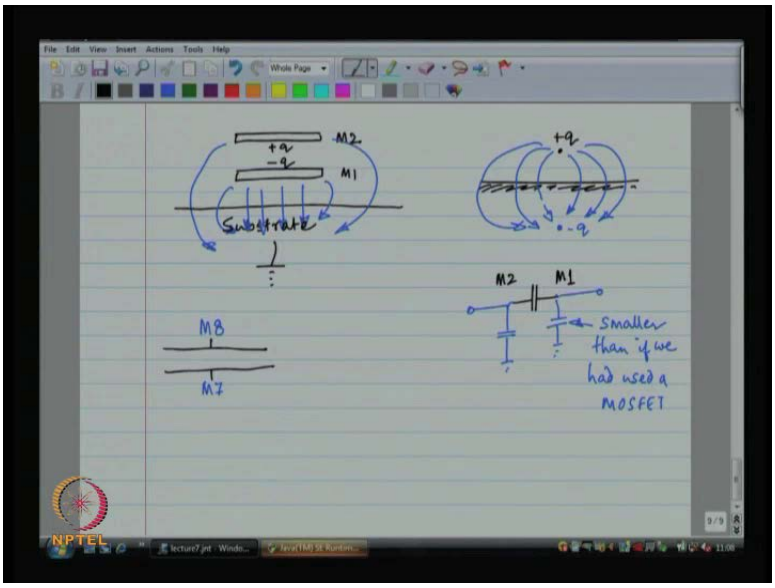

So, if you want a floating capacitor you can use two metal layers, let us say metal 2 and metal 1 is this ok, is this no it is not, because as soon as you use metal 2 and metal 1 you have to remember there is also some substrate. The substrate is connected to ground, and if you place charge minus q, on this plate plus q on the top plate, then a reflection of that charge is also going to a appear in the ground plane, do you remember. Your electro static you have a surface, you put a point charge plus q, it is going to appear as if there is a reflection charge of minus q somewhere over there, and as a result there are going to be fields line between these two charges, this method of reflection or something like.

So, if you have any charge on a top of ground plane, on top of conducting plane you get an equal an opposite charge mini the conducting plane, you do not get the charge over there, it look as a if you got a piece of charge over there. Now, you puts lots of charges each of those charges will have equivalent reflections mirror images, you put a sheet of chargers, you get sheet of chargers in the bottom. So, basically you are going to get a capacitance between M 1 and the ground plane, ground plane is the plate, M 1 is the plate you got a capacitance between M 1 ground plane.

So, effectively what you are going to get finally, you have made a floating capacitor between metal 2 and metal 1, there is going to be a patristic capacitance between M 1 and ground, there is also going to be patristic capacitance between M 2 an ground. So, you got the same old story, as before did you or did you not get the same old story as

before, the same thing. Well it looks the same it just that, the distance between the gate and the substrate is much lesser than the distance between M 1 and the substrate.

The distance between the channel and the substrate is much lesser than the distance between M 1 and the substrate, so these are lesser than earlier, these parasitic search smaller, then if we had uses the Mosfets. Because, there are little further away, so the patristic are smaller however, they are there, so beware they are, there you cannot do anything about them.

So, in that case what else can you do, if you want to make a floating capacitors, what should you be doing, you should be using the top two metals layers not the bottom metal layers. So, if your process are first eight metals layers, you should be using metals 8 and metal 7, as your two plates of the capacitors, so metal 7 is presumably much much further away from the ground plane as metal 1. Metal 8 is much much further away from the ground plane then metal 2, so as the result parasitic will be much much lesser.

If you have a equal spacing between all the metal layers, then you got four times lesser patristic in this case, in the top plate and seven times lesser patristic in case of the bottom plate, so you are really one by the huge margin. So, the idea is go as far away from the ground plane as high up as possible from the ground plane, do not be close to the ground plane, because that is going to create parasitic. What else can you do, can you use the sides, so let us say I am not going to talk about metal 1 only, I am going to draw the top g of metal 1.

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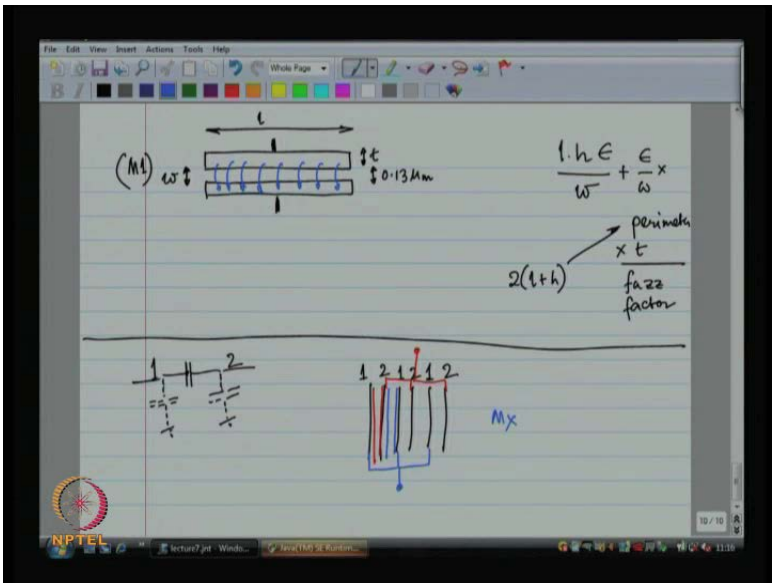

If I draw a track like this in metal 1, and another tack like this both are in metal 1, first of all remind yourself that, let us say in a process technology note of ((Refer Time: 57:40)) 0.13 micron, the spacing between 2 metal layer is 1 micrometer. Process technology node of 45 nanometers, spacing between 2 metals layers probably 0.25 microns, so it is larger, significantly larger spacing between 2 metal layers.

But, in a process technology of 0.13 micron, when I make a metal spacing of 1 micron, I can have 0.13 micron over here, between the two wires, because that is the technology nodes, that is the trace fetes the resolution I have got. So, I can really squeeze the area over there, what do I gain, what the capacitance on this, is this a capacitance, two wires parallel to each other, yes this is the capacitor this could be a capacitor. Basically, I have to think the height of the metal layer also, now the area of this is the length of this track times the height.

And the gap between the two is basically responsible for the distance between the two plates, is there going to be fringing yes of course, there is going to be huge amount of fringing, because now the height is very small. The area has two components with on the length a height and the length the height is comparable to it probably, so there is going to be fringing this going to be fringing on the over the top, and under need the bottom.

So, make sure that the there is fringing, but fringing is not bad I mean just adds component, so as long as the height, you can compute the fringing factor, the first factor

over there. And you can figure out for yourself, what is going to be the capacitance value, what is the perimeter here, the parameters is twice l plus the height of the metal. So, you can basically put two wires parallels to each other and that gives you a capacitance, you will surely get much better capacitance densities then before, because what now can really squeeze down the gap between the two plats.

So, a lot is in the hands of the foundry, so the height is in the hand of the foundry, a earlier gap between the two plates was not the hands of the foundry, now the height is hands of foundry, what else you have to simulate the first factor. You have to know that what the first factor is basically its depend on the geometry, so how do capacitors like this look, so let us say I want to make capacitors between 1 and 2. What about parasitic to ground, both of these will have equal patristic to ground, they are equally far away from the ground plane whichever layer, metal layer they are in.

So, if you use the top most metal layer, then they have equal parasitic to ground, but lesser, so beware that they have patristic two ground. As long as aware of that you make your design, in this case they have equal parasitic to ground, in the earlier cases metal 2 had less patristic to ground then metal 1. Metal 8 had less patristic to ground then metal 7, so how do capacitors look like finally, you could make parallel plate capacitor look like that. So, now you get double, you not only get advantage of this interface, you also get a advantage of this other interface. So, effectively your even for the double d capacitors density, these are commonly use techniques, what people further do is let us say this is a metal x on metal x plus 1, they have another set up these with the opposite configuration.

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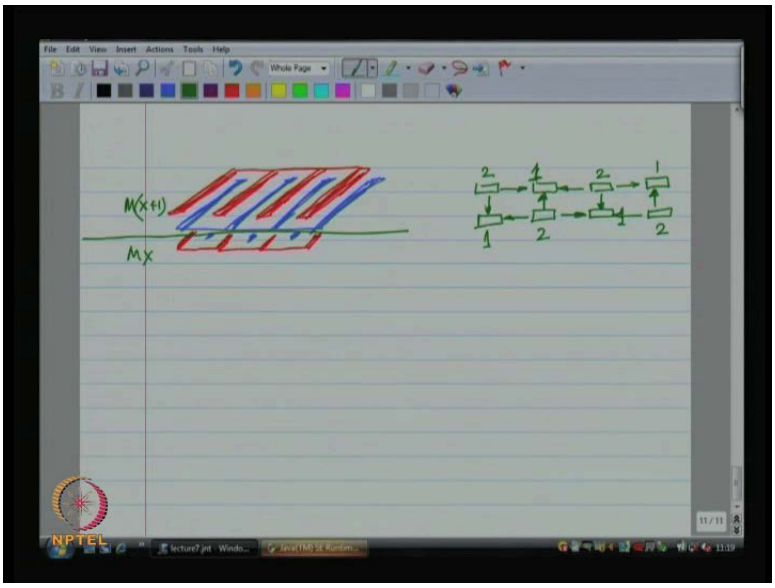

So, now I am going to draw a 3 D picture for you, so I am not sure if is it clear, but so on the higher layer, so this is metal X plus 1 and this is metal X, so an metal X plus 1 you do this finger capacitor and on metal X, we need that you do the exact opposite. So, now not only do you get the side walls for your capacitors, you also get the surface area of the capacitor, so this is the cross section. So, you not only get this capacitance, you also get this capacitance, so we will stop here, we look at couple more capacitor configurations, and we will continue with the next lecture.

Thank you.