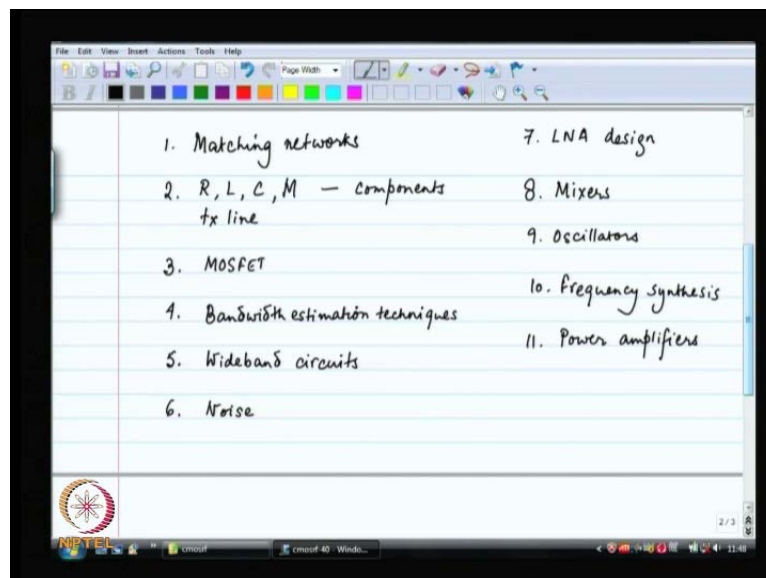**CMOS RF Integrated Circuits**
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Lecture - 40
Course Summary and Conclusion

Hello and welcome back to CMOS RF integrated circuits. Today is a fortieth lecture and we have finished all the requirements of this course, and in this lecture I am basically going to discuss, give you a broad course summary and conclude the course, basically that is my plan. So, these are all the different items that we are covered.

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We have we started of this course with matching networks then, we discussed what are all the components that are available to us on an integrated circuits. So, we have registers, capacitors, inductors, mutual inductances lot of times transmission lines. So, these are all the different components that are available to us. We discussed at length about all of these components, we discussed transmission lines at length. Why we need impedance matching? I will come to the details, I will just broadly mention what are the different chapters or models we covered then we talked about the MOSFET. MOSFET is the core of CMOS. So, it is in the title, we cannot get away without the MOSFET.

Then, we have worked on bandwidth estimation techniques; method of open circuit time constant, short circuit time constant. Actually; we just worked away open circuit time

constant. Then, we worked on techniques to make wide band circuits, after that we worked on noise, when we worked on designing a low noise amplifier then, we worked on mixers. Along with mixers we also discussed some architecture, modern radio architectures, heterodyne, super heterodyne, homodyne and so, on. Then, the next phase we discussed oscillators then, frequencies syntheses. As part of frequencies syntheses we also worked on phase lock loops and then finally, we discussed power amplifiers. So, let us take one by one, let us go back.

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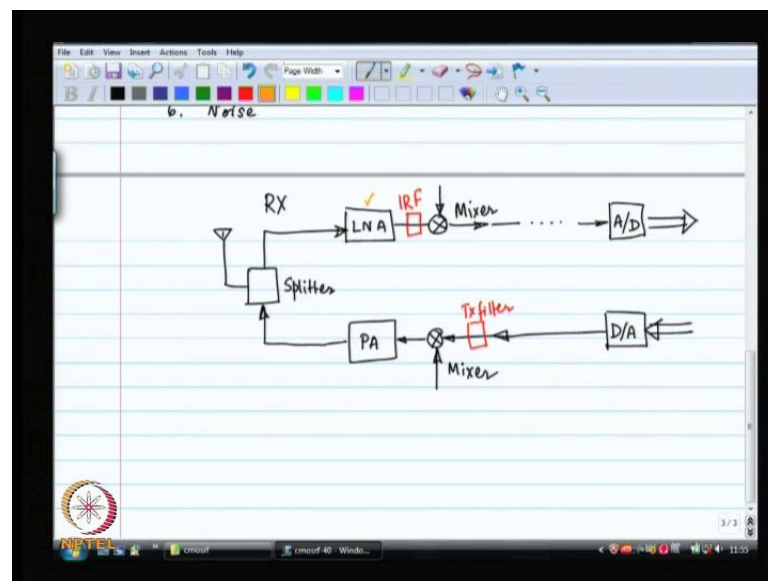
I want to take a holistic view of this first of all the radio architecture. Let us go back and see we have covered all the different component. So, there is the antenna. So, transmit and receive antenna, at the same time I promise that I would not covered antenna I did not. It is a course by itself, working on the antenna is the course by itself we did not do anything. Then, there is some sort of a splitter or a circulator or whatever you want to call it. So, this is the general architecture; we have a splitter at RF frequencies, it splits transmit path from the received path.

Now, if you are working on something like C D M A; code division multiple axis, where both the transmitter and receiver or on all the time then, this splitter is something which is extremely important, because transmit the received path are active at the same time. If you are working on time division multiple axis systems like; for example, g s m or for example, y max, y max is mix up of a lot of different things. So, for example; in y max

and in g s m the splitter is not really that important, because in the transmit chain and the receive chain are not on at the same time. When the, transmit is on the, receive is definitely off, when the receive is on the transmit is definitely off.

So, the architecture is of the communication protocol itself determines whether the splitter is something which is very relevant or not. In any case the splitter is not was not discussed in this course at all. Now, as far as the received chain is concerned; the first most important block is the low noise amplifier. Why is the most important block, because; the figure of the low noise amplifier determines the sensitivity of the entire receive chain more or less, is the low noise amplifier gain is significant than the figure of the low noise amplifier is all that matters, right. So, if you build good low noise amplifier that is all you want that is all that matters as for is the receive china is concerned a good low noise amplifier. There are other things that matter will come to there.

So, the low noise amplifier is something of great importance, as far as sensitivity is concerned that is one of the most important blocks in the receive china. The next block I have shown in red or shown I RF standing for I image reject filter. So, this image reject filter we did not really going to filter design and so on and so forth. But image reject filter could possibly we made up of a passive network capacitors, inductors, registers and so on. You can contemplate making or the I R filter using passive components, it précised the mixer in case your system is heterodyne or super heterodyne. If you are making a homodyne system, direct down conversion then, the image reject filter is of no relevance. We do not need there is no image the image is the signal. So, you do not need to reject anything right.

So, this image reject filter is something very important if you are talking about heterodyne systems, frequently we do broadband a communication protocols like y max W C D M A, when the data rate it is large right. Typically these are wide band because the data rate it is large we need large bandwidth. And, when you need large bandwidth the DC off set problem is not a problem anymore because the DC is a very small part of this broadband signal. Now, when that happens we preferred a designing a Dirac down conversion receiver, because; Dirac down conversion is otherwise easy to build, the only stumbling block that Dirac down conversion is the D C offset.

The DC offset is not critical if the data rate is large, when the data rate it is large typically we have a wider band, you need go back to Shannon. You need so much bandwidth for support such data rate, right that dictated by Shannon. Anyway so, when the data rate it is large you need larger bandwidth, if you have a larger bandwidth then the DC really DC is a very small portion and very narrow portion qualitatively of a larger bandwidth. As a result of DC offset problem is no longer very significant, even there is a DC offset, even if you do make a mistake as for as DC is concerned. DC and frequencies around DC are concerned it is not going to affect you much, it is going to degrade little bit that is not going to decrease your R that is not going to increase your B terror rate significantly, right.

So, that is the basically the idea. So, when you have these high data rate communication protocols like y max and WCDMA, we prefer building Dirac down conversion receivers. When you have holder protocols which are very narrow bandwidth low data rate for example, g s m low data rate; what is the data rate? If you use GPRS or edge probably GPRS I think is about 30 kilo bits per second. That most is not going to be much more than that. So, that is very low data rate, the bandwidth of a G S M signal is something like 100 kilo hertz right.

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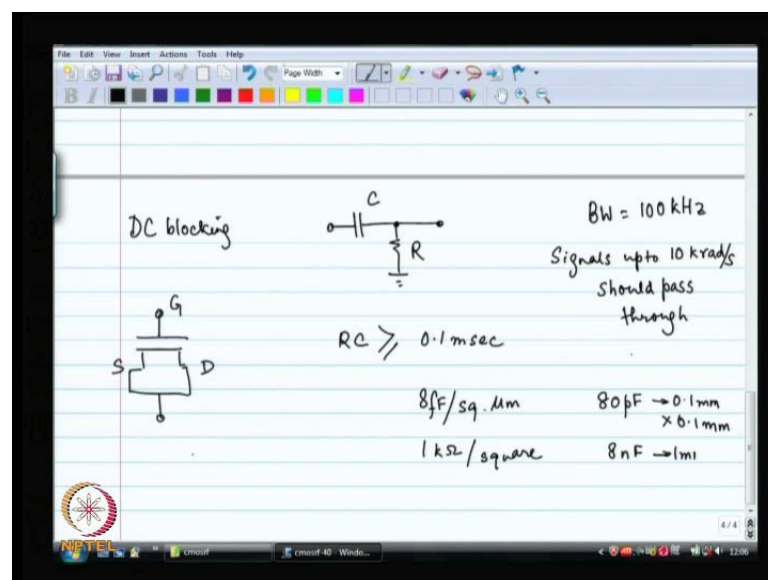
So, we that kind of bandwidth; DC is the significant portion of that, it is hard to reject DC and not, reject the signal of itself. How do you reject DC? You put a DC blocking

capacitor right, now the thought is this when you put a DC blocking capacitor that by itself is not, enough actually have to put a high pass filter to block on DC, it is C R network.Now, you put a capacitor, you put a register to lower the cut-off frequency of this. So, this is high pass filter, this high pass filter will do a good job in blocking out d c, but you want the cut-off frequency of this to be significantly lower than your signal bandwidth, right. You do not want it to cut of things other than frequencies other than DC as well agreed.

Now, let us say that your signal bandwidth is 100 kilo hertz. Now, 100 kilo hertz means you most probably want signal up to 1 kilo hertz 1 percent of 100 kilo hertz. So, pass now if you want signals of to 1 kilo hertz to pass. Let us make it will little easier let us say instead of 10 kilo hertz, I say 1 kilo hertz, I said 10 kilo radians per second. It is going to make my mathematics little that easier. So, that means; that this R C product has to be equal to or greater than equal to, great then equal to 1 by 10 k, which is 0.1 millisecond. So, R C time constant has to be more than point one millisecond for this to work successfully, for this not block out signals beyond 10 kilo radians per second, 10 kilo radians per second something like 1.5 kilo hertz.

So, R C time constant as to be more than 0.1 millisecond. Now, typical values of capacitor are what, what is the capacitor that you can build easily on a chip, on an I C. On an I C the density of capacitances that you can build for example, if you use the gate oxide of a MOSFET, you got the gate. And, if you connect the source and drain together remember; we talked about these capacitance action also, this is the where we study the MOSFET in fact, right. So, you have got a thin oxide layer in between and that is separates that gate on the channel and that is your capacitance Seahawks, I mean; density Seahawks density times the width times the length. So, typical Seahawks density is could be something like that 8 Femto farads per square micron, which means; that if you want to build 8 Femto farads. 8 into 10 to the power of minus 15 farads then, you need 1 square micron, all right.

Registers you can use some high resistivity poly silicon etcetera special or special masks and so, on. You can get resistances of up to 1 kilo ohm per square, normally this is vary larger number that I have put over there 1 kilo ohms square is quite high. Typical poly silicon resistivity as much lower they will be around 30 ohms was square is and so, on. 1 kilo ohm per square is with special in plans, right. Now, let us say you make a resistance

of 1 kilo and you make a capacitance of 10 pico farads, 8 let us say 80 pico farads. 80 pico farads means; I need 10,000 square micron mean, I am going to use 0.1 millimeters 0.1 millimeters that is a large amount of area. 0.1 millimeter by 0.1 millimeter that is a very large amount of area that we are used up in building 80 pico farads capacitor is 80,000 femto farads. So, 10,000 square microns so, 100 microns by 100 microns so, that 0.1 millimeters by 0.1 millimeters that is fairly large sized capacitor, right.

If you want make 8 nano farads that is 1 mm by 1 mm that is almost the size of your whole chip, right. If you are making 1 mm by 1 mm chip that is all that you have your going to get 8 nano farads. Remember, the product of the register and the capacitors as got to be more than 0.1 millisecond, right. So, this is basically the stumbling block that I got an area. Area is the very basic stumbling block, when it comes to making Dirac down conversion receiver you got to block out DC, the way to block out DC is by using the high pass filter like this. And, high pass filter by this like this is loops easy on papers, but; when it comes to making components it is impossible to fit the components inside, integrated circuits.

So, even when you make 8 nano farads, even then, you got to realized that you have to make about the mega ohm of mega ohm worth resistance, right. So, that is large register that you still have to make even that is going to cost you the large amount of area. So, basically the thought is do not make Dirac down conversion receiver when the bandwidth is less. When the bandwidth is more than the bandwidth is 2 mega hertz 20 times this the requirement as for as the high pass filter cut off goes down and then you go for the Dirac down conversion receiver. So, all this we talked about to explain why I need this image reject filter in the receive path? Then, there is the mixer we talked about the mixer right. Of course, you have in phrase and quadrature phase signals. So, you have to make a quad mixer rather the quadrature mixer, right. And, the quadrature mixer, there are several architectures that you can pick up.

This is the viewer architecture for example, are you can use the viewer architecture and a build a quadrature mixer. Now, for the mixer to work you need to have, for the quadrature mixer to work you need to have 2 oscillators; 1 giving the sine and other giving a cosine component, agreed. So, you have to make a quadrature frequency synthesizer as well, did we discussed a quadrature oscillators finally, I told you that do not let get me away without telling you how to make it. Well, it is easy one very popular

way of generating I and Q component is to really designing oscillators for double the desired frequency. And, then use flip flops to generate 2 phases or 4 phases that you need, we need 4 phases 0, 90, 180 and 270 degrees, right.

These 4 phases can be easily generated by module of 4 counters I am sorry, model of 2 counter right divided by 2 counters you can easily make one of these and you can generate the 4 different phrases that you need, right. So, the thought is instead of generating f naught, using the, why do not we generate twice f naught using an oscillator or frequency synthesizer. So, then we got into the whole business of frequency synthesis and study frequency synthesis we first talked about P L L s phase lock loops in quite a bit of detail.

So, the way we approached phase lock loop we would not find it in the books normally and this is not about the books talk about. They talk about it in very different approach did do not give you the control theory of approach on unfortunately. So, we build a phase lock loops it is a velocity control system. So, we need 2 integrators; one integrator is given by the oscillators itself, the second integrator is should be there as part of your loop, loop filter or as part of your controller. Unfortunately, when you have 2 integrators just 2 integrators by itself, the system is never going to be stable. So, to put in stability you have to putting a zero and the pole right, one after the other. You got 2 poles at DC and then a zero and then another pole. That finally, what is going to be stable that is part we bit? So, the loop filter is made out using a charge pump. So, it kind of integrated with the phase detectors, phase detector is really a digital block it contains 2 flip flops and this is how we build phase lock loop.

Now, frequency synthesis is just an extension of the phase lock loop, you put a phase divider in feedback, right. How you do a phase divider is fairly straight forward if you want to divide by integer are you make, is divide by n counter model n counter. And, that is going to work fine, to do division by m. Now, there are special ways to make these dividers. So, I am would encourage to look at the books the basic problems over here is that the logic circuits have to work very fast. So, you cannot really make your statics CMOS logic circuits and get away with it. You are doing a division at RF frequencies right. So, your logic circulars really have to work hard.

So, there are very efficient ways are doing this division and for that I recommend that you take a look at the literature. You did not really discuss these techniques in the class. So, I will be giving the pointers, there are the pointers in the in the notes for the corresponding lecturer. Then, we discussed fractional synthesis. So, the problem with integer division was that the loop bandwidth is very small; there are also these spurious frequencies that are being generated. And, the spurious frequencies thankfully or outside the loop bandwidth which means that they get filters.

So, the basic problem with the integer n synthesis technique is that the loop bandwidth is small. Loop bandwidth is small means; that the VCO oscillators that you have built as to work harder in terms of its phase requirements. It can track the reference oscillator weekly only within the bandwidth it tracks the reference oscillators. So, outside the loop bandwidth it has to have very good phase noise characteristics of its own. So, this is one big problem, the second big problem is the settling time. If the base station asks you to jump from frequency A to frequently B now, unfortunately you are too slow because your loop bandwidth is very small.

So, this pushed task to make these fractional dividers, the way we did fractional dividers was; the first technique was some sort of pulse width modulation. Let us divide by n number of times, let us divide by n plus one sometimes, right. And, on the average we are dividing by number in between n and n plus 1. Then, we discovered that this method is even disperse then, the integer n synthesis, as far as these disperse are concerned, because now I got a larger loop bandwidth I can settle foster. But the spurious frequencies are appearing at the exactly the same frequencies as before and they are going right through the loop. So, they became an unfortunate problem.

So, then this encouraged us to randomize the division by n and division by n plus 1. And, the way we did it that was by asking a sigma delta modulator to tell as when to divide by n and when to divide by n plus 1. So, that was the story as for us frequencies synthesis course then. So, these frequencies synthesis techniques applied to both the, transmit and receive path. Typically what happens is that you make one frequency synthesizers and somehow generate both the, transmit and receive frequencies employing the same frequencies synthesizers, same feedback loop. So, this is typically what the idea is that you do some kind of modulation in mixing in between so, that you can generate both the, transmit in the receive frequencies in one shot. Will have of course, will have 2

oscillators necessarily; or you could one oscillators and have 2 divisions that is also, possibility.

It is usually the case that you need 2 oscillators. Now, when you have 2 oscillators on the same chip there are there is the problem of pulling, it is called pulling. The oscillators tend to pull each other towards themselves. So, if you want to generate f 1 and f 2 on the same chip is f 1 and f 2 are close to each other then, invariably what is could be happens is f 1 and f 2 the 2 oscillators will 0 in, and then generate the same frequencies. So, this phenomenon is called VCO pulling. Other terms for this phenomena in or injection locking is very broad term, I mean; if the same phenomena that is happening it is not this is not really injection locking.

They might not end up locking to each other; they might just pulley each other, towards each other right. They might not lock with each other when it when they do lock just next step when they do lock it is called injection locking. So, injection locking is again something which you seen the lot of systems. If you, for example; 2 grandfather clocks on the same wall then, after sometime you are going to see that they are oscillating to gather in phase with each other. So, this is generally called injection locking, injection locking is also technique which can be used to generate quadrature phases.

So, once again I will point to reference for that we do not have the bandwidth discuss all of this in this course, right. So, that is also one reason; why are you would be encouraged to generate both the transmit frequency and the receive frequency, the transmit and the receive a loss in one shot you may using the same synthesizers. So, that the frequencies are ratios of each other again, I will point you to a reference for this, and then finally; we did the splitter, I am sorry finally, we did power amplifier now, as for as the power amplifier is concerned; we discussed class A B C D, class A B amplifiers, right. And, pulse width modulation type amplifiers now of these class A is very linear, but efficiency is very bad. Class B is quite non-linear, so non-linear that you cannot really use it in your modern RF system.

So, typically what we do is we use something like A B amplifiers. And, then we put a feedback loop around it to make sure that the linearity is not compromised. And, other way to improve linearity at is to do back of. So, you design power amplifiers to broad cost 1 watt power, but then, you do not really use it at the rated power, you use it 20 dB

below that. So, instead of broad casting 1 watt of power you broad cast 10 mille watts of power. Now, 10 mill watts of power let us say. So, it is like this that the second and third harmonics and then inters modulation.

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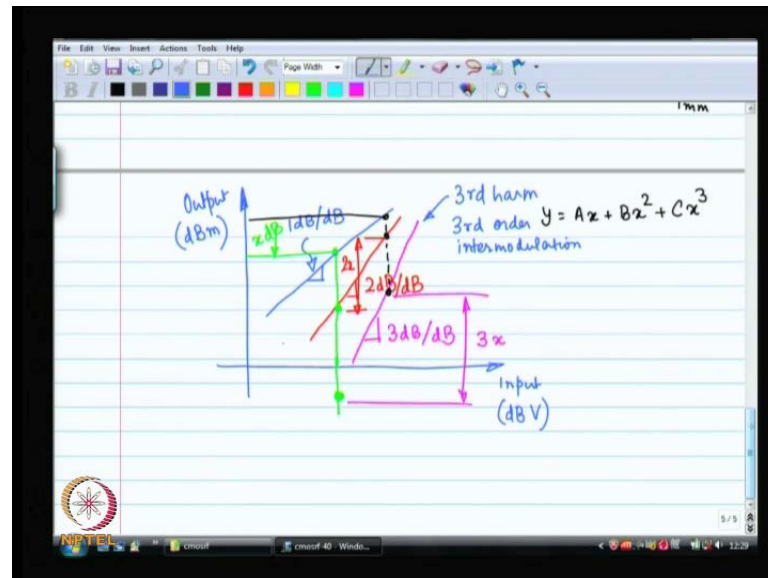
So, I am going to plot the input on the x-axis, and the outputs on the y-axis both are in the decibels with respect to volts are you want powers. Let us put d B m in the output decibel with respect to 1 mill watts. So, let us say this is the slope as for as the, this is the curve as for as the fundamental component of the power amplifier is concerned, this is the curve. So, looks fairly linear to you unfortunately, if you look at the second harmonic, the second harmonic is always going to have a higher slope. And, the third harmonic is always going to have an even higher slope. Now, the slope for the fundamental is going to be one d B for d B. So, if I increase the input by 1 decimal the output is going to increase by 1 decimal.

That is your state forward for polynomial, right. Let us say this is the polynomial that you are power amplifiers y equal to A x plus B x square C x cube something very general sum do the curve fitting and fit you are power amplifier to this particular polynomial. In that case; if x increases by 1 decibel y will also increased by 1 decibel as for as the fundamental component is concerned. x square is not going to give you the fundamental is going to give you the third of harmonic am sorry, the second harmonic, right.

Cosine squared is basically cost 2 theta cosine square theta is cost 2 theta and DC and 1. So, x squared if x increases by one decibel then x square is going to increase by 2 decibels. And, therefore; the second harmonic is going to increase by 2 decibels, and then if you look at x cube cosine cube x is cosine, cosine cube is basically; cosine cube theta something times cost 3 theta plus something else times cos theta. So, cost 3 theta is going to increase by a lot. So, if I increase the amplitude of x by 1 dB, 1 decibel then the amplitude of cos 3 theta is going to increase by 3 decibels. So, what you are going to find is that the third harmonic goes up by 3 decibels, all right. So, therefore, if I design my power amplifier to work for an output power of 0 d B m let us say or let us say I design my power amplifier to work for power of 1watt.

But then, the other 1 what output power, I get so much of second harmonic and so much of third harmonic, I really do not want to get so much second and third harmonics. So, I back off from my rated power by 20 d B; let us say 20 d B. So, if I back off from the rated power by 20 d B then, second harmonic as gone down by 40 d B. And, my third harmonic as gone by go on down by 60 decibels. So, this is typically what I mean by back off, you design your power amplifier for certain power and then you back off from their then reduce the distortion harmonic. This is very straight forward it is used all the time and a top of we used feedback and as a result you are going to get very linear nice power amplifier, all right.

The third harmonic and second harmonic are not really that important to us, we are going to filtered them out anyway, what is more important are the inter modulation products. What you will realized if you do the mathematics is that the third order inter modulation product 2 f 1 minus f 2, 2 f 2 minus f 1 these third order inter modulation products also follow the same curve as 3 d B for d B. Second order inter modulation which is not that important f 1 minus f 2, f 2 minus f 1 right, is the same thing. Second order inter modulation is going to follow the red curve 2 d B for d B. Third order inter modulation is going to follow the pink curve 3 d B for d B. So, that is really something that is of concern third order inter modulation product.

Now, we go back and this is basically the course all the lectures that we went to be studied power amplifiers, frequency synthesis, oscillators mixers, we did some low noise amplifiers, right. So, this is as for as the building blocks of the RF system as concerned, but before that to work an all of these we did some we studied some of these tools. The

first tool that we studied was matching networks Q of a network for something which we discussed at length. How to convert series L R network to shunt L R network, how to convert a series R C network to a shunt R C network and so on and so forth.

Then, we discussed the transmission line, actually; we are discussed the transmission line somewhat before is the matching networks because I needed to motivate the matching network, why we needed matching. Then we did the transmission lines, we did we discussed each and every component that is available on a chip individually, right. The resisters, inductors, capacitors, we also talked about mutual inductances, resisters are easy to build. Not, always of use in L N A is we typically avoid using registers in known as amplifier inductors are frequently used in low noise amplifiers. Capacitors of course, are used everywhere and mutual inductors also coming handier times.

Then we talk about the MOSFET we wanted to the details small signal model of the MOSFET out each and every element in the small signal model is relevant as for as your concerned. Then, we studied bandwidth the estimation techniques using the method of opens and shots circuits time constants. We did wideband circuits where we treated of delay to get more bandwidth. So, typically the trade of is let us trade of gain and get more bandwidth, but you do not always want to trade of gain to get bandwidth, you can also trade of delay and get more bandwidth. So, that is what we are talk about then, we also studied noise, ones we did all of this then we went into it. The real circuits like lionize amplifiers mixers oscillators all right.

So, please post feedback for the course and ask questions on the forums and it is also important that you refer you read the references that are listed out the each of these chapter. Because a lot of material has not been covered, a lot has been on said in this particular course. So, by no means in this course complete what I am trying to suggest is please take a look at the different references that have been made available. And, follow the techniques, follow the discussions there, because at the end of the day if you want to build a modern wireless system, it is going to take a lot of effort is not something which is very easy and which will top out of a textbook.

Thank you for your attention.