CMOS RF Integrated Circuit is
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Module - 11
Frequency Synthesis
Lecture - 36
Delta and Sigma Modulation in Fractional Synthesis

Welcome back to CMOS Radio Frequency Integrated Circuit is, today is lecture this is we are discussing fractional length frequencies synthesis. And as part of fractional n synthesis, we figured out that spurious frequency are a big problem and we needed to rethink and redesign the frequency divider circuit. The technique we needed to revisit that, so this is all part of the 11 th module, Frequency Synthesis.

So, this is what we were working on in the last class, we said that we are going to take a pause in our rethink and revisit ((Refer Time: 01:14)) of the division circuit. We need to generate some sort of, pulse width modulated signal that is our business. And we are going to pause over there and we are going to take a look ((Refer Time: 01:28)) something probably from a different course.

We will find this in a course, which discusses A to D conversion, Analog to Digital conversion is called a sigma delta or delta sigma modulator. And it is not very difficult, this is basically a feedback control system, negative feedback control system. And negative feedback control system, if the loop gain is large then, the output is equal to the input, that is basically big idea. If the loop gain is large then, the output is going to be equal to the input, the error signal is going to be equal to be 0.

So, we are going to make this loop gain large at low frequencies and small at high frequencies. So that, at low frequencies, the output is definitely equal to the input, at high frequencies the output has nothing to do with the input, so this is our plan. And why did we put this high frequencies business at all, we could have made, let us make the loop gain high at all frequencies, would that be good, no that cannot possible be. Because, this quantization noise has to go somewhere, our plant and like other plants.

Our plant over here is the plant that adds noise, it is of course, analog to digital convertor, probably a 1 bit A to D convertor. In fact in our particular case, we are going

to apply the 1 bit analog digital convertor and it basically introduces quantization noise. Now, this quantization noise has to go somewhere, so that is why we made this high pass, low pass business and we said that, let us allow the quantization noise go through at high frequencies.

We are going to focus on the low frequencies, now you could built alternate systems, where you could make the band pass edge, band pass loop filter. And say, that allow the quantization noise to go through at other frequencies, but only in this small band of frequencies, I want my signal to go through, it is up to you, this is all yours. So, these are all different kind of designs, you can design the low pass sigma delta, you can design the band pass sigma delta, etcetera. So, you can study all of this in your A to D conversion classes.

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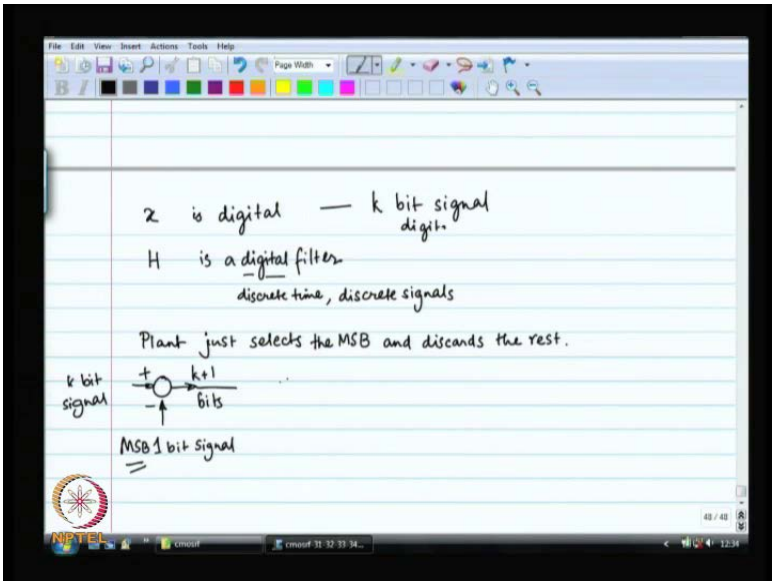

For our purpose, let us see what happens, if first of all x is the digital signal, what are we doing in A to D convertor class, x is already digital, does not matter. Let us say x is digital and it has lots of bit is in it, so x is a number like 0.1, 0.2, 0.3, let us say that number is represented by k bit is, then, the loop filter H is what is the loop filter it is a set of adders multipliers delays. So, it is a digital filter by digital I mean that it has bit is as input, so it is not just a discreet time system it is discreet time and digital.

Al the plant that we have what we called an a 2 d convertor is nothing, but something that selects the MSB and throws out everything else. So, the plant is just one wire the

order of course, this particular adder that I have got we have to be little careful about this you have got k bit digital signal over here you have got 1 bit signal over here, because the plant has selected the MSB and discarded rest, so the plant is 1 bit. So, the feedback signal that is coming back is 1 bit signal, so this plus minus signals you have to be little bit careful this is the MSB this subtraction part you are subtracting the MSB paired with 0.

So, it is not just subtracting that 1 bit signal it is subtracting 1 bit signal that has the most significant bit anything else that, you have to worry about how many bit is are there here k plus 1 bit is. Just in case there is some over flow there is some problem because, the MSB both have MSB that is why just to keep some space, you keep k plus 1 bit I think this signed system is there sign is this a sign addition sign subtraction are these all unsigned numbers. What do you think can I work with sign I could work with the un sign think about it and you do not have sign atoll I can just work with unsigned numbers and do the job, so this is my basic story that I am going to have k bit digital signal as my input. So, it is not just sigma delta from A to D convertor book it is a sigma delta suited to our needs.

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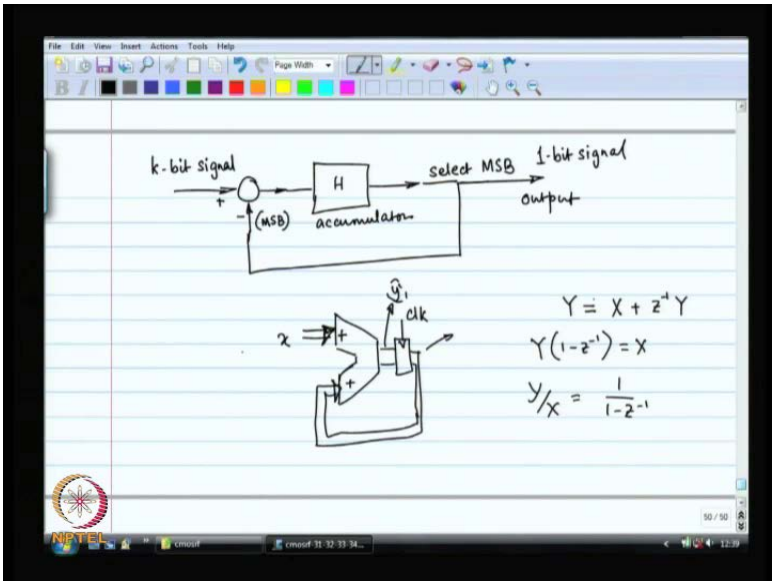

The output is the 1 bit signal and the claim is that the average of the output. So, suppose the H is the filter which has very high gain at d c infinity high gain at b c and low gain at other frequencies does not matter what the gain is at other frequencies, what at d c it is a

very high gain infinity high gain, so typical structure could be an accumulator what is an accumulator something look like this. So, every clock cycle it is clock of course, every clock cycle it takes the previous one and it adds and sends it out.

So, you could clock, you could tried in this fashion are I think what people would prefer is you put set of flip flops, register, guest law at the output of the add it. So, every clock cycle you take the previous output and add it to the new output add it to the input that is going to the new output. So, this has the transfer function of let us say this is y this is x, so that means that these are all z domain at this is the transfer function of kind of this system.

Now, if you pick y from here you got this if you pick y out of this 0, then you got the delayed version of that, so you will get z inverse by 1 minus z that is the only difference. Now, if I have such a scenario then in the presence of the overall feedback I am going to assume that there is some quantization noise, because of selecting the MSB and regarding the rest quantization over their next selected the MSB thrown out the rest of the digit you have quantized you have number to certain to discreet possible levels. ok

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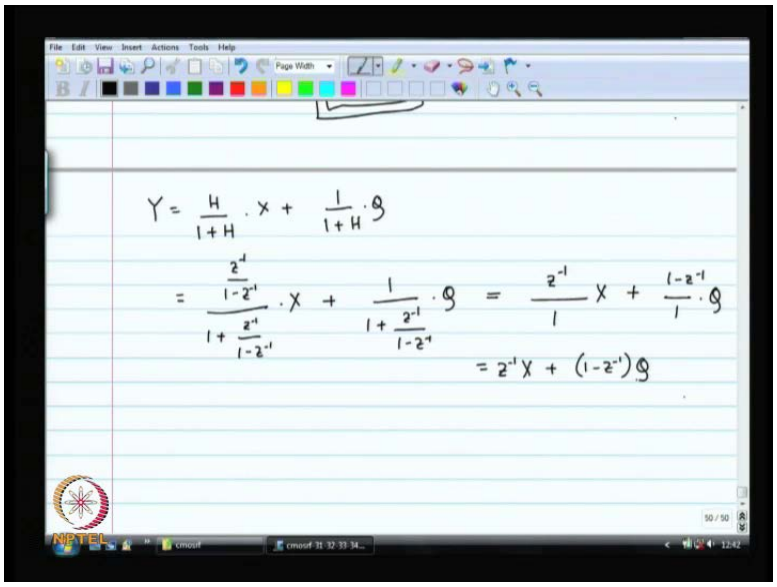

So, this is your H now of course, I do not want really to call this x and y I would rather call this e and y hat now, y I know is equal to H by 1 plus H times x plus 1 by 1 plus H times q and H is 1 h is either 1 by 1 minus z inverse or z inverse by z. So, that makes it let us say H is z inverse 1 by minus z inverse I am going to do what is suit is me best

now multiply denominator 1 by z inverse. So, you have got z inverse in the numerator and the denominator you have got 1 minus plus z inverse which is 1 times x plus again 1 minus z inverse in the numerator divided by 1 times q. So, you have got z inverse x plus 1 minus z inverse times q what is this it is the previous value of x plus the difference of the last 2 values of the quantization noise.

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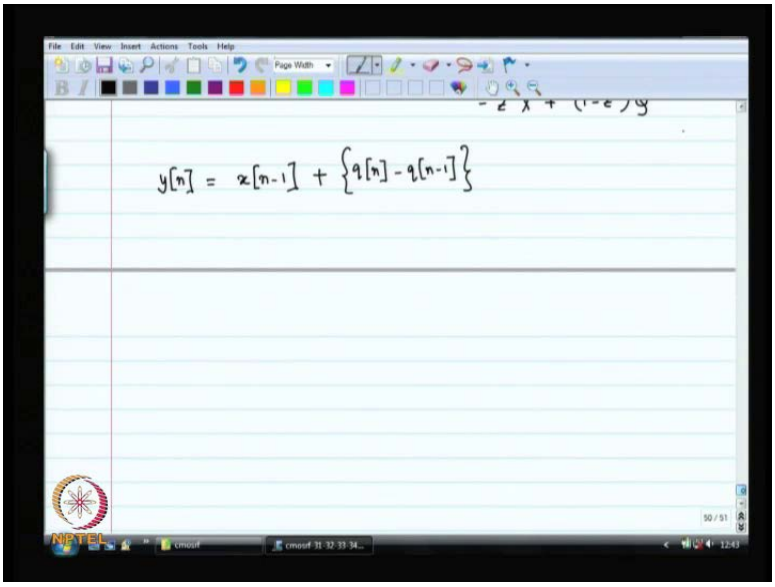

That is what you are output series is going to look like series of numbers that is what it is going to look like and if you want to plot the spectra of these, please go ahead you will find that 2 z inverse x is actually an all pass transfer function. It passes everything it is just x previous sample of the x and 1 minus z inverse is high pass function if there is change in quantization noise then it is going to go through that there is no change it would not go through. So, let us do an example let us say that I want x to b 0.1 al x is 0 1. Instead of doing it with the binary bit is very complicated doing the actual system we just try to solve this time series and let us see what happens.

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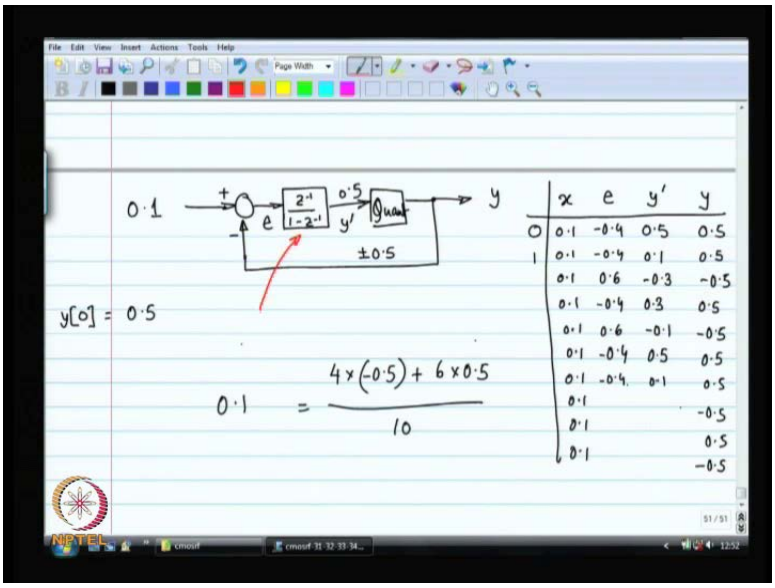

So, here as the MSB selector part all I am going to do is I am going to say whether the quantity is positive or negative. Let us say, I quantize to 0.5 no plus minus 0.5, so this quantize output is these are these 2 possible values plus 0.5 and minus 0.5, so let us do the system let us say that initial quantizer output is plus 0.5. Let us say, that initially what I have got over here is 0.01 or 0.5 that is the initial value at the input of the contacts. So, let us make a table x is always 0. 1 this is y and the input to the quantizer is y is y hat and this is error.

So, let us say time 0 x is irrelevant the error signal is irrelevant y hat is 0.5 and y is 0.5 this is where we start from x is always 0.5 time instant number one the next clock cycle, you are going to find that the error is minus 0.4. So, your new y hat y hat is going to be the previous y plus the previous error previous y plus the previous error is equal to previous y hat plus the previous error is equal to 0.1 and 0.1 is going to be quantized as plus 0.5 and again the error is minus 0.4.

Now, the new y hat is going to be minus 0.3 and since the new y hat is minus 0.3 the new y is going to be minus 0.5 which means that my error is now, going to be plus 0.6. Now, the new y hat is going to be plus 0.6 plus minus 0. 3, so plus 0.3 which means that I have got 0.5 over here and that means, my new error is minus 0.4 if the new error is minus 0.4 old y hat is 0.3, so the new y hat is going to be minus 0.1 that means, I am again going to

get minus 0.5 and I have again got minus 0.5 over here means that my error is plus 0.6 and then keep doing this.

So, the new y hat is going to be plus 0.5 now, which means that my new y is going to be plus 0.5 and my error is going to be 0.4 and it is kind of, it is going to repeat and this I have made some mistake it is going to repeat it is self. What you are going to see is that if you look at 10 cycles then 2 of them are going to be plus 0.1, minus 0.1 I am sorry 2 of them are going to be minus 0.5 8 of them are going to be plus 0.5 no; so 4 of them are minus 0.5 6 of them are plus 0.5 over 10 cycles, so the average is going to be 0. 1.

Which is what you wanted to have as your average then fortunate part over here is that the cycle repeats it is self. So, first of all this is the basic sigma delta modulator it is called the first order sigma delta modulator, cycle is repeating it is self means that you are still stuck with periodicity and as long as you are stuck with periodicity, you are going to see the spurious storms your output, so this is still not exactly what you want.

So, to break the periodicity what 1 need is to do is to make this filter second order, third order and typically it is seen experimentally that is sufficient to break the periods. What do you see as the output over here is minus 0.5 sometimes plus 0.5 sometimes I have already written the output. So, not going to plot it again the output is plus 0.5 therefore, 2 cycles and minus 0.5 for 1 cycles and again plus 0 again minus 0.5 and again plus 0.5 from the 2 more cycles etcetera.

So, it is a pulse rate modulator sigma this is the plus rate modulator signals for you the width of the pulse is telling you how big the signal is, so we are achieving the same result as before it is just that this periodicity is not that well determined, so for example, if I wanted instead of 0.1 if I wanted 0.3 things could be different over here or instead of 0.1 if I wanted 1 by 3 things could be well different over here.

So, this periodicity also kind of dependents what the signal is as far as the sigma delta is concerned once again these are called spurious frequencies this periodicity is called spurious frequencies and sigma delta designers do not like this which is why first order sigma delta modulator are generally found up on, but the good news is that as soon as you make your H.

We did this first order system just for to get some understanding, how the sigma delta modulator is going to possibly works, but if you replace this first order is z inverse 1 minus z inverse. If you replace it by second order block the good news is that the periodicity is broken you no longer get this kind of repetitive behavior and as soon as that happens the output spectrum of the sigma delta modulator.

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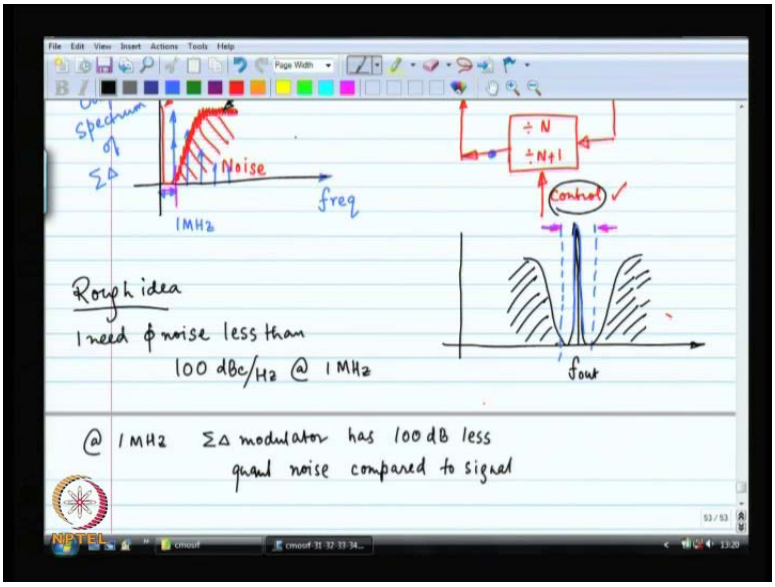

Now, the output spectrum of the first order modulator kind of looks like this these are the spurious frequencies, but as soon as you break the periodicity by making it the higher order system you get the better rejection over here and you get the higher slope for the quantization. Now, as far as we are concerned our signal this signal I have got over here this x is it a low pass signal high pass signal, so number it is a number the constant number the base station tells me go to this channel I have to figure out I have to, so much to go to that channel that is that number.

Actually, the fractional part is what you are taking the integer part is already there base station tells you have to go to this channel I figure out that my n should be 90 and I need to divide by 90.1, so I need to figure out whether to divide by 90 or 91 according to that, I will divide by 90 by 1. So, this x is basically something 0.1 it is a fixed number is low pass signal it is not changing at all or it is changing as rapidly as the base station is asking you to switch channels which is not very fast unless you are in plane.

So, as far as we are concerned this x is the low pass signal it is like a d c the constant signal. So, really the signal to noise ratio the signal to the quantization noise ratio within the pass band can be made arbitrarily signal to the noise ratio can be made arbitrarily large, if you just keep in using integrators or accumulators as your building blocks. The sigma delta modulator to use is not something very ordinary second order sigma delta modulator will do the job for you all you have to now make sure is that you have broken the periodicity.

Which second order or if you go to the third order even better will definitely equal to the now, why I draw this output spectrum if this is the spectrum of the division by n division by n plus 1 signal, what do you think is going to be the spectrum of the frequency output of the v c o, tough question this is the spectrum not going to call both control signal. So, the spectrum that I have drawn on the right hand side on the left hand side is the spectrum of this control signal.

Let me draw more realistic spectrum for you more realistic spectrum is going to look like this were all of this is noise quantization noise and this is your signal this is more realistic scenario. Now, this is the spectrum for this particular wire over here the question is what spectrum are you going to see at the output of the v c o because, that is the key thing that is what you are trying to fix over here what was the spectrum of this control signal earlier, when we were doing pulse width modulation, what was the spectrum of the control signal when we were doing pulse width modulation.

When we were doing pulse width modulation you pick 901 cycles out of 901 cycles first 810 you would divide by n, so it is 0 next 91 you are going to divide n plus 1. So, it is going to be 1 which means that every 901 cycles, it is going to repeat which means it is going to repeat as we had 900 and 1 mega hertz at the outputs, so 901 cycles mean it is going to repeat at a frequencies of 1 mega hertz. So, this control signal this pulse r width modulator signal it is self is periodic with the frequency of the channel raster.

So if you look at the spectrum of that particular signal you would see the d c and then at the channel raster frequencies and it is harmonics you would see impulses. And interestingly enough the output of the v c o was also looking like that just modulator at f naught f out the control voltage for the v c o look very similar impact the spectrum of the

control voltage for the v c o also reflected this behavior, there was some d c and there was the fundamental at the raster frequency and it is harmonics.

So, that is what I have broken that is what I have successfully broken if I can claim that the control signal is coming from the delta signal output which is no longer periodic. So, given that control signal output is no longer periodic, you can expect the signal over here to be not periodic at 1 mega hertz anymore, but yet you are going to do some sort of division by n plus a fraction which means that you have done your job.

Now therefore, what do you expect at the output of the v c o what is that you expected output of the v c o come on, so answer to my question what do you expect over here you do not expect the channel raster to be their fine good what do you expect. Expect the output of the v c o to look exactly like at modulator at the output frequency, that is what going on I just modulating the signal at the output frequency.

So, this f out comes to your d c and around f out systematically you are going to see junk because, of, the quantization noise of this sigma delta modulator. Now, tell me how good that sigma delta modulator have to be it is got to be good within the loop bandwidth of your synthesizer this is going to look like the reference within the loop bandwidth, so the face noise of the reference is going to be tracked by the output of the v c o, but that is only within the loop bandwidth.

So, let us say the loop bandwidth is this much, so within that loop bandwidth the face noise of the reference is going to be tracked by the v c o raster the v c o face noise is irrelevant outside that the v c o noise kicks in. So therefore, what should be the signal to the noise ratio requirement as far as your sigma delta modulator is concerned tougher and tougher questions, so you have to make sure that you have to keep this region clean enough within the loop bandwidth.

That is where we started from that within the loop bandwidth there was the spurious frequency that spurious frequency went through that was the problem. Now, let us say that this my loop bandwidth over here, I can have the large loop bandwidth now, because, I can do this division by a fraction. So, loop bandwidth is not 110th reference of frequency then the loop band time is 110th of frequency it is just that reference frequency a much larger.

So, I can have the large loop bandwidth now, within this loop bandwidth whatever noise the sigma delta is producing whether it is the discreet tone because of pulse width modulation or whether is quantization noise or it is anything else. Whatever noise the sigma delta is producing within the loop bandwidth that noise is go through my phase lock loop because, it is within the loop bandwidth and it is going to effect the performance of my system. So, I have to design my sigma delta modulator to have certain signal to noise ratio within the loop bandwidth.

So, all of these are now, getting related to each other the sigma delta modulator design now, suddenly we said that it is going to be easy it is no longer sounding because, now, you have to make sure that let us say this is my loop bandwidth over here half of the design, let us say this is 1 mega hertz. So, from 0 to 1 mega hertz you have to make sure that there is only signal and no quantization noise, so now, you have to make more intelligent design for the sigma delta modulator, so that no noise is produced in that region so we have to place 0s for example, you have to make the higher order sigma delta modulator.

So, that the quantization noise is, so many decibels and decibels below the signal or something like that. So, all of this dependence what your face noise is requirements are now, it is really getting inter linked, so the face noise requirements are the face noise requirements of the reference oscillator, so to meet those face noise requirements you should make sure that you do not add additional noise because, of, your mistake of the sigma delta modulator with the division is adding some excess noise into system you do not want that to happen.

,so you have to keep yourself clean within the loop bandwidth and within this loop bandwidth your requirement as far as signal to noise ratio is concerned is dictated by the face noise requirement of your final output within that loop bandwidth which is basically that face noise is of the crystal oscillator. The crystal oscillator is very clean you have to be as clean as that you have to be sure that you do not make it dirty.

So, this is the seam of things these are all inter linked these are all getting inter linked with each other the sigma delta design has to be clean enough, nice enough, robust enough that you do not additional noise as a result your simple addition circuit. Over here is definitely not going to work you have to work herder you will have to place 0s

You will have to burn more power in your digital circuit all digital there are no analog signals in the sigma delta over there we listed out all the different components H is the digital numbers H is the digital filter.

Basically what I am saying is that digital filter is going to be far more complicated you will need adders, you need multipliers probably hopefully you would be able to do just shift operations if you can go shift operation we and good you have saved yourself in some trouble, but you need large number of bit is because, you need to make sure the precious and so on, so forth. So, you are going to burn man hours we are going to burn power in the sigma delta modulator area and power in the sigma delta modulator and you are going to divide by a fraction.

Dividing by a fraction is going to allowing you to have larger loop bandwidth will allow you to have faster settling time people allow you to have better face noise and less you have dirtied the face noise which your sigma delta modulator . So, this is more or less were we are going to close this topic of frequency synthesis, we are gone into lot of detail we have studied face lock loops.

We did it really examine what should be the precious values of the resister capacitor in the face lock loop, but we did go into lot of detail and if you looked up the references then all of this is discussed the very different manner. So, that is also 1 reason why you come to a class because, the teacher explains things to you in a different way, he give you different perspective. So, that is what I try to offer to you I gave you face lock loops from a very different perspective from a control theory perspective we are trying to do velocity control this is what you have got to do.

So, that is how we studied face lock loops then we said that this integer n frequency synthesis is just extension of face lock loop you are just divide the face by factor now, it, so happens that this factor can only be in the integer no problem then we saw examined were spurious frequency is came from the integer n frequency synthesis why is that. So, much importance given to this spurious frequencies because, spurious frequencies are very annoying if you are making the receiver and you have spurious frequencies in your synthesizers.

Then you might receive someone else is channel instant of yours or you are making the transmitter and you have spurious frequency all over then you are transmitting at all over

channels and that is no good as far as the transmitter is concerned. So, it is very annoying this spurious frequencies really cause and lot of, times people do not pay attention to this and these come in from deferent sides and you have problems in your radio.

So, we saw that integer n synthesis this spurious frequencies were because, of, non idea ethics fraction length systematic no matter what you do you are going to get spurious frequencies and those specific, add the channel raster frequencies. So, that was also that is were we said that fractional synthesis is good I want to do some things like divide sometimes dived n plus 1 sometimes.

But I should not be doing this periodically, I need to stop doing this periodically and that is where we came up with this we pulled up sigma delta modulators from our A to D convertor book and we modified a little bit because, we are not really doing analog digital conversation you already have the digital numbers you are going to create 1 bit digital number whose average is represents the original digital numbers. However, I want to make sure that 1 bit digital number is not the periodic signal that that was our necessity and that is what we suited out.

Sigma delta modulator for then I briefly discussed this sigma delta modulator it is self we looked at the dynamics, we saw that first order sigma delta is still going to be periodic which is bad news, we have to make higher order modulators then we saw that suppose I make the higher order modulator without paying too much attention then I am going to have face noise problems any way. So, you have to make the sigma delta modulator have to design it carefully enough.

So, that you do not pollute your voltage control oscillator upward, so mathematic for that is very involved we are not going to get into it, but as a rough idea you can say that if I need. So, many d b c at an of set of, so much frequency. So, rough idea of what is requirement of sigma delta I need face noise less than let us say 100 d b c per hertz add an set of 1 mega hertz suppose, this is the requirement of the face noise of v c o final now, the crystal oscillator is good enough for this to give you this your loop bandwidth is 1 mega hertz.

So, you need to make sure that at 1 mega hertz your sigma delta modulator gives100 d b less noise compare to the signal this kind of gives you an idea of what needs to be done. However, this is not end of the story you have to work on this you have to stimulate the

entire dynamics and you have to fine tone your requirements with this we are going to close this lecture as well as this module about frequency synthesis and in the next lecture we will start a new chapter all together that is our amplifiers.

Thank you.