CMOS RF Integrated Circuits
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Module - 11
Frequency Synthesis
Lecture - 35
Fractional Spurs

Hello and welcome back to CMOS RF Integrated Circuits, we were discussing Frequency Synthesis techniques. So, that is what a business was and we had a developed some sort of a fractional synthesizer, fractional end synthesizer that what we called it. Today we are going to take a re look and understand where are the spurious frequency if I at all, so that is what we are going to understand and then we are going to develop better ways of doing fractional synthesis, so that is my plan now, just recap.

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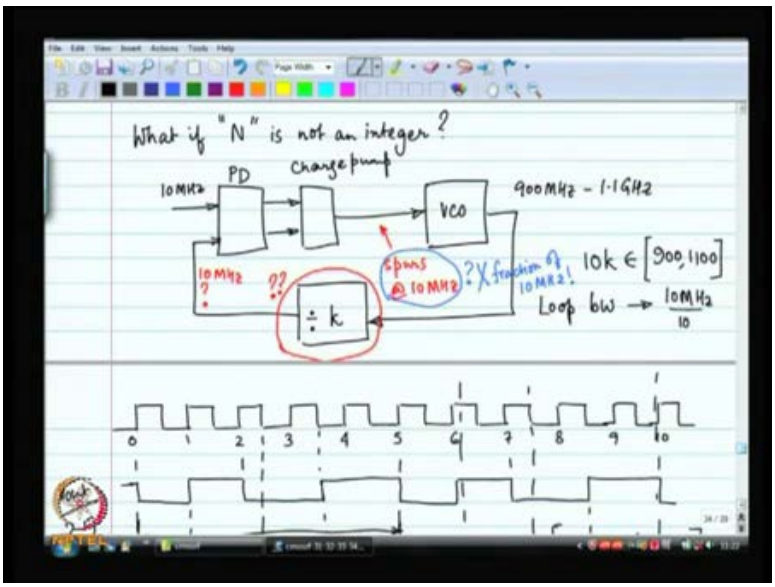

So, this is what we wanted to do we wanted to have the phase look loop and on the feedback path I wanted to divided by k, k is suppose to be programmable and I should be allowing k to be not just integers also fractions, so this is the basic problem I want k to be a fraction not just a integer, integer is easy to do that is what we did in the first shot. We found that my loop band width would be very restricted and restricted loop band width means, I need a better phase noise performance as far as the VCO is concerned, I need a to allow for slower settling time as an longer settling time.

So, it will take much longer time to hope from one frequency to another the synthesizer this are the problems with lower loops bandwidth I do not like lower bandwidth, so as a result I need to be able to divide by a fraction. So, this was the basic premise of the story now, given that this is the basic premises we develop a way to divide by a fraction.

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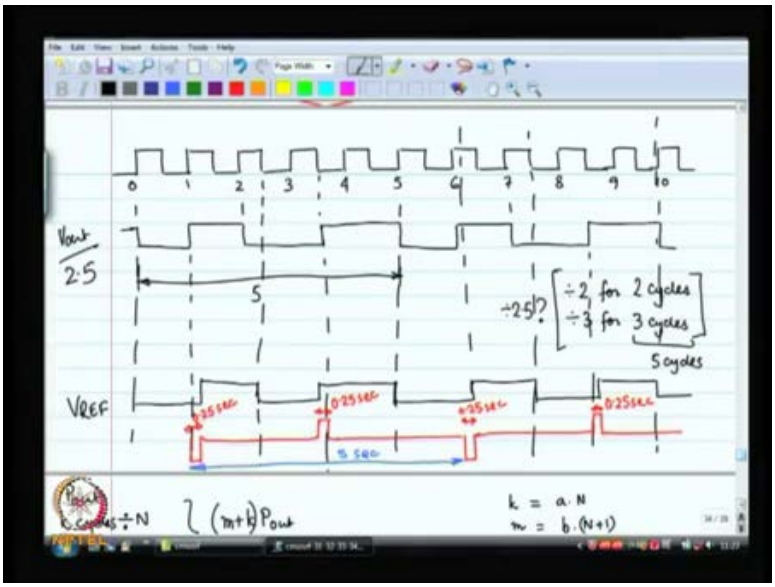

I set let us divided by 2 for 2 cycles let us divide by 3 for 3 cycles

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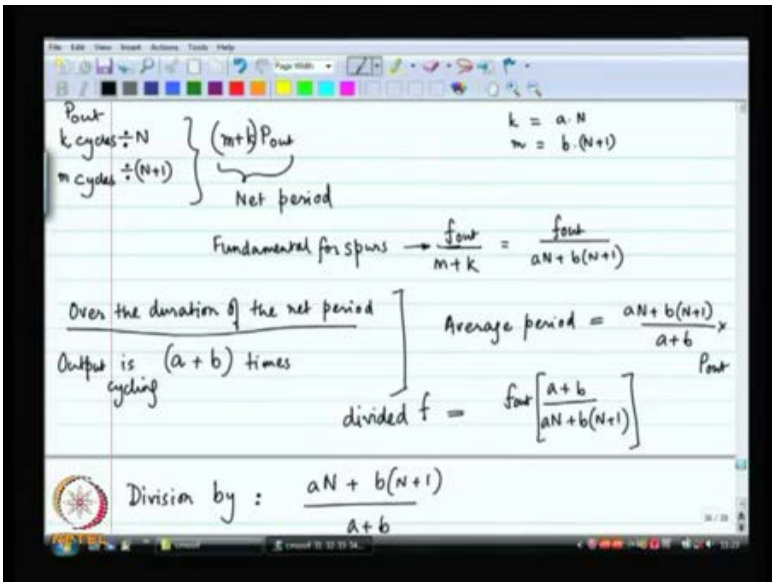

You could generalize this and say that let us divide by N for k cycles and let us divided by N plus 1 for m cycles, but of course, k has to be a multiple of N and M has to be a

multiple of N plus 1 that is, but of course, and I said that let us assume that k equal to a times n and m is equal to b times m plus 1 k cycle and m cycle. So, the total number of cycles that I am waiting for is k plus m which means the net period of the whole business is k plus m cycles at the output.

So, my fundamental for this spurs will be at this particular frequency I will get spurious frequencies this is the net period for those porous frequency. So, I will be getting some up pulses some down pulses etcetera and they will keep repeating at this frequencies, so this is the fundamental and then we figure out that we average period. So, then I figure out that over the duration of the net period the net period is, so many clock cycles over the duration of a n plus b n plus 1 clock cycles. The output is going up and down a plus b times which means that on the average the divided frequency is f out that is the frequency at the output times a plus b is going up and down a plus b times over a net period of a n plus b n plus 1 clock cycles this is my divided frequency and therefore, I have achieved a division by this particular factor.

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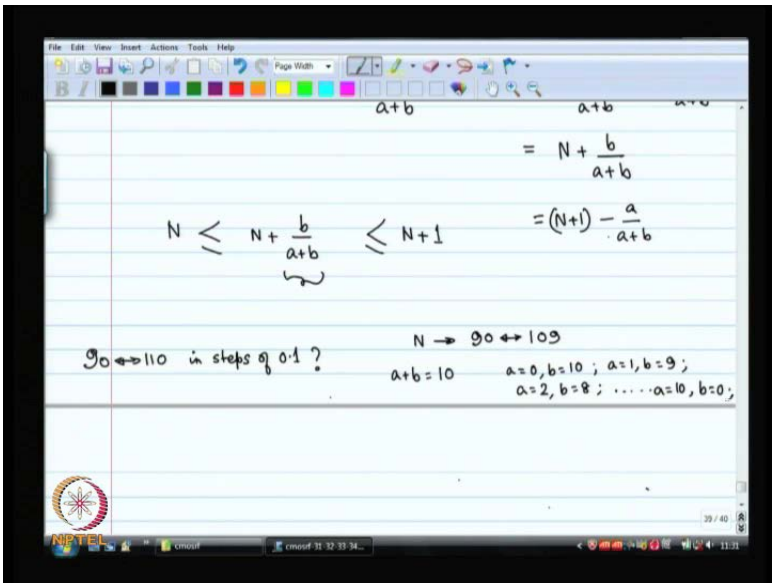

This is what I have managed to do now, what at this mean is this number going to be more then n has to be more than n this is definitely more than, so this is definitely more than N is it a more than N plus 1 no it is not more than N plus 1 it is little less than N plus 1. So, I have got I have managed to divide by something which is more than N less

than N plus 1 and by what fraction is it more than N by b by a plus b, so that is why it is called a fractional n synthesizer.

So, you are dividing by a little more than capital n little less than capital n plus 1, but of course, sometimes you are dividing by N sometimes you are dividing by N plus 1. So, in effect you have got to be on the average you got to be dividing by something more than N less than N plus 1, so this is basically d plan. Now, N can be a large number N can be I do not know N can be one thousand N can be one hundred for example you could say for our previous example what was the example we had chosen I do not see the example anymore.

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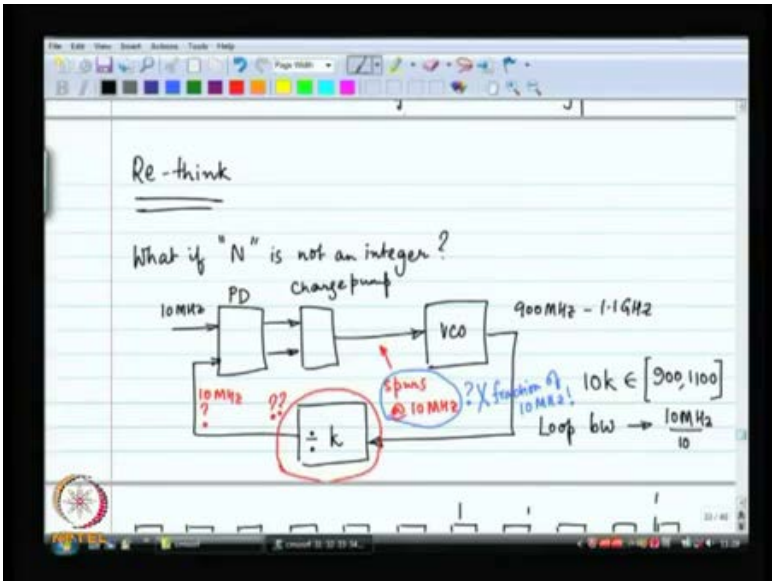

This is the example that we are chosen the input reference is the 10 megahertz I want an output between 900 megahertz and 1.1 gigahertz. So, a with a channel raster of 1 megahertz this was my plan. So, I want to be able to divide by k, k ranging from 90 to 110 with the first decimal place, so can I can this go from 90 to 100 and ten in steps of 0.1 how will you do that see n can always be changed, so the range of n has to be from 90 to 109 if you want a little more you can range from n from 90 to 110 no problem what about b and a I want a plus b to be a number like 10.

So, I can have 10 possibilities a equal to 0, b equal to10 I really do not need to do that I could just choose a equal to10 b equal to 0 it will give me the same thing same effect I can go for the next hire number. So, I have got this eleven possibilities 1 of m is retain

dent does not really matter and that will cover this entire a range and I will get my steps of 0.1.

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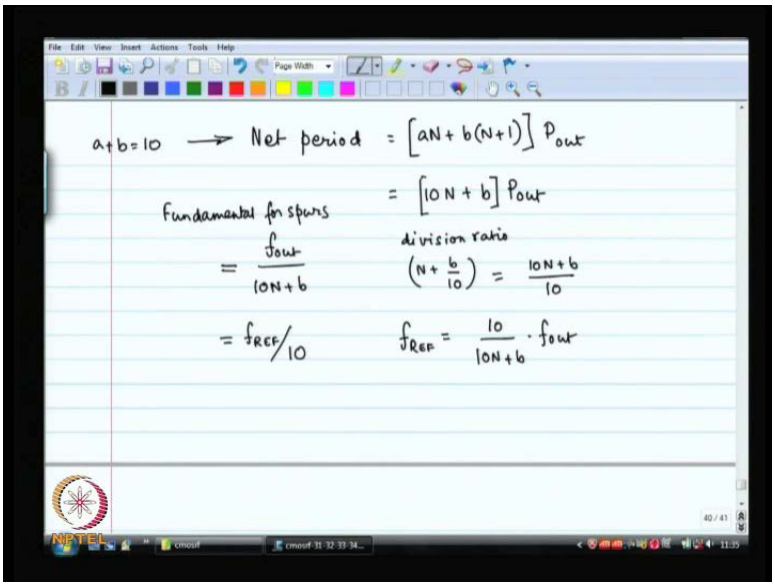

Now, how do you organized this a before that a plus b is now, equal to 10 what does that means, as far as the net periods is concerned I am calling something the net period what was the net period that is going to give me the fundamental frequency for this spurs. This is the net period and over here a plus b is restricted to 10 which means that I have got10 times N plus b times p out that is my net period which means that the fundamental as far as the spurs are concerned.

So, where are the spurs coming from the control voltage is having some gliders at a certain frequency what is the fundamental frequency for that the fundamental frequency for that is f out divided by 10 times n plus b, what is our division ratio? Our division ratio is n plus b by 10, that is are division ratio a plus b I am saying let us be 10 this is the specific example.

That we have doing that is equal to 10 times n plus b by 10, that is my division ratio which means that the frequency f ref is equal to 10 n plus b times f out and a just do a little bit of jiggling and you will see at this is what you have got f ref was 10 megahertz. So, you have got the fundamental for this spurs at precisely 1 megahertz which, so happens to be the same as the fundamental for this purpose in the integer n case amazing.

So, you decided to have a certain channel raster no matter what you did whether you did an integer n circuit or whether you made this complicated fractional n circuit this porous frequencies are precisely at the channel raster frequency no others strains frequencies. This is really amazing and unfortunately this has rather bad consequences for this kind of a fractional n synthesize why because, of basic premise of building a fractional n synthesizer why did we built it why did we make it, so complicate dived by n divide by n plus 1 we made it.

So, complicated because we wanted larger loop bandwidth I want a 10 times larger loop bandwidth, so that is why instead of having the channel raster frequency as 1 megahertz I need the channel raster frequency equal to 10 megahertz and instead of dividing by integers. I divided by integer 0.1 decimal place right this was my basic plan that means, that my basic idea was to increase the loop bandwidth by 10 times loop bandwidth let us say it is 110th of the reference, so reference was 1 megahertz loop bandwidth was hundred kilo.

So, the integer n k reference was 1 megahertz loop bandwidth hundred kilohertz porous frequency are appearing at 1 megahertz offset from the fundamental from the output which means that the loop is rejecting significantly, this porous frequencies they are out of band porous frequency are at 1 megahertz, 2 megahertz, so on loop band width is only 100 kilohertz, so 1 megahertz, 2 megahertz are getting rejected by 20 db.

In our case this fractional n case the new, loop bandwidth is 1 megahertz because, that why I built the fractional n the porous frequencies are at 1 megahertz, 2 megahertz and, so on same as before and therefore, this porous frequencies are passing through the loop without any attenuation within the loop bandwidth. Do you see what we have pointing at over here the problem that we have over here the problem that we have over here is that fractional end has larger loop bandwidth and this porous frequency are within this loop band width. So, there will pass through the integer n as narrowed loop bandwidth this porous frequency are out of band.

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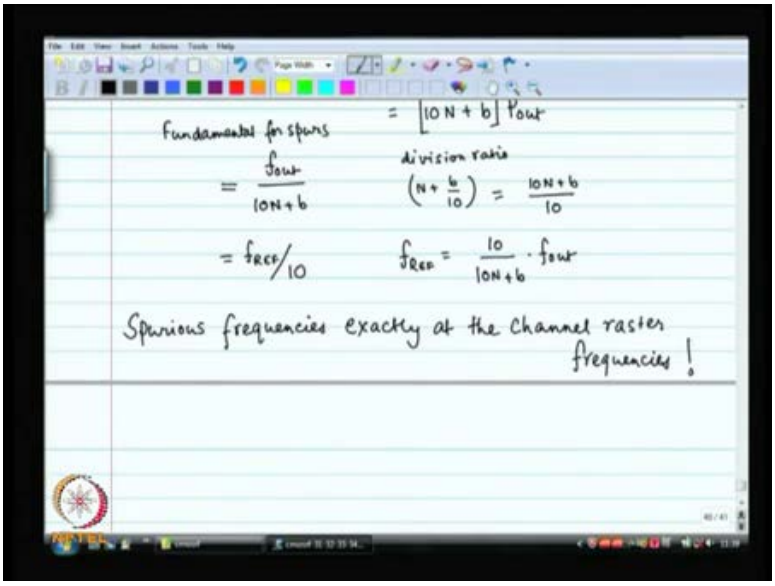

So, in both cases this porous frequency are appearing preciously at the channel raster frequency, spacing between 2 channels, so this is a big problem. So, whether you are building and integer and synthesizer or this kind of fractional n synthesizer you got porous frequencies and this porous frequencies are precisely at the same frequencies as in both cases.

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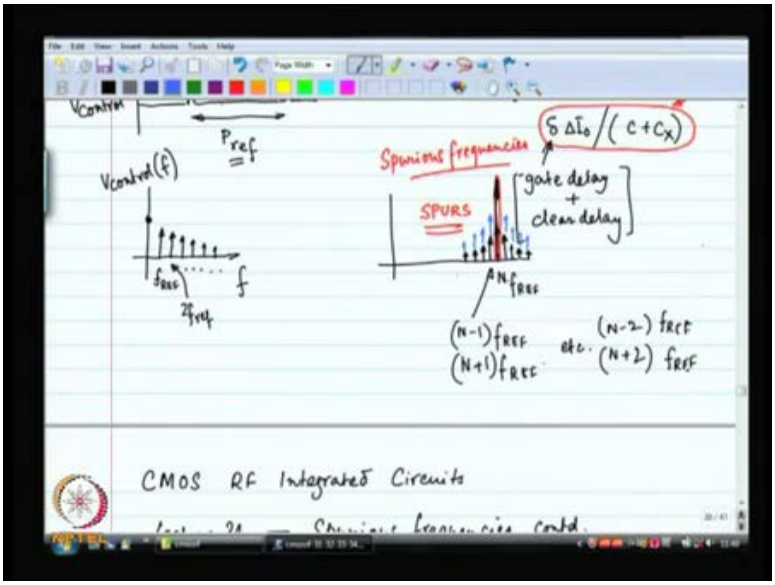

Spectrum will look the same spectrum will look exactly the same except for the fact that in the fractional n this porous frequencies will be larger because, why will this porous frequency n be larger because they are within the loop.

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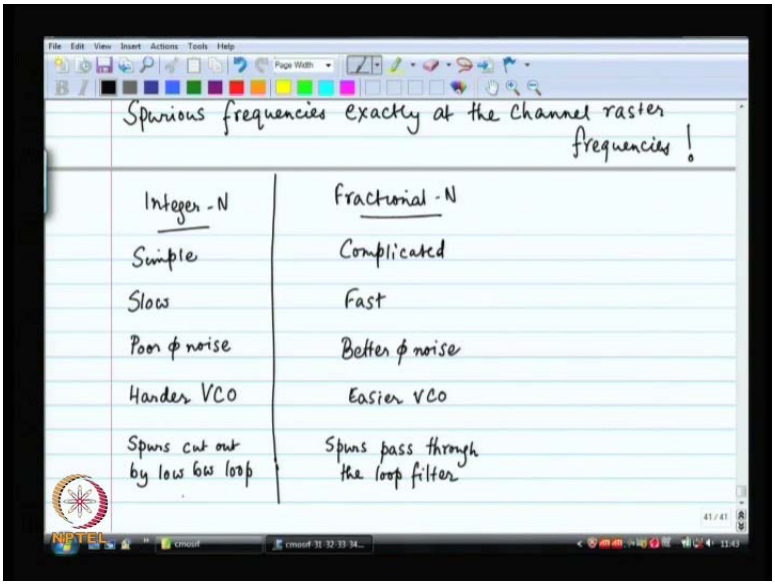

So, let us do a head on comparison of the 2 techniques that we have leant so far, integer n simple, fractional n complicated its more difficult to understand what is going on next integer n slow very slow, fractional n can be made first. Slow in the sense it has very slow settling time the settling time, is really a inversely to proportional to the loop bandwidth the larger loop bandwidth faster its going to be low or the settling time.

Next what else, so the integer n I say that it has poor face noise fractional n has better face noise why did u I say such a thing because of low loop bandwidth integer n has the lower loop bandwidth which means the it a can mimic the reference over a lower bandwidth fractional n has more loop bandwidth. So, v c o face noise requirements are less reneged, so I am just writing as a harder v c o and easier v c o it has better face noise.

Then so for, the integer n this spurs are cut out by the low bandwidth loop whereas, for the fraction n synthesis technique, the spurs pass through the filter through the loop now, this spurs happen to be precisely at the channel raster frequencies which is very annoying to the base station why because, these are the next channel where the other user are going to be you are transmitting signals at other channel as well you are occupying you are

creating a lot of interfere. So, as a result this is extremely annoying as far as the total r f environment is concerned.

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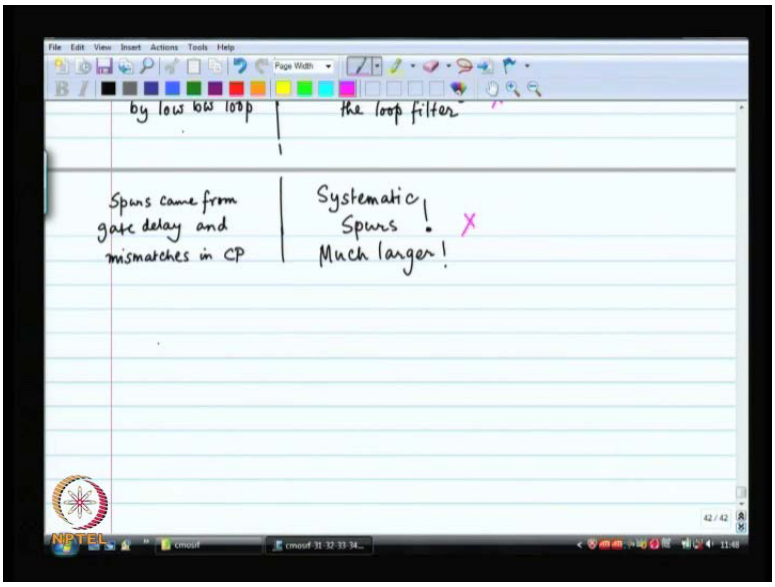

So therefore, we have a problem now, one more thought where did the spurs come from in the integer n case and in the integer n case the spurs came from gate delay and miss match between the in the charge pump in the 2 current sources in the charge pump, where did the spurs come from in the fractional n synthesizer, they did come from mismatches no it did not come from miss matches it came systematically take a look at that it came systematically the way I divided my output frequency to compare it with a reference frequency.

That very technique introduced equal and opposite up and down pulses of certain duration remember that is how we did it. So, that is where the spurs came from, so the spurs in the fractional n are systematic they have nothing do with this matches they are nothing do with get delay etcetera they are systematic which of course, means that this spurs are once again going to be much larger than the integer n case the integer n case of course, to a tiny I could lower mismatches 0.1 percent.

I could improve my I could built faster gates etcetera. I could try to do lot of things to get of spurs in the integer n case in the fractional n case this spurs are systematic they are going to be there they are not because of, any non idealities itself it is the very technique that is introducing this spurs frequencies.

So therefore, we need to seriously thing about what can be a better way to do this division by n and n plus one, so you see over here for the fractional n I like the fractional n because, it is fast it has better face noise. I can make an easier voltage controlled oscillator this are the reasons I like it and there is nothing, that you can do in the integer n circuit to improve this you cannot do anything to improve this things just not possible if you have to have the loop bandwidth 110 of the channel raster.

So, what can I do to the fractional n to get read of this spurs seem to be very serious in this fractional n synthesis we are very serious first of all they pass through the loop filter. Secondly, they are much larger because they are systematic, so what can I do, so once again re think and re visit.

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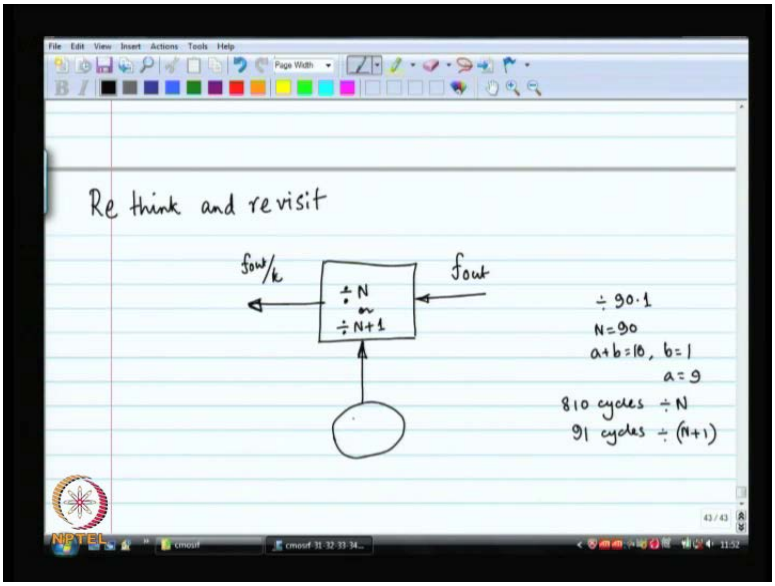

What was my strategy to do this division seems to be the basics stumbling block because, the division is creating the spurs and I need to be able to divided by a fraction if I just keep dividing by integers it is not enough as far as loop bandwidth is concerned. So, I am calling this f out by k in terms of frequency, so this was our strategy I was dividing by n or I was dividing by n plus 1 to do a division by 90.1 let us say I want to divided by 90.1 to do a division by 90.1 what we did was we choose n to be equal to 90 we choose a plus b equal to10 and we choose b equals to 1.

This was how we manage to divide by 90.1, so f out will be 90.1 times the reference frequency is 10 megahertz, so f out will be 901 megahertz this was the strategy that we

have. Now, you have to control over here digitally, but of course, when you are going to divide by n when you are divide by n plus 1 and what are this a and b, so for a times n cycles an cases is 9 and n is 90, so what I am saying is for 810 cycles divide by n and for the remaining 91 cycles is that 91, b is 1 n plus 1 is 91.

So, for 810 cycles it is going to divide by n and for 91 cycles it is going to divide n plus one, so this particular logics circuits is clock by this and there is the counter over here that is going to count till 901 now, out of this 901 is going to say 810 times let us count by n and 91 times let us divide by n plus one. So, this is basically the thought process what can I change over here to remove the periodicity there is the periodicity over here every 901 cycles takes 901 cycles and every 901 cycles out of that 810 its asking to divide by n 91.

Its asking to divided by n plus 1 the output is always the same every 901 cycles which means that the entire thing is periodic with the period which is 901 times the reference I am sorry 901 times the period of the output lock which is the channel raster once again. So, we have to some of break this periodicity we cannot let it be, so periodic what do I do what you think what can be done what can possibly be done over here now, think a little bit do you think this is some sort of an of a pulse quick modulation do you see a some kinds of pulse modulator signal this one.

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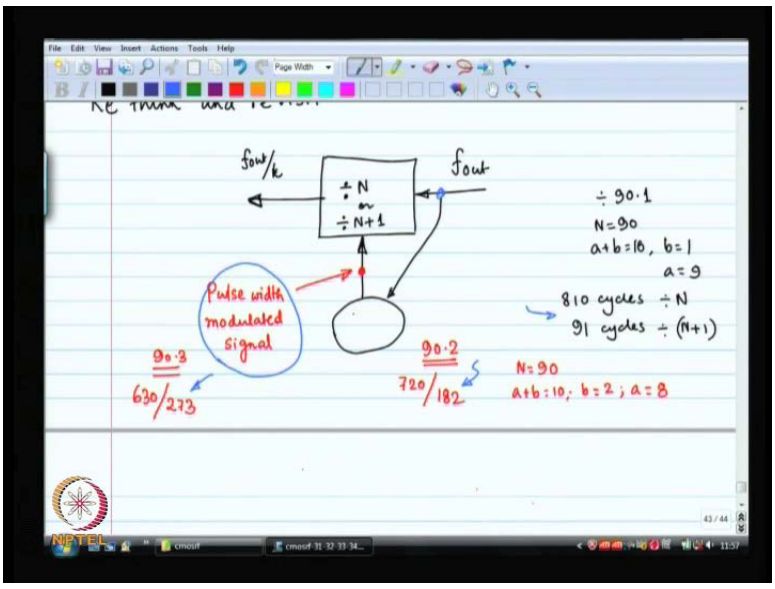

So, that particular signal over there is 1 or 0 if it is 1 you divide by n plus 1, if you 0 you divide by n that is the idea as far as the divider is concerned now, that particular signal is some sort of a pulse quick modulator signals you are modulating the width of the pulse if you wanted a 90.2 then you would do n equal to 90 a plus b equal to 10 b equal to 2 a equal to 9 this is what you would do a equal to 8 I am sorry which means, 8 times 90 is 720 cycles you would divide by n and 100 and 182 cycle you would divide by n plus one, so that is how you would get division by 90.2.

So, the width of the pulse is kind of telling you what this division is going to be if you were to divide by 90.3 the width of the pulse would be 630 to 273. The duty cycle of the pulse is going to increase, so here the duty cycle was if I want to divide by exactly by 90 duty cycle is 0 here the duty cycle is 10 percent, here the duty cycle is 20 percent, here the duty cycle is 30 percent, 90.3 duty cycle is 30 percent, 90.4 you expected duty cycle of 40 percent 90.5 50 percent and, so an 90.9 you will have a duty cycle of 90 percent, 91 you can do a duty cycle 100 percent or you can change n and make the duty cycle 0 percent.

So, this is the plan and as a result this particular signal over here is pulse width modulator signal are there better ways, to get this pulse width modulation you are getting a pulse width modulator signal by counting clock cycles, you are counting cycles of f out and you are saying for this many cycles I will have a 1. Over there for this many cycle will have 0 over there and that your pulse quick modulator signal is there any other way to make pulse modulator signal.

So, you are converting this number this fraction that you want to a pulse quick modulated signal how else can you create a pulse quick modulated signal. Any other popular examples think about A to D convertors way to, A to D convertors come here there is A to D converter here you are converting floating point number of fractions into a 1 0 signal your converting a fraction 0.1 0.2 0.3 this kind of a number into a duty cycle of a 1 0 signal, how else could you do this sigma delta modulation a delta sigma modulation whatever you want to call it.

Are you familiar with delta sigma modulations, so the thought is that you want to randomize this pulse with modulator signal over here you do not wanted to be show deterministic you want to create randomness, over here and you want to break the period

at the output you do not want that you do not want the period of 1 megahertz the period happens to be exactly equal to the channel raster frequency that is not good that is not that is exactly what you want to break.

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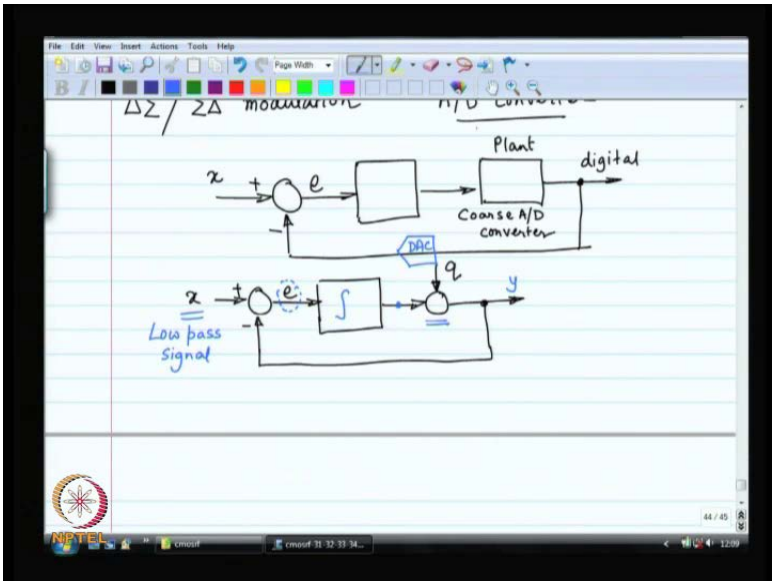

Now we are want to go back this is we are lifting material from possibly a different course analog to digital conversion and we are going to take a brief look at what a sigma delta modulator does very brief look. So, let us keep this on standby over here pose over here, let us briefly study sigma delta modulation and then we will get back now, I will briefly study I will only very briefly study this right it is your job to go back a probably look up the appropriate course or look up a book there are books written about sigma delta modulator or read some good reference paper.

I can give you some good reference material primer basic reference material as far as sigma delta conversion is concerned. So, that is going to be available with reference is called this particular module, but that is your responsibility I will only very briefly discuss the basics of sigma delta modulation.

So, sigma delta modulation is an unlocked to the digital converse technique its very popular, its very robust and why it is very robust is because of, the huge of feedback. So, we have use feedback in face lock loops we know something about feedback, so this is how you are feedback system looks like control system this is how it looks like I am

going to call the import as the x of d actually, let us call it x of n let us make it a discreet time system or although there is no reason to make it discreet time let us call it x.

It could be a discreet time systems it could be a continuous time system that is your business completely this is a feedback control system and a sigma delta modulator is just another feedback control system the plant that I am talking over here is an A to D converter it is a course A to D converter. The course say that A to D convertor that you can possibly think of is a 1 by A to D convertor its usually quite popular to 1 way A to D convertor as the plant over here why 1 bit because, 1 bit A to D convertor is travail its extremely easy to built A by D convertor that is why.

So, this is typically what people do you can put multi plate A to D convertor lot of people like putting multi bit 2 or 3 bit A to D convertors or even 4 bit A to D convertors as the plant as far as we are concerned it is just some A to D convertor. Now, an A to D convertor unfortunately unlike plants and A to D convertor introduces quantization noise this is something unfortunate, so I am going to module this system this is just a module it is not this is how I am going to module the plant, the plant is something which introduces quantization noise.

Now, you are going to come back to n say that x is analog signal this error is analog signal this is the controller or the loop filter whatever you want to say that is an analog signal output of the A to D convertor is digital how can you convert how can you subtract the digital signal from analog signal well yes this got to be a duct over here. Some sort of a d to a converter over here is necessary if you are talking about 1 bit at d conversion then this d to a convertor is travail is nothing in fact, it is a wire right 1 bit signal either e d b or 0.

If you convert it to digital I am sorry if u you convert it to analog you again get back b radiant and 0, so it is the duct is the wire as far as the 1 bit A to D convertor is concerned. If you want to make it a multi bit A to D convertors as the plant then the duct will have to be there you will have to worry about the d to a conversion as well, so in our system in any case this d to a convertor is not something that is going to add any noise and ideal d to a convertor the module for I to d convertor is a straight line is a wire that is the module for ideal d to a convertor the input is, so much the output is going to be the same quantity just that is an analog volt.

So, this is the model for our system I have got I have added some quantization noise here this is the unfortunate part and you are trying to make a controller to fix this problem now, suppose I restrict my x to be a low pass signal. So, this is the biggest things about the sigma delta modulator that I am going to restrict x to be a low pass signal in that case if I have, let us say a some sort of integration over here let us put 1 integrator over there we can put 2 three as many you like let us start with 1.

So, let us say the controller is an integral controller x is a low pass signal, let us say x is constant signal in that case if the average e is not equal to 0 then the voltage over here is going to built up which means that it cannot happen the average error has got to be equal to 0. If the average error is equal to zero that means, that the average of the output is equal to x is this understood the average of the output is equal to x I am not saying what are the dynamics of the output I am just saying that the average of the output is equal to x.

So, if I look at the spectrum of the output at the c I will see x at other frequencies you will see other junk, but I already know that my signal is a low pass signal I already know that my signal is a d c let us say. So, from this information from this output I can put my low pass filter and I can extract out the average quantity digital is this let us think a little more let us say this loop filter is an integrator, let us say that the property of the integrator instead of putting integral over here, let us say it is called H.

H is the either the z transform or laplace transform of the pulse response of that loop filter now whether you are using z transform are laplace transforms all depends on whether you are working with a discreet time system or a continuous times system.

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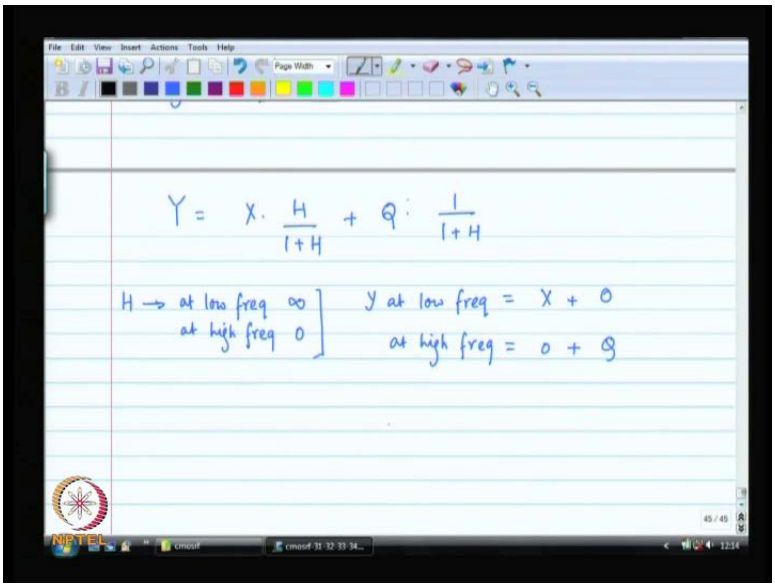

So, suit yourself let us say that is equal to H the loop filter is equal to h in that case the transform of the output that is y will be equal to x times H by 1 plus h forward gain divided by 1 minus the loop gain is equal to minus H plus q there that is the noise you have added quantization noise you have added times 1 by 1 plus h forward gain is 1 and a loop gain is minus H. So, this is the characteristics of the y.

Now, if H is such that at low frequencies it is infinitely large and it high frequencies it is 0 r that is an integrate for you at low frequencies which infinitely large at d c is infinitely large at high frequencies its equal to zero, so then y had low frequencies is going to be x times infinity by 1 plus infinities. So, x plus q times 1 by 1 plus infinity that 0 and at y at high frequencies x times 0 by 1 plus 0 that 0 plus q times 1 by 1 plus 0 that is 1 very interesting.

So, you added quantization noise and this quantization noise is kind of shape in the frequency domain and it push towards higher frequency where as the low frequencies you are stark with the signal its wonderful right. So, this is the idea of the sigma delta convertor where this name is coming from there is this is some sort of an integrator which means you are doing some sort of addition sigma and a you have got a subtraction over here.

So, that is the delta now some people call it delta sigma because the subtraction happen before the integration and, so on really does not matter what it is called that heart of it is

a feedback control system. Now, you can built n more and more intelligent transfer function h to do better and better jobs you can do first order h you can do second order h you can have a third order h and you can have 0 in h etcetera.

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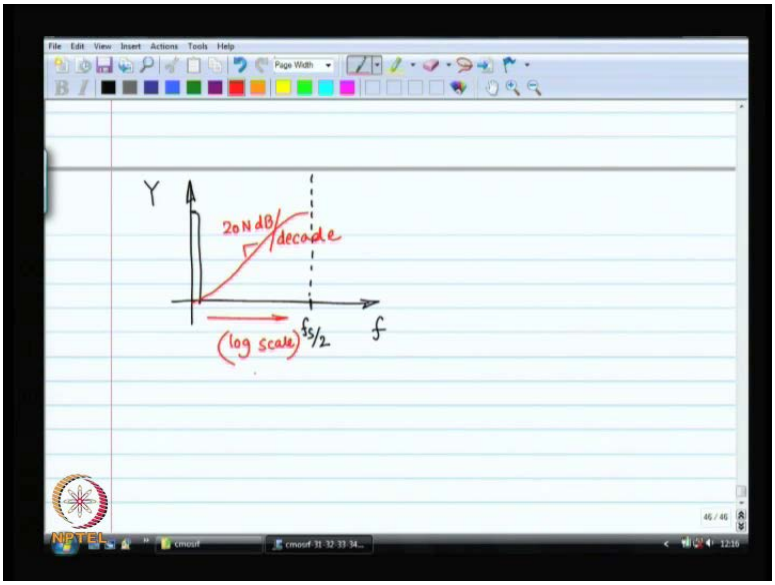

you can do fancy staff and as far as I am concerned as far as this particular lecture is concerned all of this is irrelevant what is relevant let us come to that is the dynamics of this, so if you look at this output spectrum. Now, let us put a sampling frequency over there and let us say it is a discreet time system, so this is your f x by 2 suppose it is a discreet times system in our case we have a time discreet system.

So, the restriction for the sigma delta sigma convertor is that a input is a low frequency signal it is not changing as fast as the sampling rate that is the basic restrictions. In fact, its changing much slower than the sampling rate what you are going to see is that because the loop filter passes the signal and cuts out the noise the output of the sigma delta modulator will look like this.

So, if you plot in the long scale if you plot x axis in long scale then you will see a certain slope and that slope happens is going to be equal to twenty times n n is the order of the transfer function. So, we are going to stop here and in next lecture we have going to try to use this sigma delta to our advantage.