CMOS RF Integrated Circuits
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Module - 11
Frequency Synthesis
Lecture - 34
Spurious Frequencies (Contd.) Fractional N Synthesis

Welcome, back to CMOS Radio Frequency Integrated circuits, so we are in the 11 module, we are talking about Frequency Synthesis and as part of the frequency synthesis, procedures in the previous lecture we were discussing, how we can modify a phase lock loop and create something called an integer N frequency synthesis.

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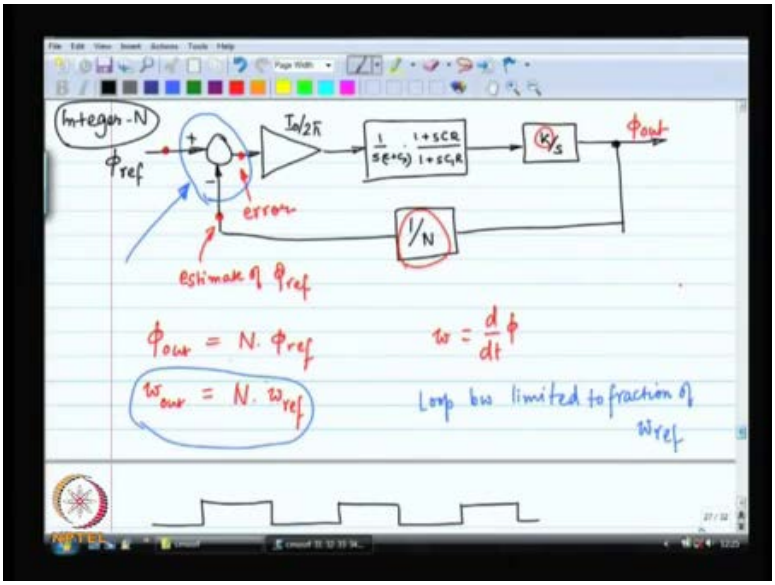

So, the small modification is a clock divider, which is readily available using digital circuits, that is the modification that we are going to make and we are going to label, this as an integer N frequency synthesizer. Now, some important points as far as the integer N frequency synthesizer is concerned number 1, the loop band width limited to a fraction of the reference frequency, it has nothing to do with the frequency that your finally, generating, it has everything to do with the rate at which, the phase detector is operating. So, the speed at phase detector operating, that is what is important over here not the rest of the circuitry, that is going to tell you what is the maximum band width, you can have for the loop great.

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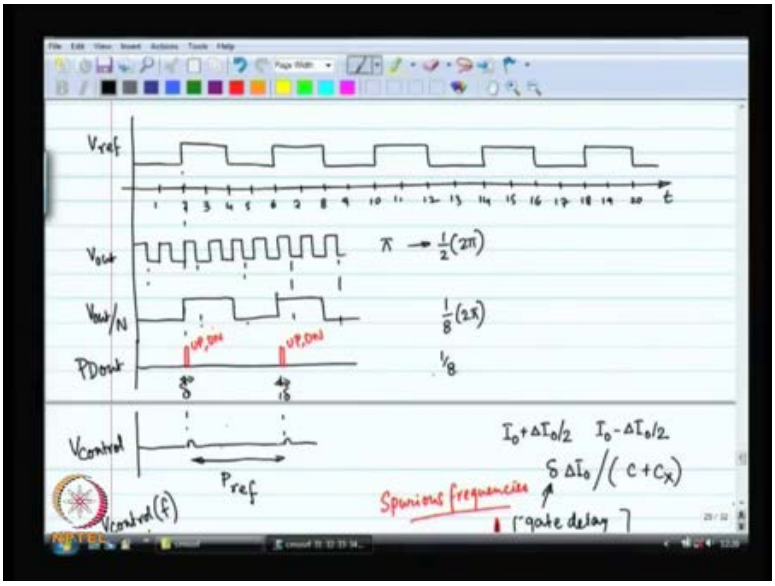

So, next we did a small exercise and we saw, that even when up and down even at perfect lock between, the reference and the divided output even these two are perfectly locked up and down have small pulses of equal duration. And this happens, because of the delay of AND the get as well as the clear operation within the flip flop.

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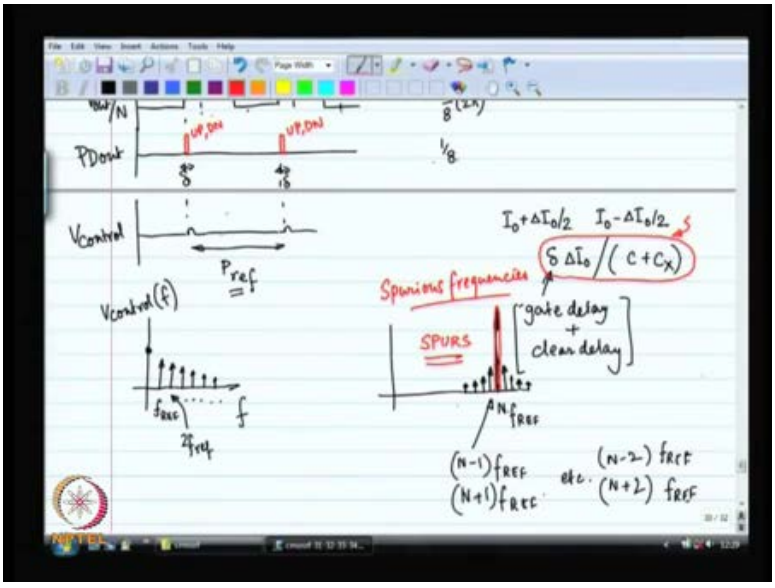

Now, because up and down have the small clutches and because it is impossible to perfectly match to current sources, also note one current source is a source the other is the sink. So, they are not even of the same quality, so one will be made with N

MOSFETS, the other will be made P MOSFETS is very hard to perfectly match, an N MOS and P MOS, it is not possible there will be a small bit of error.

So, with this small bit of error between the two current sources, because of these two small these errors in the current sources and because of the finite delay, non zero delay of the gate and clear signal going to get small glitters on the control voltage. Now, this glitches are going to appear periodically at frequency of the reference frequency, that is the periodicity involves; which means that if I look at the a plot of the spectrum of the control signal. Then I will have a d c and I am going to have all of these tones, the fundamental is f ref I will have f ref and all it is harmonics, in my control signal agreed.

Now, notice over here, how can I reduce these tones I can get it of the tones by making the time, the delay equal to 0 not possible, I can get it of the tones by making delta I naught equal to 0, mismatch not possible, I can get rid of the tones by increasing c plus c x. So, what I am say over here is that why do not we increase c plus c x, that is going to reduce the tones what going to happen if I increased c plus c x.

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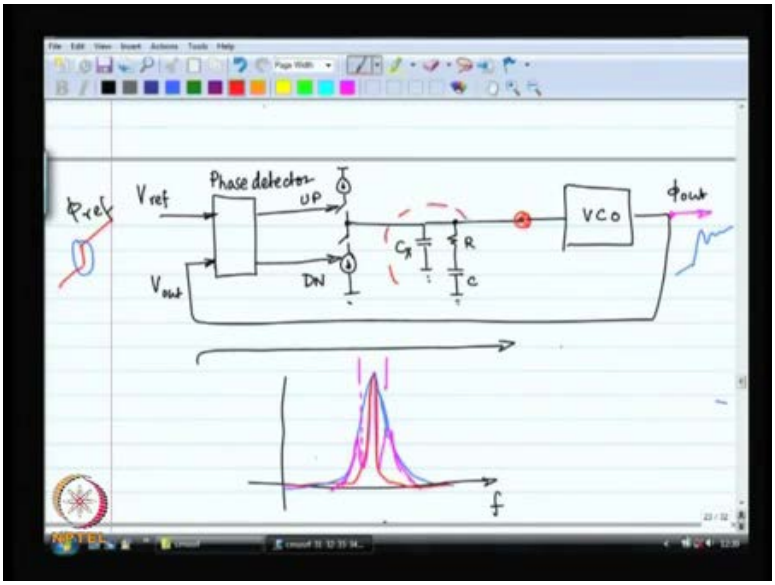

What going to happen if I increased the capacitors, if I increase the capacitance the r c product is going to increase, which means that the loop band width is going to decrease; fairly, simple if I decrease the loop band width, if I decrease the band width of this particular filter.

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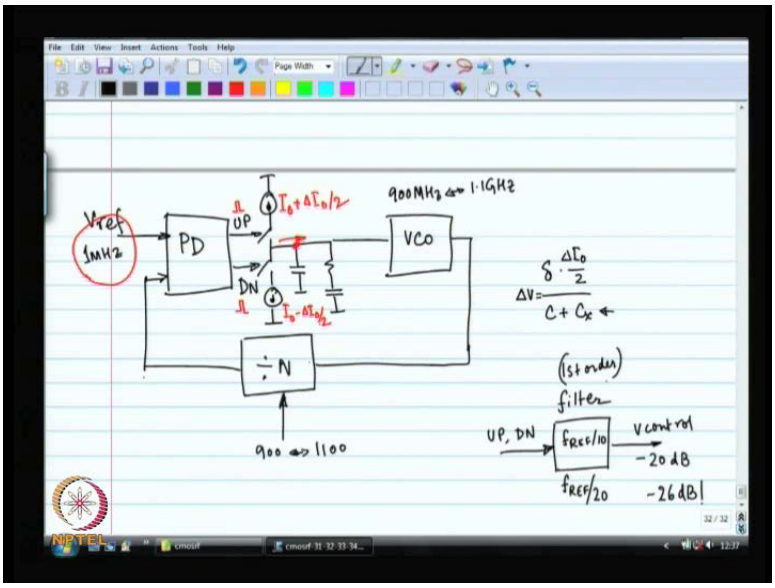

Lets retry, so this is my synthesizer n is programmable, this is the integer n synthesizer either n is programmable, let us say it is take some number here, let us say at 1 mega hertz. Let us say n is programmable between 900 and 1100 and let us say, you built a v c o to operate from 900 mega hertz to 1.1 gigahertz, so if you do a such a thing then when n is 900 the output is going to be 900 mega hertz, when n is 900 h and 55 output is going to be 955 mega hertz.

So, as I when the base station instruction you to go to a particular channel, you can go to that particular channel the step size you have got over here is 1 mega hertz. So, the channel raster, the spacing between 2 channels is 1 mega hertz that you got over here why, because you choose the reference as 1 mega hertz very interesting. So, the reference has got to be raster, the step size between the channels spacing between the channels, that is the reference frequency then you can go to any arbitrary channel that you, so desire.

Now, let us come to the point what I am saying is as follows that there are glitches on up and down, even when the circuit is large and there are mismatches between these 2 currents, as a result some extra charge goes into the control load. And when, the extra charge goes into the control load what, we are going to see is that the voltage is going to increase a little bit by this quantity that is the extra charge going in the charge divided by the capacitance is the amount of voltage increase.

So, this is the problem and what I am suggesting is increase c plus c x increase the capacitance, if I increase the capacitance the loop band width is going to drop, if the loop band width drops then effectively I am going to filter out the signal which is f ref. So, there is the signal coming in think of is a filter, your input is the up and down signal, your output is the control voltage.

So, what I am suggesting is decrease the band width of the filter, if I decrease the band width of the filter by n times, then depending on the order of the filter I get that many number of decibels, rejection. So, let us say if the band width of the filter is f ref by10, I get 20 db is a first order filter is it a first, let us say we are got first order system over here band width of the filter is f ref f ref of 10. In that case if my input is f ref, that what the input f ref and it is harmonics, then your output will have rejection of minus 20 d b per decay at f ref, at f ref by 10 everything passes.

So, what is going to happens a f ref f ref going to get 20 db lesser, what if I change the f ref by 20, then I am going to get 6 d b more improvement. So, what I am suggesting over here is that consistence, if I double the if I half the band width that means, doubling the capacitance, if I double the capacitance then the size of these delta v becomes half. So, the same phenomenon it agrees, so make the loop band width smaller you are going to get better performance, you can get rid of this completely unfortunately as you make the loop band width smaller and smaller, the v c o is going to remit the reference within that loop band width. So, that becomes a problem says noise becomes a problem.

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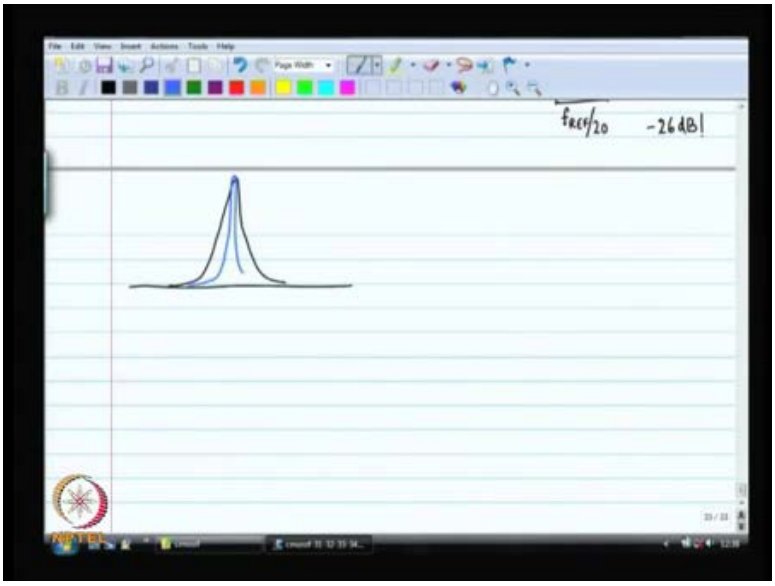

So, the output that you are going to see in the v c o, suppose this is the free running v c o output and this is the this is the output if I mimic, the reference, how you going to mimic the reference, what does it this mean by mimicking the reference, the reference is at a different frequency.

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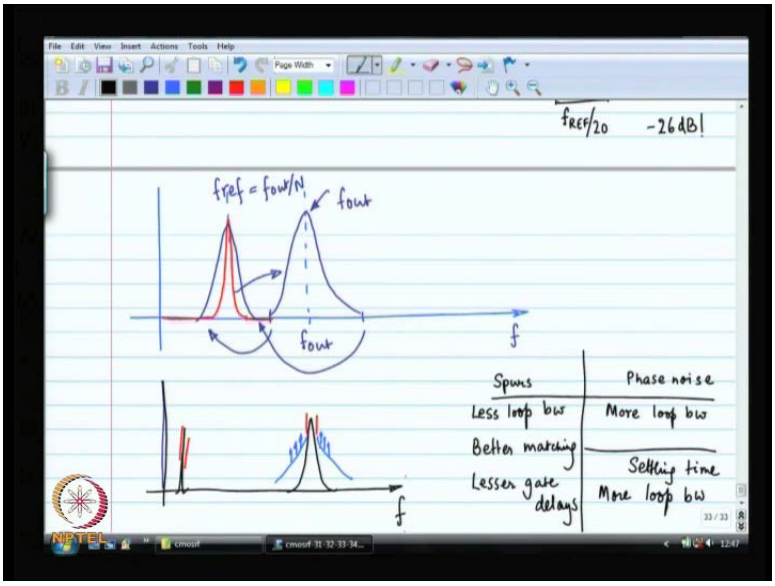

So, let us say n equal to 2, so this is sorry this is the crystal accelerator spectrum and twice this frequency is my v c o spectrum kind of exaggerating, the view put a lot of bad noise are there. Now, the comparison is between the divided output you divide the output

by a factor of 2 and then compare, each other that is you compare the reference to the divided output. So, when you divide this particular v c o output by a factor of 2 what does it mean, how is the spectrum going to look like, any guesses the spectrum is going to scale in the x axis by a factor of 2.

So, this point will translate to point by 2, this point will translate to this point by 2, every point is going to translate to that point divided by a factor of 2. So, your compressing the x axis by a factor of 2, so this compressed version is probably going to look like this I do not know, hopefully its towards in the crystal accelerator, I mean not hopefully crystal accelerator it is going to be crystal accelerator, crystal accelerator is beautiful.

So, then the job of the loop is to make sure that, when you divide it the final the job of the v c o loop is that make sure that the aero signal between these 2 equal to 0, which means that the divided spectrum is going to look like the reference spectrum. In other words, if you scale the x axis of the reference spectrum by a factor of n, n times if you make it n times then that is the extra spectrum at the output of the v c o, you get what I mean.

So, if you multiply this by n times, just the n axis point by point your going to get the spectrum at the output. So, therefore, what I mean by saying that the output has got to mimic, the reference is really not quite the statement, it is not exactly correct the output has to mimic, a scaled version of the reference the x axis has to be scaled n times. So, if you are reference looks like this, then you have to take point by point scale it up, expand x axis may be this is how, the output spectrum will look like, the scale reference is going to look like.

Now, what this mean as far as our synthesizer is concerned is that within the loop band width remember, but the loop band width is only this much that is the strange part, that the loop band width is only that much. So, within that loop band width the output is going to mimic the reference and outside that loop band width, it is going to behave exactly as if it were the normal v c o.

So, our job is make sure that the loop band width as largest first possible, so I can get rid of as much phase noise are possible and then quarterly, we are saying that reject the outputs as much as possible, some spars over here to reject the spars as much as possible I would like to keep, the loop band width as small as possible. Now, comes the

engineering tired of you have to figure out, how much exactly loop band width you are going to allow accordingly you have make a very good voltage control oscillator.

So, that do not create too much extra phase noise, accordingly you can relax on the delay of the and gate, and of the flip flops, and on the mismatch between the up and down currents of the charge pump. So, these are the trade off, what about settling time, well less loop band width means, automatically means, that the settling time is going to be that much more too bad.

So, if you want a improve spurs performance of the spurious frequency, you want to reduce the spurious frequencies, then you have lower gate you delays, you have to have better matching between the up and the down currents, you have to have lesser loop band width. Unfortunately, if you want better phase noise you need more loop band width, if you want to have lower settling time then you want to have more loop band width. So, lot of reasons why you want to have large loop band width and so there are lot of reason, why you want a have a large loop band width. So, either you leave with the spurious frequencies or you have to do a better job with the matching between the potion pull current, up and down current, and you have to have lower gate delays.

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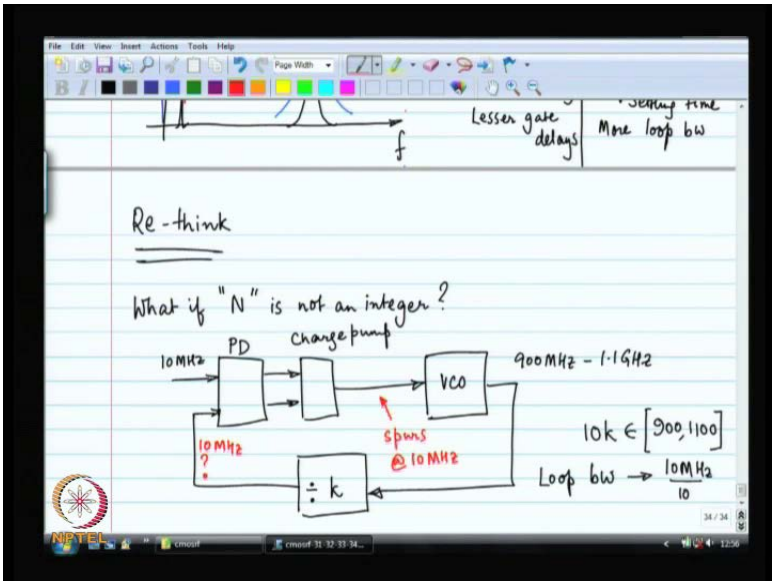

The other possibilities is a Re think, what if N is not an integer, lets re think let us say that here we divided by a number n that was architecture, what if I do not divide by n integer, I have restricted n integer I say that lets try to design a circuit, which will make it

in the future. Suppose I make a division some sort of divider circuit, which divides by non integers by any number, any real number.

In that case the reference oscillator does not have to be the channel spacing, remember the reference oscillator is the channel spacing in our integer n synthesizer integer or division, reference oscillator running at the channel spacing, which means that the loop band width fraction of the channel spacing. And it also means that you are going to get spurious frequencies at the channel at precisely the channel spacing, which means that at every channel, you are going spurious frequency is ridicules everyone else.

So, the suggestion is that what if I make n to be a non integer, let us not think about the spurious tones, now if n is allowed to be not an integer then the reference frequency does not happens to be the channel spacing. Suppose I want to arrange between 9 hundred mega hertz and 1.2 gigahertz at a channel spacing of 1 mega hertz, but I am allowed to do division by not only integers, but 1 tenth of integer also. So, I can do division by 9 hundred 90 point 1, I can do the division by 90 point 2 and so on, so forth.

In that case my we f ref could be10mega hertz think about this, so if I am able to divide by k, where 10k is number integer between 900 and 1100, I mean in this just a thought it might not be what you are going to do, but this is just a thought. So, I am allowed to divide by 90, I am allowed to divide by 90 point 1, k can be 90, k can be 90 point 1, k can be 100 point 5, k can be 100 and 2, k can be 100 and 2 point 1, k can be 110 will it work, will it work better than before, why it can work better than before, it can work better than before for the simple reason, that now the loop band width, maximum loop band width is going to be fraction of 10 mega hertz.

So, earlier my loop band width was a fraction of 1 mega hertz, in this case I have manage to increase my loop band width 10times, is not that nice quite is nice. Because, now I can improve my performance as far as phase noise is concerned, I can improve my performance as far as settling time is concerned, I can settle luster I can have my oscillator will a lower requirements as far as phase noise is concerned, you would not have to worry about your phase noise, next to my oscillation frequency.

So, it will mimic the output of the synthesizer or mimic, the reference with a larger loop band width 10 times larger loop band width, that is the lot as far as that means, a lot to me. We look at the importance of phase noise earlier on can be there working in next

source right. So, v c o is noise going to be relevant within that loop band width outside the loop band width of course, the v c o should have good phase noise performance.

So, this is the better approach what you think, now we cannot really say what this is going to do as far as spurious frequencies are concerned. So, that is question mark, because we do not k now what the signal looks like with do not exactly know what is the signals looks like, most probably not going to exactly10 mega hertz, if we dose if we does look exactly like10 mega hertz, then is there is problem there is no problem as far as the spurious tones are concerned, spurious tones will start appearing at 10 mega hertz apart instead of 1 mega hertz apart.

So, that is clear if it is also a 10 mega hertz signal, may or may not be at all depends, how I do this division, so supposing it also looks like a 10 mega hertz signal in that case the spurious tones will appear at spacing at 10 mega hertz. And, Since my loop band width is 1 mega hertz 10 mega hertz will have the same 20 d b rejection as before here whatever I was getting in 1 mega hertz I will get the same tone, but10mega hertz. So, in that sense also this is kind of better since to be better, so this all need only stumbling block is nothing, how can you possibly divide a frequency by a non integers. So, our traditional digital circuits I can make a counter which I mean with my flip flops and so on, this is what we have done to make the division.

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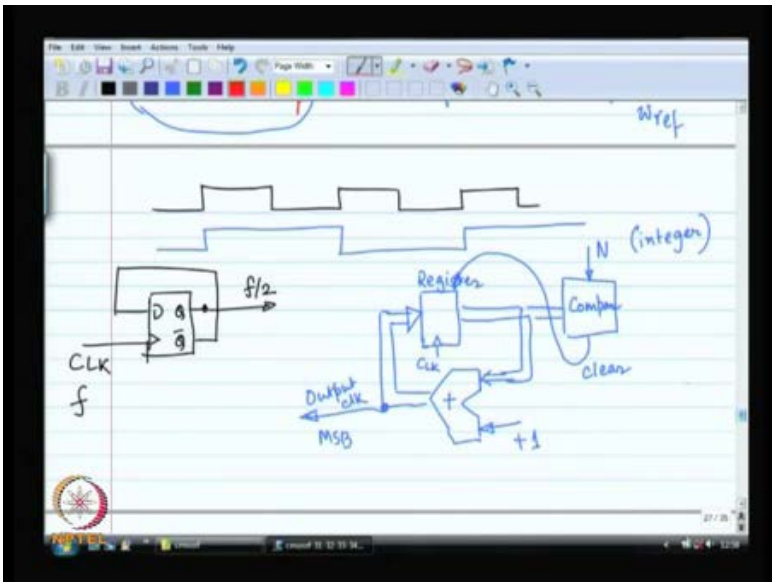

And this is kind of not good work with non integers, so this is a problem how we going to make this division by k, so everything is fine in theory on paper it looks like this is going to perform better, is definitely going to perform better in terms phase noise, is definitely going to perform better settling times, performance in terms of spurs looks like is going to be better on paper, will have to be examine that only question mark over here is what is inside this division by k

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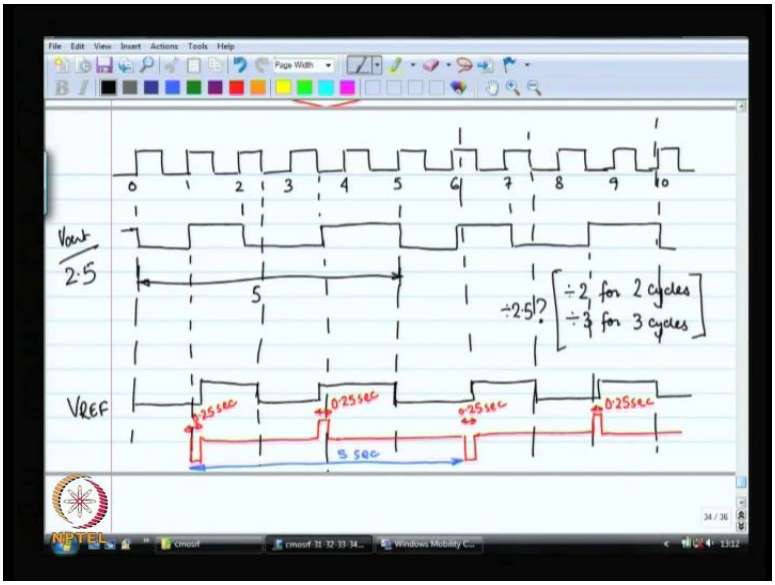

So, let us try to divide by a non integer and as an example let us try to do the following, let us say, that I have got a clock running at 1 hertz and I am going to follow this algorithm, that every 2 clock cycles I am going to divide by 2. So, far 2 clock cycles I am going to divided by 2 and for 3 clock cycles I am going to divide by 3, so funny kind of situation 2 clock cycles I am going to divide by 2. So, from here to here I am divide by 2 cycles and next 3 clock cycles I am going to divide by 3, again for 2 clock cycles I m divide by 2, and for the next 3 cycles I am going to divide by 3, what the output of this want to look like, the outputs going to looks like this.

So, I divided by 2 for 2 clocks cycles and then, I want to divide by 3 for 3 clock cycles and this going to be periodic is going keep repeating itself, at what rate what is the total period of this is the total period of this 5 seconds, It is going to keep repeating 5 seconds. Now, what does this look like as far as the phase detector is concerned does this look like a signal.

Which has a period of 2 point 5 seconds or other as far as the phase detector is concerned do you think you have successfully divided by 2 point 5, divided by 2 point 5 means a period of 2.5 seconds, well on the average it is like this you got 5 seconds, in 5 seconds you got 2 cycles got 2 up and down. And the average cycles seems to be lasting 2.5 seconds is that not, so average cycles seems to be lasting 2.5 second, which means that this like you have a successfully divided your whatever was coming from the v c o by 2.5, so looks interesting.

Now, let us say that the reference was at 2 point 5, 1 by 2 point 5 hertz is point 5 hertz, so this is 1 that needs to go high 1 point 2 5 second then lower 2 point 5, there is going to go high at 3 point 7 5 little before, this comes then low at the right point and this is going to be. So, this is let us see the reference, now this is the reference let us examine what our phase detector is going to do, we are going to do same phase detector.

Now, the output of the phase detector is going to do the following, first the edge of v I going to 2 point 5 comes, so it is going to give you a down palaces then the edge of v ref comes things are going to be stabilize. So, this is for quarter of second, then after a long time the reference goes up first, then quarter of second later stabilizes then again is a down palaces of a quarter of second. And no is a down palace for a quarter of second, I think alignment problem here this should have been the off palace for the other quarter of the second, this is going to be the output of my face deducted.

Now, this looks brilliant does not it up and down of the equal durations different points of force of course, it is beautiful is not, it very nice which means if everything is perfect then things are going to nothing, is going to change as far as the control voltage is concerned, if nothing changes as far as the control voltage is concerned then the output of v c o does not change, which mean you have got lock.

So, you have successfully divided by point 5, now if I can do 2 point 5 I can do any other fraction, I just have to spend time on it, so this is something which is very interesting is not it what is the periodicity of it palace. So, without any loss of generality if I can do 2.5 I can do other numbers as well this is basically the strategy, I am going to follow. We now have the technique to do this division.

Next question is what does this mean as far as are concerned, we think that frequency is that correct the reference frequency is 1 by 2 point 5 hertz are the spurs coming 1 by 2

point 5 hertz or at some other frequency, what is the periodicity in the face detector output, what is the period. The period, is the net period which happens to be 5 seconds in our case 5 seconds means that, we are really getting is spurs at 1 fifth of a hertz point 2 hertz, not point 4 hertz.

So, this is the story, so this spurs are not going to coming at 10 mega hertz are spurs not coming at the reference frequency, here the reference frequency was point 4 hertz. But, this spurs as far as I am concerned are coming at point 2 hertz, even slower rate periodicity in the spurs is lesser period is more. So, if the spurs are not going to come 10 hertz, this spurs are going to at the fraction of 10 mega hertz.

So, now as far as my loop band width is concerned, I have made my loop band width equal to 1 mega hertz also spurs are coming at 1 mega hertz, let us say in that case spurs are going right through problem, spurs are almost with in my loop band width. In fact, they are going to be within the loop band width for larger, ratios for larger, for deeper fractions now fine.

So, the understanding is first, let us try to understand how we did this magical division by 2 point 5, how did we do the division we took 1 we took 2 periods, 2 cycles during which I divided by 2, and I took the next 3 cycle and divided by 3. So, over 5 cycles I have done my job and for some of this 5 cycles, I have divided by 2 some of this 5 cycles, I have divided by 3 let us try to generalize.

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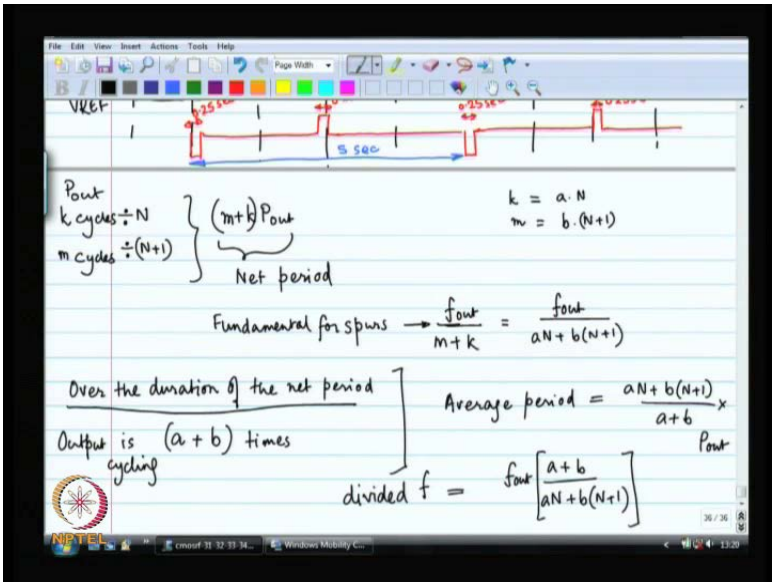

Let us say that I take the lot of these cycles and for some cycles, I divide by m and for some other cycles, I divide by n plus 1. Let us call them k cycles and m cycles, so for k cycles I am going to divide by capital n, for m subsequence circles I am going to divided capital n plus 1, it is fissile to do this with digital circuit. So, let us say output has the period of p out, so the total time during that I am doing the experiment is k times p out plus m times p out.

So, this is the total period during, which I am doing my experiment and of course, m plus k times p out is going to be the net period and if, this is net period then this spurs are going to appear at 1 by this. So, fundamental for spurs 1 by m plus k times p out, p out is f out. Now, what is this fraction by which we have managed to divide by, let us try to understand what this fractions is, k clearly has to be got the multiple of n, and m clearly has got to be the multiple of m plus 1.

So, k number of cycles has to be something times n, otherwise you cannot divide by n nicely and m cycles you want that to divide with plus 1, so that also has to be some multiple of n plus 1. Otherwise your division is not really quite gone work out, so that means, this is equal to, that is the net period that I have got. Now, over this net period over the duration of the net period, how many cycles, how many time is the divided voltage going up and down that is the question.

So, as long as I am dividing by n I am dividing k cycles by n, so it is going go up and down a times, during that division and it is going to go up and down b times, while I am dividing by m plus one. So, the output of the clock divider is going up and down a plus b times over the duration of net period, which means that the average period or rather the reference period as got to be equal to this net period divided by a plus b, net period is equal to a n plus b n plus 1 whole thing times p out.

So, that means, that the frequency at the output of the divided is 1 by the period times and 1 by p out is basically equal to f out. So, the quantity by which you have done division is this a n plus p times, m plus 1 divided by a plus b.

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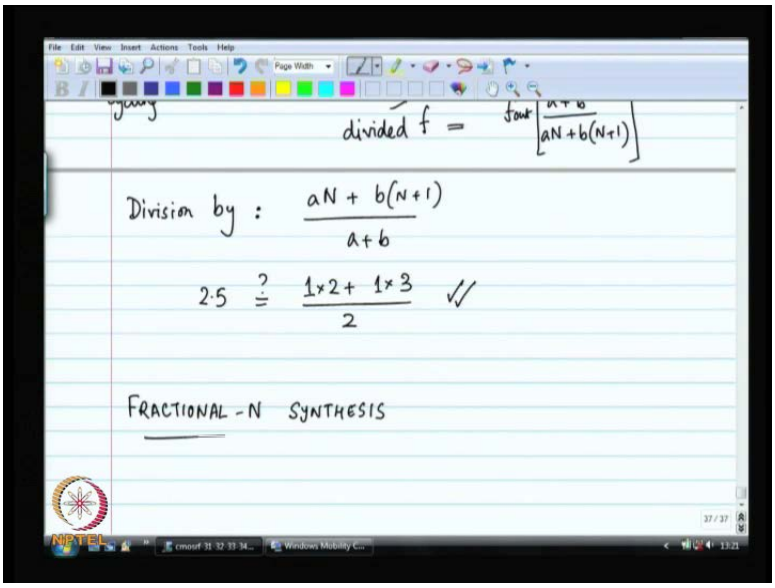

Now, this does work out as far as example was concern we said that we have done the division by 2.5 is that equal to 1 cycle times n it is right. So, therefore, this formulation is correct is way of checking whether work have done whether it is correct or not and basically you now choose your n choose n plus 1 a and b and you can get different kinds of fractions as far as you are concerned.

So, we are going to summarize here we are going to get into more details as far as this division is concerned in the next class this technique is called the fractional l frequency synthesis I am giving you the name after doing the whole thing let us stop over here and we are we are going to carry on in the next lecture.

Thank you.