CMOS RF Integrated Circuits
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Module - 11
Frequency Synthesis
Lecture - 33
PLL Dynamics Integer N Frequency Synthesis

Welcome back to CMOS RF integrated circuits in this lecture we are going to discuss dynamics of the phase lock loop and then we are going to move on to study about a integer and frequency synthesis. So, in the last lecture we were talking about a phase lock loop. So, I had built up a phase lock loop in general how to a reasonable topology of a phase lock loop looks like. So, we had built a phase detector we went into the complete a circuit for the phase detector there will be 2 flip flops and gate clear, state machine diagram and so on. The phase detector generates 2 signals which are basically 2 bits of a 2 bit binary code is for plus 1 minus 1 or 0.

So, these to bits are called up and down and then we have a some sort of current steering deck I am going to call current steering deck if you look up the books it is called a charge pump and this digital value is converted to an analog representation over a capacitor now. If I just use a plane capacitor then unfortunately the system becomes unstable because there will be 2 integrators in a loop and I cannot do that. So, instead we have this combination of a capacitor and a resistor capacitor series and this particular impedance will have a pole at d c it will also have a 0 and another pole.

So, that is basically the idea and this voltage is used to control the VCO the voltage controlled oscillator. This is a phase lock loop in general we said that our analysis works only when the loop band width is some fraction of the oscillation frequency something like one tenth of the oscillation frequency. So, that is when the phase lock loop really is going to work now unfortunately we want as larger loop band width as possible which means that I want exactly that much loop band width which gives me. I want exactly the maximum amount of loop band width where the dynamics still works according to our mathematical model after phase lock loop and the reason why is because I want the VCO to have the phase noise properties of the reference oscillator.

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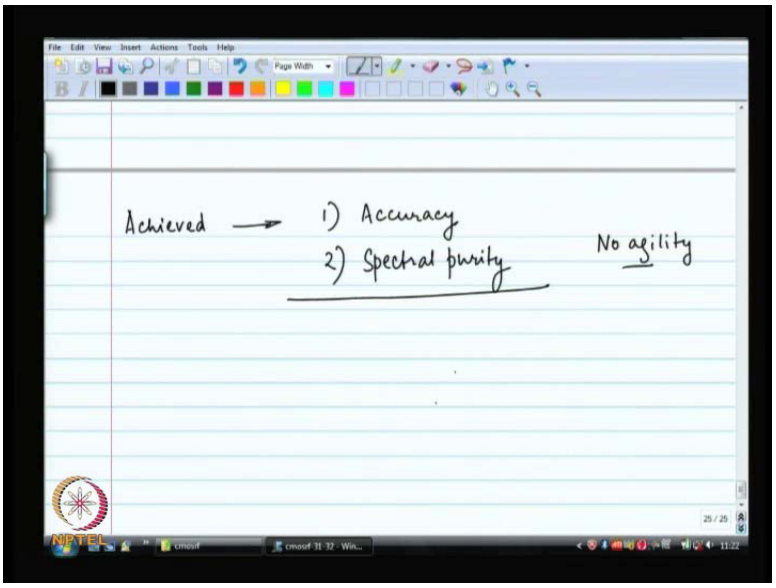

So, what have we achieved with this if the reference oscillator is oscillating perfectly at 1 giga hertz with 10 ppm of variation then the local oscillator the voltage controlled oscillator is also going to oscillate exactly at 1 giga hertz with 10 ppm of variation. So, I have got accuracy what else have I got accuracy in terms of a number what exactly is the frequency I have also got spectral purity within the band width within the loop band width I have got spectral purity outside the band width of the phase lock loop the voltage controlled oscillator does whatever it wants to do, but within the band width the phase is controlled by the reference phase. The reference phase is being tracked.

So, the phase of the voltage controlled oscillator is equal to the reference phase right. So, you have got spectral purity there. So, these are the two things that we have achieved we have not achieved any kind of agility, before I move on to the next part I want to kind of understand what is going on. First of all does frequency a does phase lock also mean that a oscillators will have the same frequency.

So, what I am saying is that phi out phi out is equal to phi f if phi out is equal to phi f does that mean that the derivative of phi out that is the frequency is equal to the derivative of phi f the frequency of the reference absolutely there should be no mistake in that that is great news. So, you get a perfect frequency synchronization you get phase synchronization next question is will this always work what if my voltage controlled oscillator is unable to generate such a frequency or what if the voltage controlled

oscillator is able to generate such a frequency with great difficulty. So, the answer to all this is something called lock range.

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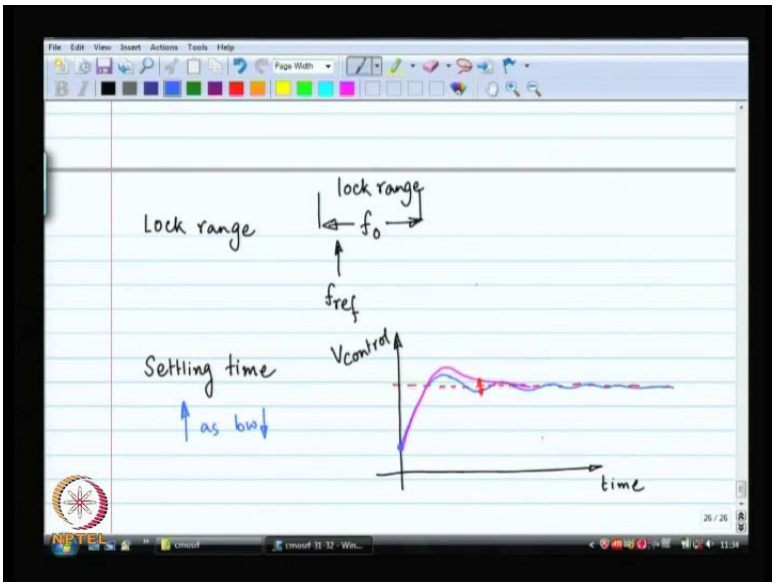

So, phase lock loop has a lot of these properties lock range is one of them. So, the voltage controlled oscillator has a certain center frequency free running that is that is the frequency that it is going to oscillate at and if the reference frequency is anything within the lock range of that. So, if the reference frequency is out, then the voltage controlled oscillator will be able to lock to that reference frequency.

so there are lot of these properties of phase lock loops. Now we do not want to get into all of these details I really want to move on to the next topic, but then this is of some interest because you want to make sure that when you have made your voltage controlled oscillator over the entire range of process corner variation, etc. The reference falls within the lock range of your standalone oscillator around within the lock range centered on the free running oscillator. So, you want to make sure of that what else next thing is how much time it takes to settle. So, if you build a phase lock loop and you switch it on you switch on your reference frequency all of a sudden then the phase lock loop is going to try to lock. Now if I plot the control voltage to the VCO as a function of time may be this is the control voltage that is suitable for frequency lock. This is the control voltage that is the correct one you start it off let says initially the control voltage is over here. when you start it off or may be its at 0 volt may be let say it is over there.

So, what is going to happen is depending on the transfer function. So, you have got a lot of these poles, zeros, etc. what is going to happen is this voltage is going to try to reach the target it could go in that fashion it could also go in a different fashion it could do something like this or if you have not paid attention to the values of the resistors and capacitors then it might not even settle ever in which case it is going to go like this. So, all of these are possible these are all dependent on what are the resistors capacitors that you have chosen over there how exactly you have built the loop what is the precise transfer function where are the poles and zeros what is the damping factor we like damping factors of something like square root of 2.

so you need to read up all of this in your control theory book. velocity control you can also read up all of these in a book, which has a chapter on phase lock loops dedicated to phase lock loops how exactly to choose the damping factor how to choose the resistor value and the capacitor value, etc. but we are not going to go into too much detail as far as this is concerned. now settling time is this something of great importance it is something at most importance because if your base station asks you go to this frequency now it is going to give you a certain amount of time to reach their and your settling time you have to reach there that particular frequency within that time allocated to you. So, you have to worry about it. Now definition of settling time. No concern what you are really finally, trying to do is achieve oscillations with a certain amount of jitter or certain amount of phase noise. So, you want to reach your target value with a certain amount of accuracy. So, that will decide how much time it has taken for you to reach the target frequency. now the next thing is what does this settling time depend on do you think the settling time will be more.

If the band width is less or the settling time will be more if the band width is more the loop width what do you think does this or does this settling time have anything to do with the loop band width at all. This loop band width the settling time will be less if the loop band width is more. Settling time will be more if the loop band width is less why because if I put an impulse think about it over here. if I put any put a some sort of a. So, phi f is a ramp, but supposes I have a step on top of the rank.

Wherever the step is there are extremely high frequencies at that point of time. So, there are high frequency components. now your control system has to track these high frequency components if it has infinite band width then the output also will look exactly

like that, but unfortunately you cannot build your control system with infinite band width. We have some restrictions right that means, only certain components up to certain components can go through, which means that your phi out phi out is going to try to behave like that.

But unfortunately because some high frequencies are blocked out by the loop it is not going to be able to mimic exactly what phi f is doing. So, this is basically the idea. The larger the loop band width the better phi out is going to look in relation to phi f, which means that the settling is going to become faster. if you block out most of the high frequency components then your system is going to slow down and as a result the loop is going to stabilize with a much larger settling time.

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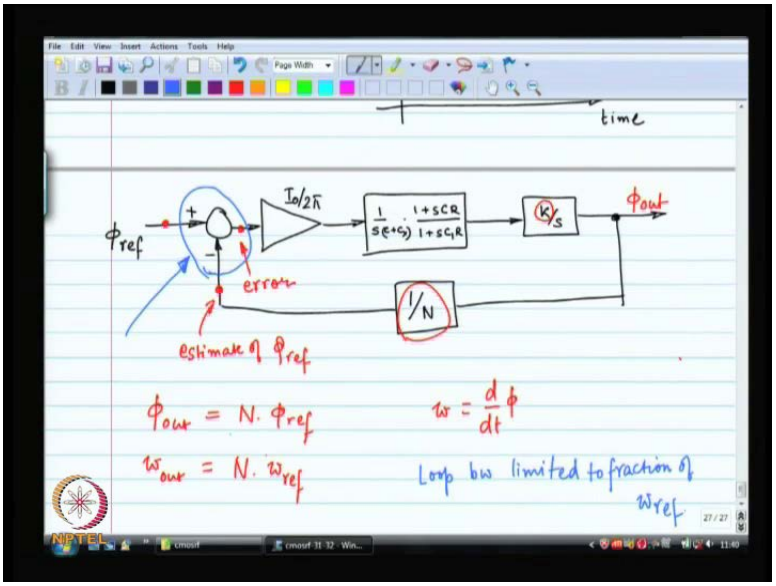

Now, let us move on right is it conceivable this is my phase detector. So, this is the normal phase lock loop what is going to happen if I put a division by N in the feedback path will this loop also work off course this loop will work I mean it has the same dynamics as before it is just that effectively instead of having K by S you now have got K by N by S.

Some gain is there 1 by N gain is there in the loop. So, you just have to work your way for that 1 by N gain otherwise it will work, but the question is this what is now going to be the relationship between phi out and phi f is phi out going to track phi f or something else is going to happen. you see whenever you have feedback the idea is that this is the

error signal this is called the error and the job of the feedback loop is to make sure that this error is as small as possible that is how you think of any feedback loop you have got an error signal the job of the feedback loop is to make sure the error is as small as possible which means that these two points, one is phi f the other should be an estimate of phi f which means that phi out is now going to be equal to N times phi f.

So, nothing a drastic it is just that phi out now, has to be N times phi f what does that mean as far as the frequency goes the phase is N times the reference phase frequency id duo by d by d t of the phase is equal to the frequency. So, the frequency is N times the reference frequency very interesting. Now what are the what is the constraint now at the loop band width.

we said that the loop band width is constrained over here right to 1 tenth of the oscillation frequency, which oscillation frequency are we now talking about why did the loop band width get constrained the loop band width got constrained because of this particular block this block is not really there, it is not exactly like that. I do not have a plus minus over there. I have got two flip flops they are giving me. Digital output and the time for which it is 1 or minus 1 gives me the estimate of the phase error.

So, there is an averaging that I am implicitly doing over there in my analysis. So, that is where the phase the band width limitation of my control system came, where the analysis is incorrect and because this analysis is incorrect I cannot arbitrarily increase the band width that is the story. So, what frequency is this happening at what is the oscillation frequency as far as this phase detector.

Oscillation frequency is omega f, which means that my loop band width should be limited to 1 tenth of omega f not 1 tenth of omega out. Now how are you going to divide this phase is it possible to do such a thing I mean a first of all is this a something interesting, do you want to build this is not this something interesting omega out is N times omega f. I can have even a reference frequency of 10 kilo hertz and if N is 1 million. I can generate 10 giga hertz. So, it is something very interesting, I can use a low frequency as far as omega reference is concerned, but I can generate any high frequency as far as omega out is concerned. So, seems like it is something which could have some utility. Now how are you going to make this 1 by N how are you going to divide phase is

it possible to divide the phase of a signal. Now the saving grace over here is that this signal this phase is in the form of a digital clock.

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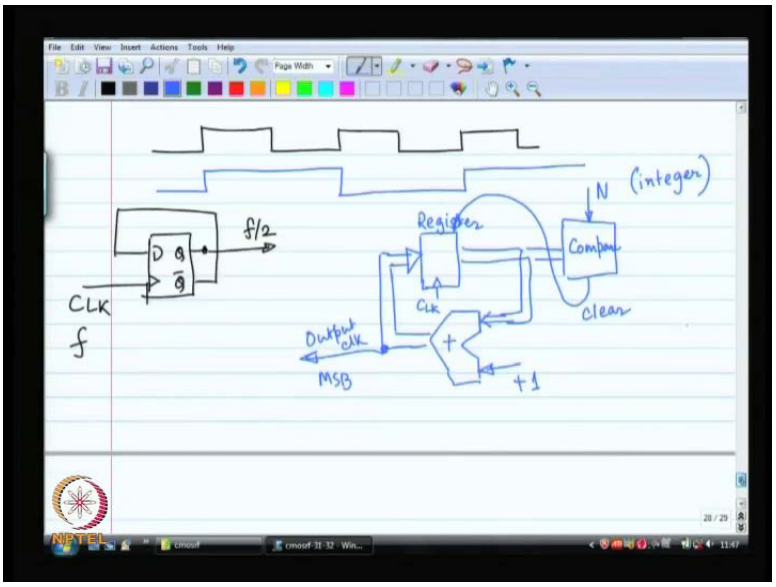

So, Vout really looks like this. It is a digital clock and is it possible to divide the phase of this clock what does it mean when you say lets divide the phase of this clock. it means you also divide the frequency of the clock by a factor N. how do you divide the frequency of a clock by using a counter. So, for example, divide by 2 counters with 1 flip flop, take the output from anywhere take the Q output. For example, so, this is the clock running at frequency f and this one will be running at f by 2. So, if I use this as my circuit over here I am going to get. So, on wonderful.

So, I can use my knowledge of digital sequential circuits to build counters and that can help me in dividing a clock by N now. This N could be anything N is 2 that is the example that I have drawn over here. N could be any number for all that you know N could be a large number. You could a conceivably have an adder every clock side you add one. So, let us say I have a register I am just drawing crude very crude this is not how it is done this is not how it is done.

But anyway I am still drawing it just to I could imply something like this and every time the resistor hits a value of N whenever it hits a value of N, I am going to clear the resistor. Now, N can be programmable from outside and I have successfully divided which is the output lock over here well the output lock could be the M SB of this

something like this will work just that this is no not how it is done because of speed and other reasons.

So, finally, this is not the implementation that we use. However, this is a crude possible circuit. Could use an adder whenever the result reaches N you clear it take the output from the MSB. That will successfully divide your input lock by a factor N. So, it is conceivable to divide your clock by an arbitrary number N now only thing is N has got to be an integer that is all.

It is a easy if N is an even number also otherwise you are going to have trouble in generating fifty percent duty cycle, but if N is an even number then you can have fifty percent duty cycle. So, that is basically the taught process its possible is conceivable to build such a clock divider now let us just calm down right lets calm down and think about what is going on over here let us say that we are dividing by 4.

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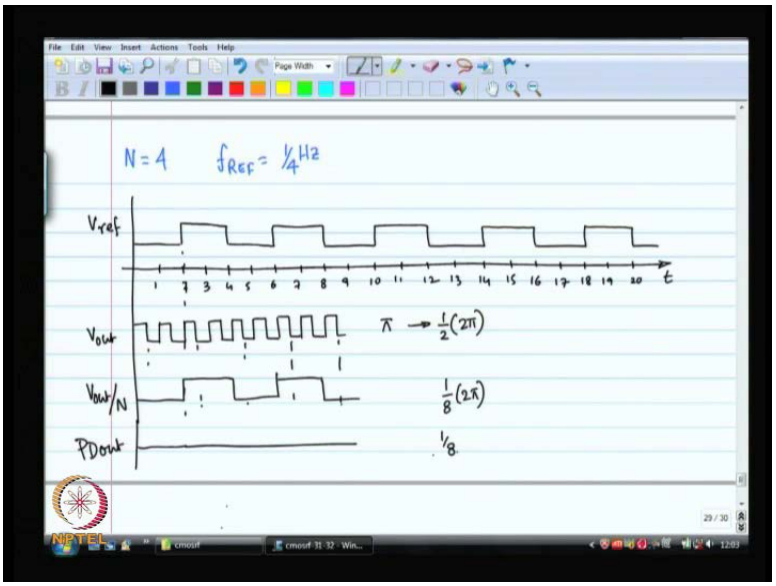

Let us say N is 4 and let us say we are working with the 1 hertz clock f ref is 1 hertz. Just for convenience I want to see what phase detector output looks like, etc. So, as a function of time let me first plot the reference equation the reference voltage. So, the reference voltage probably looks like this.

Now, let say that initially the VCO output is at 1 by 3 hertz let say initially the VCO output was that 1 by 3 hertz if the VCO output is at 1 by 3 hertz then I am sorry.VCO

output is a 3 hertz, 3 hertz will be how to show over here. I have got to change my scales sorry about waste of time over here. Let us say that is my f REF and the target output frequency is clearly 1 hertz, N is 4. However, let say instead of 1 hertz initially my VCO was giving little less than 1 hertz may be 0.6 hertz or something let say this is what the VCO was doing initially. running slower than required now in that case when I divide this by 4 as I divide by 4 counter that I have got and the divide by 4 counter what it is going to do is its going to count 2 cycles then it is going to change its phase.

Now what does this mean as far as the phase detector is concerned it is not really Vout by N its Vout the division is in the frequency domain. So, what is going to happen to the output of the phase detector. So, this is running really slow, this is going to be compared with V f is at different frequency all together and output of the phase detector is going to go to 1 at the plus 1 at the rising edge of V f and its going to remain there till you get the rising edge of the other frequency then it is going to come to 0 immediately there is another rising edge of V f which means again it is going to go back to 1 and its going to stay there forever till the next.

Situation arises now what does this mean as far as we are concerned this means that the phase detector is telling you that hey you need to increase frequency this is the up you need to go up in terms of frequency. So, the VCO responds and goes up in terms of frequency because up signal is coming up signal is coming means that the control voltage is increasing, now if the control voltage increases supposing the VCO responds to the control voltage in the correct direction, if it does not then we have a problem we have to invert the signs. So, the control voltage increases and as a result the output of the VCO increases in terms of frequency.

The output of the VCO does not look like this keeps going up in terms of frequency till it reaches till it becomes faster significantly faster suppose it now becomes point 5 hertz. It is still not 1 hertz in that case what happens to give output of the counter the output of the counter accounts 2 cycle then goes high again counts 2 cycles then goes low, etc. So, once again the output of the phase detector goes up at this point of time and then it comes down, but sure it comes down and then again it goes up and remains up for a very long time. So, you see that the phase detector is again telling you that you need go up in terms of frequency increased frequency become faster speed up. Now suppose the VCO

speeds up even further and instead of point 5 hertz now it is running at 1 hertz, but with some funny phase alignment.

It is not aligned to our reference. So, VCO is now running at 1 hertz, but I am going to put a lag of 180 degrees. So, suppose this is how the VCO is running in which case the divide by N is going to be something like this. I am sorry I drew it incorrectly. So, it is going to count 2 cycles and then it is going to go up. So now you see that the frequency of Vout by N and V f are the same. However, there is a phase misalignment now let us see what happens. So, what is going to happen is the output of the P d want to go up come down. then again it is going to go up and come down and notice that now the output of the Pd is on for an fraction of the time is up not permanently like before. So, when the frequency is different when it slower up really goes high.

Now, it is on for a fraction of the time how much time is it on for its on for half a second output of every 4 seconds. So, for one 8 of that of time you have got up remember I put a phase lag of pi degrees over here pi degrees typically corresponds to its half of 2 pi . So, half of 2 pi degrees is the phase error that I constructed I put lag of half of 2 pi degrees 2 pi radians over there now the phase is been divided by a factor of 4 which means over here I am getting a lag of 1 8 of 2 pi radiance 1 eighth 2 pi radians corresponds to a voltage of 1 eighth 2 pi radians corresponds to voltage of 1 as the P d output right.

So, that is what happens. So, the time average remains the same its 1 eighth and I am only getting up pulses why am I getting up pulses because the output of the VCO is lagging behind by some radians. So, the output of the VCO needs to speed up the VCO needs to speed up its lagging behind. So, eventually everything falls into place and a supposing this square the output of my clock divider then my up and down signals would disappear all together. So, the Pd output would remain 0 does it remain 0 does it remain 0 or do you see something is the Pd output 0 well recall that up and down of the phase detector are both going to be equal to 1 for a brief amount of time.

If both the clock edges come together. So, suppose v f and v out have their edges together. So, when both the clock edges come at the same time plus 1 and both of these outputs up and down outputs become one at the same time. That means, that after a delay little bit of delay the delay and gate the clear signal gets activated and by the time the clear acts we have got a little bit of delay. So, there is a short duration of time during

which both up and down are high at the same time now if you made the dack over here current steering dack up and down or high at the same time it should not matter up and down or high at the same time fine I 0 goes in I 0 comes out no charge accumulates on the capacitor it is all clean unfortunately this is not the case right up and down are high together for a brief amount of time unfortunately these 2 current sources I 0 and I 0 are never going to be exactly equal to each other.

They are never going to be exactly equal to each other what does that mean as far as we are concerned. That means, that the output of the phase detector is going to see a deep pulse over here both for up and down now if the dack was ideal this pulse is irrelevant unfortunately. The dack is not ideal the currents will have some mismatch around each other now if the currents have some mismatch from each other.

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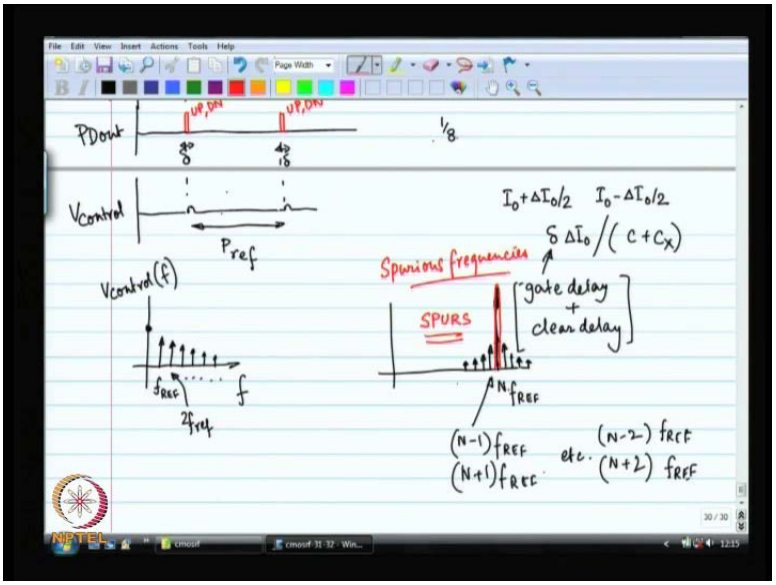

Let say the up current has a little bit 1 percent more than the down current that will mean that there is going to be a 1 percent charge accumulation on the capacitor there is going to be. So, if I now look at V control the control is going to see a little glitch over here. Because little bit of charge accumulation on the capacitor is that understood why there is the glitch over there. So, there is a little bit of glitch V control is accumulating little bit of charge and at what frequency is this happening first of all how much charge is being accumulated.

Let say I have got I 0 plus delta I 0 and I 0-delta I 0. So, let say these are the 2 currents that I have got delta I 0. So, the mismatch between the up and down currents is delta I 0. So, this delta I 0 is going through for what duration the duration is the delay of my gate this duration is same every time delta amount of time gate delay + the delay for the clear to work. So, if you make that delay equal to 0 then once again it does not matter if the currents are mismatched.

So this is the total amount of charge that is going in through this charge pump. this charge off course is going to get accumulated on to that capacitor which means Q equal to C v remember the voltage that you get the extra voltage that you get is this divided by the capacitance C + C x that the extra voltage that you are getting. if this capacitor size is extremely large then it should not matter this delta voltage is close to 0 that is also true. Now next is what is the frequency of this happening at what frequency is this happening what rate is this happening what is the period of this non ideality what is the period what is the period that I have got some 2 seconds to six seconds. So, exactly 4 seconds, which happens to be the period of my reference.

So this glitch is happening at exactly the reference period what does this mean this means that if I look at the spectrum of V control if I look at the spectrum of V control as function of frequency off course v control the final value should have been a constant voltage that is what you wanted a constant voltage over there if you have a constant voltage as v control then you are going to get a perfect frequency output of the VCO plus phase noise, but off course.

Lets ignore phase noise for now let say that everything is noiseless perfect in which case V control is a constant voltage then I will get an get a tone as far as VCO is concerned that is what I want unfortunately V control is not a constant voltage V control has some periodicity with frequency f. So, V control has a large DC component which is what you wanted it also has periodicity with repetition rate f REF it has all the harmonics what does this mean as far as the output of your VCO is concerned very straight forward the output of the VCO will have all of these components. In addition to the fundamental.

So, the output of the VCO will be your N times f ref impulse at N times f REF, but in addition to the impulse at N times f REF sees if the control voltage had been a perfect DC then you would get this as the output. now I am saying it is not a perfect DC it has all

of these extra stuff in it which means that you are going to get tones corresponding to those extra stuff around the carrier is this clear.

What is the rate what is where are those tones going to come at the tones are going to come at precisely (N-1) f REF (N+1) f REF, etc. (N-2) f REF (N+2) f REF and so on. So, these are the components that you are going to see at the output of the VCO now the good news is that the band width of the loop is the fraction of f REF which means that within this band width.

Your output it is a fraction of f REF it is by f REF ten it that band width the output is going to reference oscillator outside that band width whatever else could possibly happen is going to happen this is what is going to happen. So, nothing is going to get filtered outside the band width of the loop. So, we are going to summarize this all of this phenomenon these are called spurs. So, in one word these are called spurs or spurious frequencies. So, whenever you have designed a frequency synthesizer like this you are going to get all of these spurious frequencies this frequency synthesizer has a name it is called the integer N frequency synthesizer. Now we are going to stop at this point of time and we are going to carry on from here in the next lecture.

Thank you.