CMOS RF Integrated Circuits
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Module - 11
Frequency Synthesis
Lecture - 32
Charge Pump

Welcome back to CMOS radio frequency integrated circuits, we are in the middle of eleventh module, we have been discussing frequency synthesis and part of frequencies as part of frequency synthesis, we were first discussing the phase locked loop.

So, in this lecture I am going to introduce to you the charge pump, and move on, and build up phase locked loop, but before that brief recap what we all have done.

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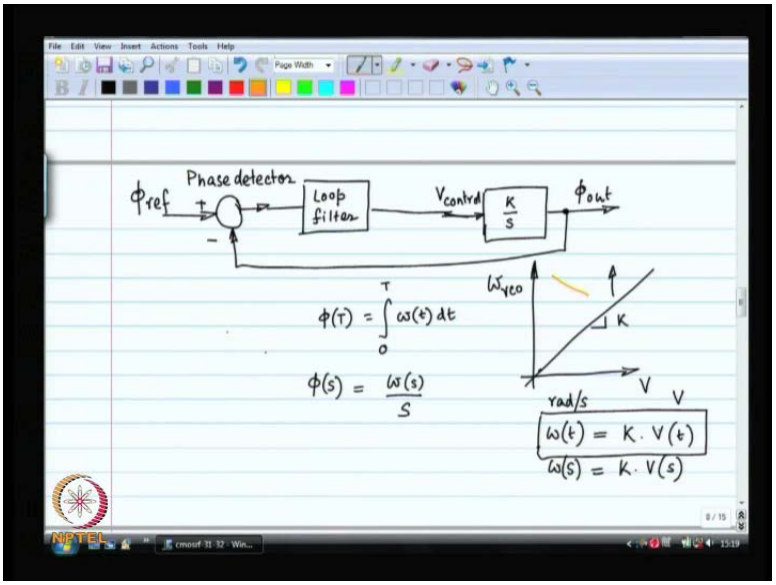

We have understood that these are basic building blocks, first of all we have understood the characteristic of the input phi ref is really a phase, the phase of a voltage. So, phi ref means to be tracked the phase of this voltage, the voltage is coming from a crystal oscillator the phases of ram, you want phi out to be tracking this ram. So, to do that you have to make a velocity control system that is number 1, number 2 the phase detector is something very special it is not a simple subtraction, inputs to the phase detector are really the voltages corresponding to phi ref and phi out.

You have to design a circuit whose output is the different of the phases of these 2 voltages. The third thing is the voltage controlled oscillator, the voltage controlled oscillator that is the plant for the control system, has characteristic of K by s something of that nature K by s.

So, here we assumed that I have got linear V c o this assumption need not to be true or analysis will work in spite of this assumption. So, without any loss of generality K could be negative. For example, the value K over here could be negative, without any loss of generality it could be offset from 0, and that brings us to I could I could easily create a curve that looks like this. So, without any loss of generality this kind of a structure is going to work us alright, next what we did in the previous lecture was we tried to build the first building block out here the phase detector.

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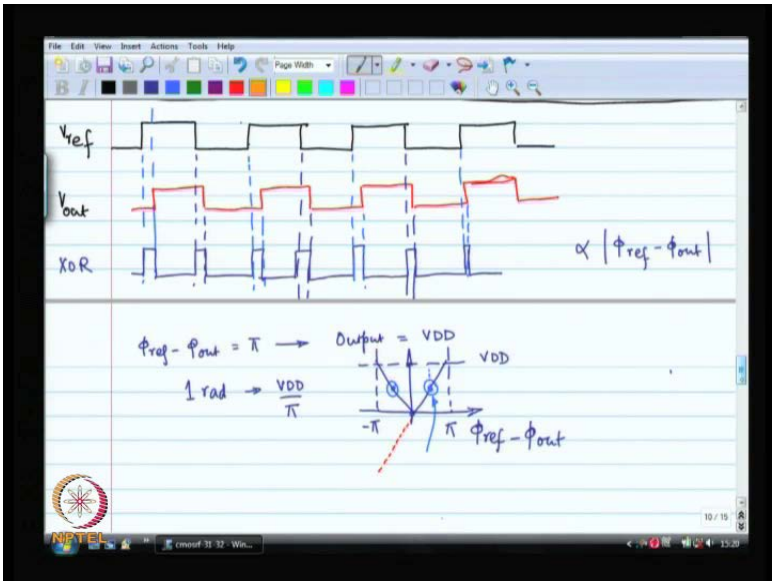

Now, this phase detector we figured out that the input signals are really digital signals. So, there is no reason why the phase detector should not be a digital circuit, our first experiment was with an XOR gate, we found out that the XOR gate kind of works, but it works at a bias point of pi by 2, or minus pi by 2 as the case may be, right.

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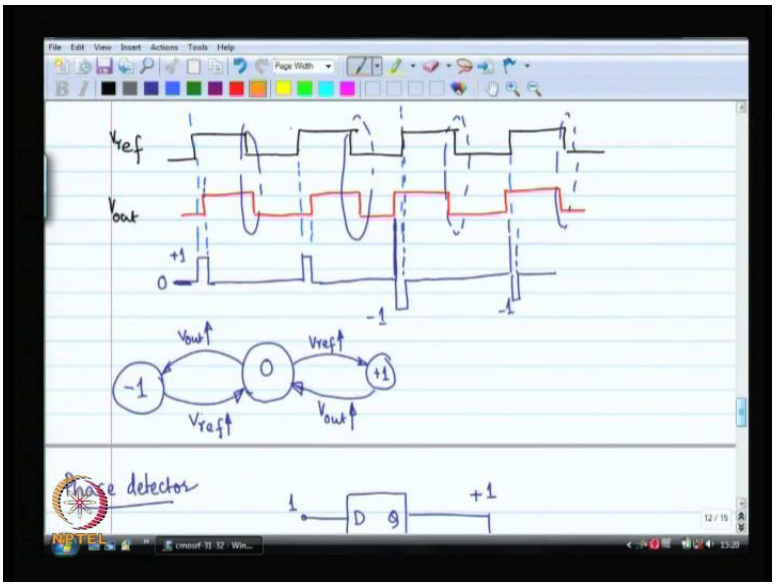

So, this is this was our first attempt, next attempt was more organize 1, and here we first made a state machine state machine diagram state diagram was a funny kind of state diagram with which responded to the edges of the 2 inputs, and then I after that I constructed the machine corresponding to that particular state state diagram it easy to understand this machine as well.

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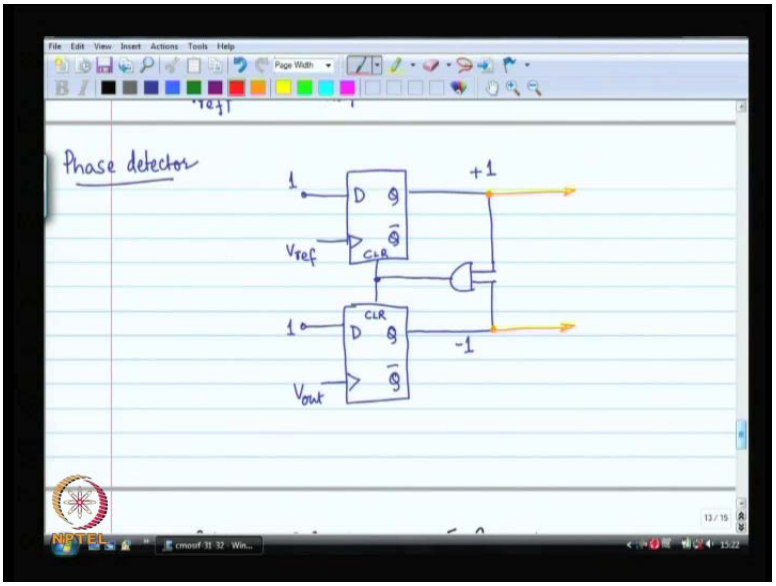

Now, the outputs of these machines are plus 1, and minus 1, plus 1 corresponds to the symbol plus 1, minus 1 corresponds to the symbol minus 1, and both of them are 0 the net result is zero.

If both of them happened to be 1 which should not be the case because as soon as both of these outputs are equal to 1 clear will be activator and both of them will be clear, right. So, this is our phase detector. So, the output is the digital representation of the sign of the phase whether it is positive or negative, or whether the phases are identically equal, the duration of these pals indicates how much the phase is off by.

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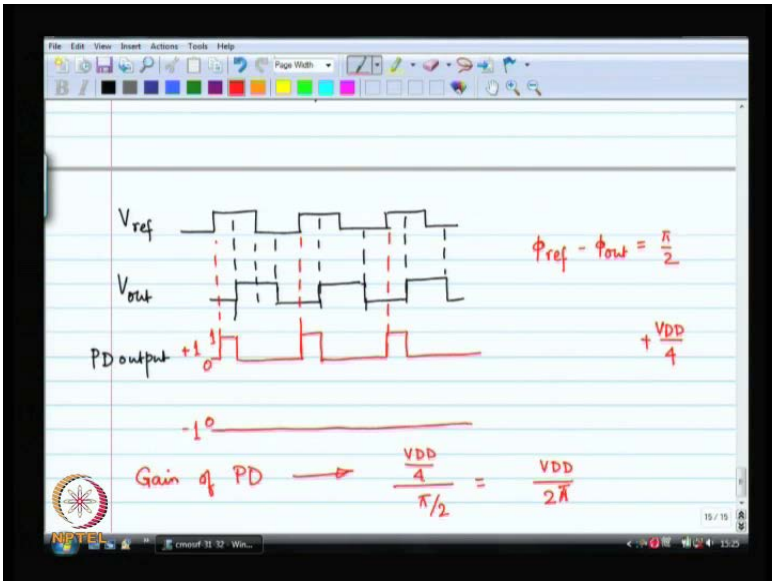

So, if my reference voltage is like this it is not really phi ref its V ref, and V out is let us say ninety degrees behind V ref, in that case the output of my PD phase detector that is my PD the output of the PD, there are 2 outputs of the P D.

This is plus 1 output, this is minus 1 output, right. Now the way the plus 1 works is when the edge of the reference clock comes immediately it goes to plus 1, and then it waits for the edge of the V out, then it goes back to 0, and when the is what about the minus 1 output the minus 1 output is always 0.

So, if my phase difference phi ref minus phi out is ninety degrees ninety degrees is pi by 2, then the phi PD output is plus 1 for 1 fourth of the time, which means that the PD output the average PD output is VDD by four. If I had phi out leading phi ref then it

would be minus 1 one fourth of the time. So, the PD output could be minus VDD by 4, fine. So the gain of the PD so for pi by 2 phase my output is VDD by 4. Therefore, the gain is VDD by 2 pi, alright. So, this is what I have got as the gain of the pe/phase detector.

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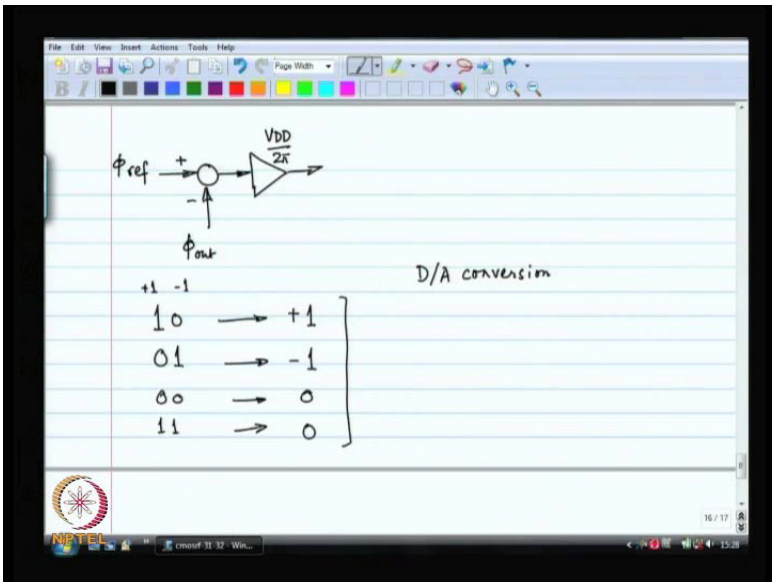

So, the model for the phase detector is something that looks like this, but we are not done as yet. Next thing you have to understand is that the output of the phase detector is a digital code, right it could be 1 0, which means the output is plus, it could be a 0 1 which means the output is minus 1, it could be a 0 0 which means the output is 0, and it will also be 1 1 for a very short duration, if you notice over here for a very short duration both the outputs are 1, as soon as both the outputs are 1 the AND gate output becomes equal to 1, and the clear is activated. So this delay the delay of the AND gate and the delay of the clear operation taking affect.

That total delay for that duration 1 1 will also be true, and 1 1 really means a 0 as far as we are concerned plus 1 minus 1 equal to 0 right.

So, what we have got to do over here is some kind of digital to analog conversion, crude digital and analogue conversion that we need to do, we also have to do some sort of averaging in the process.

so the correct output of the phase detector is the average value of the plus 1 signal, minus the average value of the minus 1 signal, that is the correct output of the phase detector, over a given period, right.

So, over a given period over a given period I want to add so plus 1 over here corresponds let us instead of plus 1 and minus 1 let us call them up and down, it is a this is my this is going to be nomenclature.

So, up corresponds to a plus 1, and down corresponds to minus 1. Now, what we have to do is we have to covert this up and the down signal into an analog value, why do we have to convert it into in an analog value, because we need to use the output of this phase detector to eventually drive the voltage control oscillator which is an analog, this is an analog signal, right.

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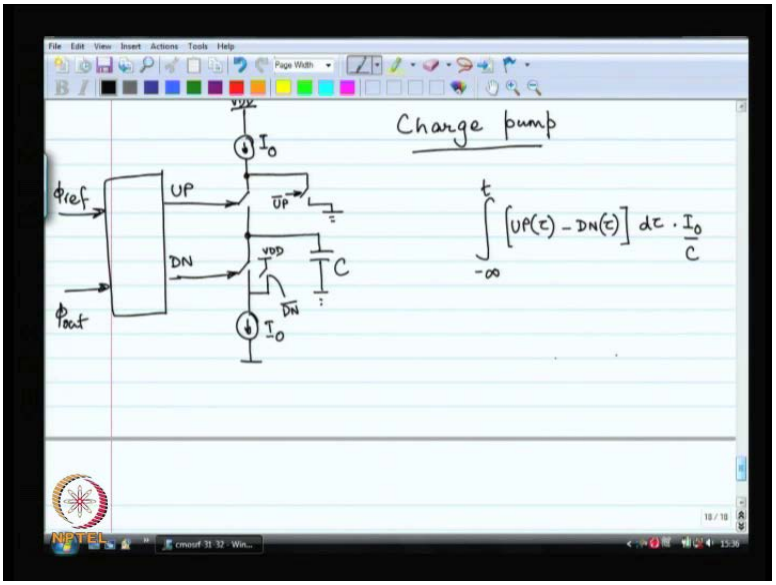

So, how do you do digital to analog conversion fast, digital to analog conversion you can do something like current steering this is a typical current steering back, very typical current steering back, or actually you we even not waste that current you can push it to another resistor and you will get differential output, fine. This is a fast current steering back we can use something like this, right.

And the output is an analog version of the sign of the phase difference between phi out and phi ref, phi ref and phi out, agreed. Now, what I am not showing over here I am not

yet done over here is the fact that I am not interested in the instantaneous value of up minus down, and interested in the average over a period of up minus down, over 1 period what is up minus down. So, instead of the resistor over there easiest fix is to put a capacitor. So, as long as up is high the capacitor charges, and when down is high the capacitor discharges.

You get up minus down, if up and down are high at the same time and the current just passes through does not charge the capacitor at all or discharge is the capacitor, right. So, this is the basic charge pump. Now, there are lot of problems over here we will come to the 1 by1, but the understanding is clear right what I have got is unfortunately the integral of the instantaneous up. So, consider up and down as either plus 1 or minus 1 plus 1 or 0, right. So, this is what I have got, ok.

It is not the average at all, 1 by this 1 by the total time during which I have done this job is going to be the average value, this is not the average value, is it the average value, no. So, this is what I have got at the output of the charge pump.

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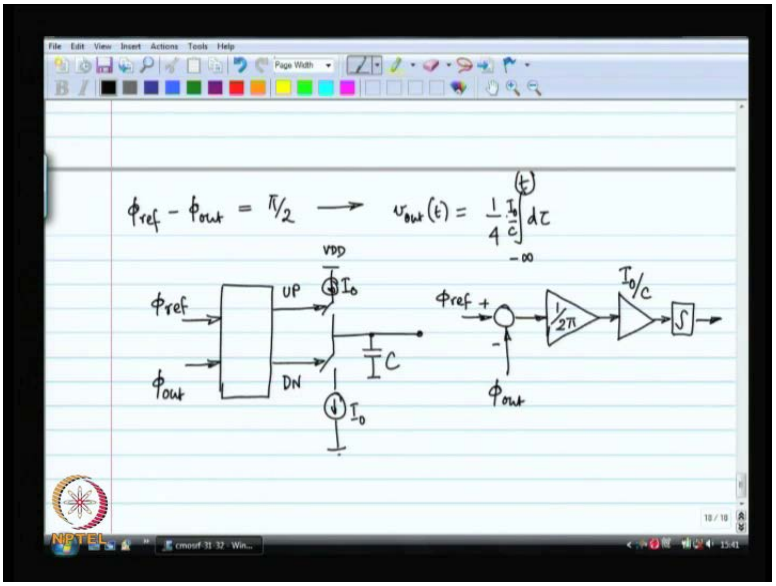

Now, if the phase difference between phi ref and phi out is ninety degrees just like before then up minus down will be 1, for 1 fourth of the time, right. So that means, that this result is going to be I naught by c 1 fourth of that integral minus infinity to the current time, is this alright, is this alright with everyone. So, what I have got essentially is this I

have got phi ref and I have got phi out and I have made a digital circuit I have got 2 signals up and down.

And with these 2 signals I am trying to figure out whether I should charge capacitor or discharge capacitor with certain amount of current, right. So this entire block can be modeled this entire block can be modeled as. So if the phase difference is pi by 2 then it is 1 fourth I naught by c.

If the phase difference is 1 radian its 1 by 2 pi times I naught by c. So, this is the model for the entire thing, it is an approximate model it works only when the time for which you integrate is much larger than the size of the period, right that is the only.

So, here this this t has got to be much much larger many many periods have to be covered right then only the average can be taken out of the integral, otherwise this is what you have forget to do, this is the truth this is an approximation that works only when the size of the integral, the time duration over which you are doing the integral is much larger than the period or rather than the yeah the period of each clock cycle, alright, so, this is the model that we have.

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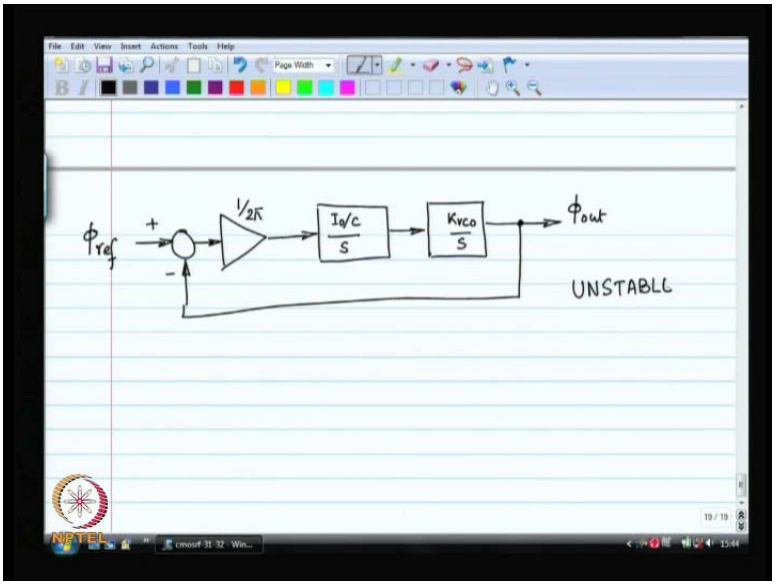

Now, if we plug this in to our system, if we plug it in our system as is without any further modification, then unfortunately our system is going to oscillate because there are

just 2 integrators with some gain, you agree or not agree. You got 1 by a squared in the denominator of the loop kin.

So, if you have 1 by a squared in the denominator of the loop kin and its negative in sign then in the overall denominated/denominator you are going to have 1 plus some constant times a squared, which means you are going to get poles on the j omega axis in the system is going to oscillate, it never going to stabilize, right. We want to make a stable system, so this is not going to clapping finally, do it just this is not enough. So, if I just make a charge pump and connect the output of this to my V c o is not going to work. Why not because I have got 2 integrators and as a result, my system is unstable. So, what we do now if you have done your, job that is your job was to go back open your control theory book and read about velocity control, how it is done.

There are several techniques, 1 of the techniques which is quite popular is to add a 0 into the system. So, the point is then I don't want to just put 2 integrators over there what if I had my current.

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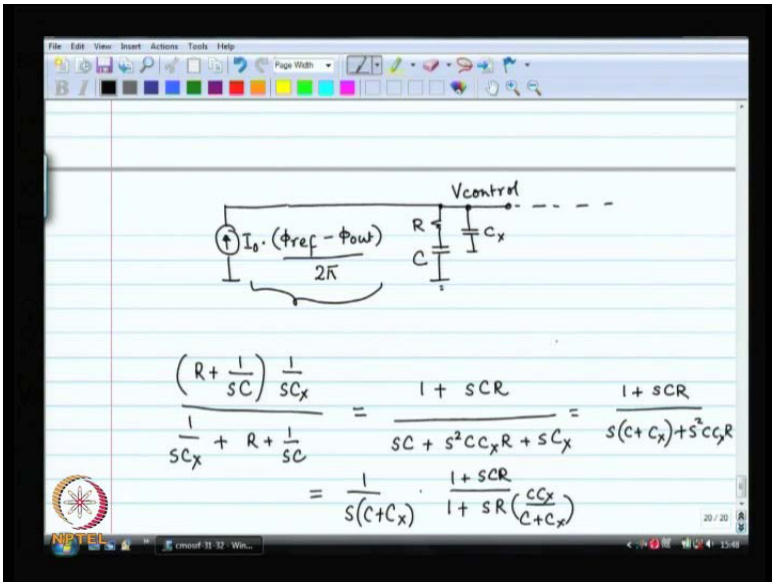

Let us say this is this is my average current what if instead of pumping it into a capacitor I pump it into a resistor capacitor and capacitor. Let us call this c 1, let us call this c 2, let us call this R or let us say this is C and this is C x.

So this is the model for the current coming out of the phase detector or the dac the current staring dac that is the current coming out of the current staring dac on and average that is what it is, and let me push that current in to this kind of system, and we will take this output to the V c o.

So, first of all what is this impedance that have created R in series with c insant with c x what does this look like. So, R plus 1 by s C is whole thing is insant with C x . So, this is the impedance I have neatly divided it up into poles and zeros for you, the impedance has a pole at zero is got a 0 at minus 1 by R c and it is got another pole at minus 1 by R times C series with C x, ok.

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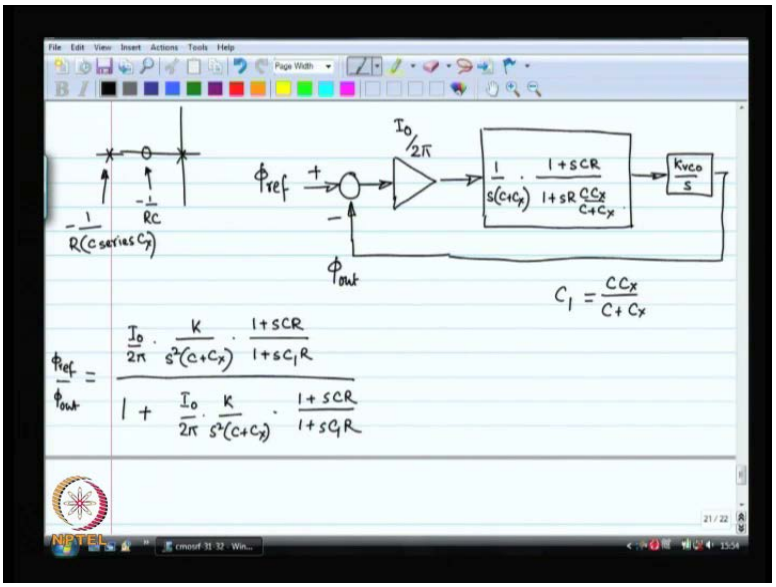

So, C in series with C x is smaller its smaller value than either of C and C x is definitely smaller than the C. So, you have got a pole at 0 at the origin then you got a 0 at 1 minus R c and then you've got a pole at minus 1 by R c in series with C x, right. So, this is what I have got as my loop filter. So this is called loop filter and, if you now do your analysis.

Instead of 1 by 2 pi I am going to write it as I 0 by 2 pi, then pole at the origin 1 more pole and 1 more 0, and this entire thing is going to control my plant; my plant is some constant divided by s, that is generating the phi out phi out. Now, if you do your analysis first of all let us check for stability it is going to be stable, but let us see let just work it out.

So, the open loop gain is I naught by 2 pi times 1 by or rather K, I am going to call it K not K V c o times squared C plus C x times 1 plus S C by 1 plus let us call this C in parallel C in series with C x let us call it something else.

Let's call it C s or let us call it C 1; C 1 is much smaller than c that is a lonely thing over here. So, this is my open loop gain. So this is a final expression, now of course, this will require simplification it is very difficult to handle these numbers.

So, I naught times K times 1 plus S C R that is what I would like to keep in the numerator and in the denominator I am going to keep I naught times K times 1 plus S C R plus 2 pi time S squared C plus C x times 1 plus S C 1 R, and further you would like to divide numerator and denominator by I naught times K.

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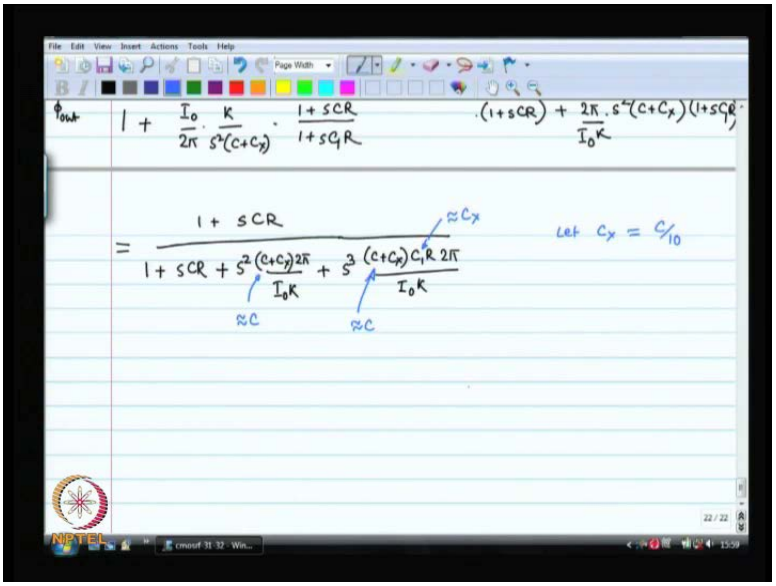

In which case this is what you're going to end up with little more simplification will oh actually its pretty need it is not bad at all its quite need in fact. So this is your system your close loop transfer function still not clear, if the system is stable at all or not, right ,and to prove stability what you need to do is some sort of uh an estimation of where exactly the poles are you could do that or you could start with this.

Could start with this polynomial this expression and do a routh hurwitz criterion remember Routh Hurwitz criterion, yeah, you work with the open loop gain, and you see

whether when you put the open loop transfer function in a close loop, your system is going to be stable or not, that is the routh hurwiz criterion.

So you could that as well or you could work with this final polynomial, and find out where the roots of the denominator are whether they are on the right half plain or on the left hand plain. Now, what you have to do over here is you have to understand that C 1 is small, smaller than C x and C, and c plus c x is of course, larger than C and C x, if I say that let us C x is let us say C by 10 if I choose C x to be something like C by 10, then C plus C x is going to be approximately equal to C, and C 1 is going to be approximately equal to C x; C x is much smaller than C alright, and you can show that under such conditions this kind of system is going to be stable this is not going to be too much of problem with this.

Look, you just have to find out where the roots are, and if you have nubs your nubs are C, C x, and R, and you have to make sure that C, C x, and R are such that their roots of this polynomial lie on the left hand plain you're done. So, that's all (( )), ok.

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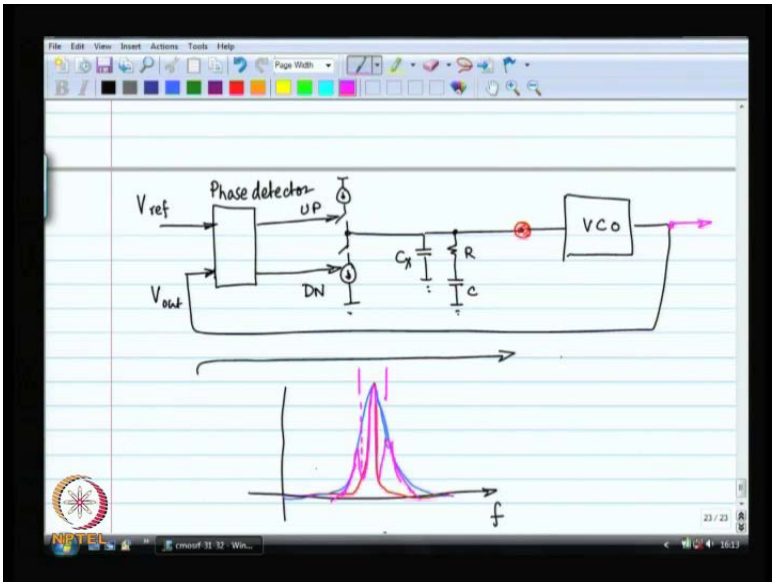

So that is p l l architecture I am I am going to make a phase detector using my beautiful digital circuit. The phase detector takes its input as 2 voltages, but for yeah sure it is going to generate up or down, now up or down also has significance; up means that the V ref is running fast, V ref is running fast, I need to increase I need to make the plant run faster, So I need to speed up the plant; down means that V out is running too fast I need

to slow down right that's why the terminology is also up and down in the books you will see up and down not plus 1 and minus 1, but really these 2 signals are digital codes for plus 1 and minus 1 together they make digital a digital code, right.

And then we have got the charge pump the simple charge pump is no good, we have to make a more sophisticated loop filter than simple capacitor, typically C is going to be much larger than C x; C x is about to tenth the thumb rule keeps C x about tenth or fifth of C, R and C together will determine the loop bandwidth.

This filter this is a filter this filter has a bandwidth, look at our expression this filter have a bandwidth it have a pole at d c it has a pole at 0, ok, and that pole is given by C plus C x, 1 by S, C plus C x, right. The total capacitance in conjunction with R is going to define the bandwidth of my loop. So, where was I. So, if I plot the response for this a kind of system I am going to get infinite gain at d c, right, and then I am going to get a 0 at minus 1 by R c what does that mean as far as we are concerned.

So, if I do the bored a plot is falling at 20 d V per decade then it is going to level off at minus 1 by R c and then again it is going to start falling off at minus 1 by R C 1. So this is called the loop bandwidth, why because at that frequency I will get 3 d V less than this value as the impedance that is my loop bandwidth that is the all important loop bandwidth.

Now this loop bandwidth what should its value b can the loop bandwidth b as high as the oscillation frequency, if the loop bandwidth as high as the oscillation frequency then it is like this V ref and V out are changing at the oscillation frequency those changes will go right through this entire loop, ok.

Think of think of this entire thing as filter, V ref and V out are changing at the oscillation frequency do you want this particular node to be changing, no this particular node is going to the voltage control oscillator, this is the control voltage it should be a fixed voltage because if this voltage is changing then the frequency of the V c o will also be changing you do not want to that you you do not want to this voltage changing at all, right.

So the idea is that this loop bandwidth has got to be much lesser than the oscillation frequency by itself how much lesser, it turns out that if it is not atleast 10 times lesser

then the system has not going to have the dynamics that we describe here. In fact, what's going to happen is that this approximation that we made is no longer going to be valid we made one approximation over here the fact that the output of the loop filter is a time average that approximation is no longer going to be a valid approximation.

If the loop bandwidth is larger than something like a tenth of the frequency of the oscillation if the loop bandwidth is as larger as tenth of the frequency of the oscillation then; that means, that minus twenty d V is the rejection at the frequency of the oscillation which means that if your whatever the amplitude of oscillation 1 tenth of that is going to come through come right through, it is a curiostic argument unfortunately this cannot be conformed in this theory you need to read a couple of papers there are some excellent references, which actual given the notes for the particular lecture.

There are some excellent references you can study the references, and this particular claim the 1 tenth number where it is come from it is really more of thumb rule it works if you go beyond this if you make loops that have larger bandwidth, loop filters that have larger bandwidth then unfortunately this approximation that we made over here is no longer valid.

Once the approximation made is no longer valid, then you have to work out the dynamics of this phase locked loop with greater thought, with greater. Basically the problem is at some point you have to do a conversion between discrete time and continuous time systems, right. and the complexities of that are going to be much much greater.

So it is going to go beyond classroom teaching. So this approximation works when the loop dynamics when the loop bandwidth is less than the tenth of the oscillation frequency, alright. Now, why would you want the loop to have large bandwidth, why why do you want loop to have the large bandwidth, is there any reason? is it to have 1 hundredth the loop bandwidth to be 100 of the oscillation frequency does it matter.

It does not matter if the V c o is good, but remember the V c o that you are made kin, one of the reasons, why you are making the voltage controlled oscillator is I am sorry one of the reasons why you are making this phase locked loop is to track the phase of the reference, you know that the reference is coming from a crystal oscillator; a crystal oscillator has far superior phase noise performance than the oscillator that you have built

on chip, right. That is the reason why you are making this phase locked loop. So you want to track the reference phase, now if you make a large bandwidth for your tracking then overall a large bandwidth the output of your oscillator will look like the output of the crystal, the reference.

So suppose this is a spectrum of V ref, and suppose if you just run your V c o as is then this is your spectrum, I am sorry probably it is not as bad as this. Let us say this is what it is have exaggerated a lot of over here, and now suppose your loop bandwidth is this much then that means, that the output the final output V out will have characteristics that look like the reference within that loop bandwidth, and beyond that loop bandwidth it will look like a free running V c o. So, within the loop bandwidth it is going to look like this the final output.

Outside the loop bandwidth it is going to look like here free running V c o, which has horrible phase noise, that is the reason why you want this loop bandwidth to be large want this loop bandwidth to be as larger possible, because of this on the other hand the loop bandwidth cannot be cannot increase forever; The loop bandwidth can be at most something like a tenth clapping of the oscillator frequency.

Now, that means when you build your phase locked loop you would like it is loop bandwidth to be exactly equal to tenth of the oscillation frequency, because otherwise you lose in terms of performance, right. So with this understanding we are going to proceed in the next class. So, we have kind of try to build of phase locked loop I do not exactly know if you completely understand what is going on over here, or not, but we are going to see more of this in the following classes.

Thank you.