CMOS RF Integrated Circuits
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Module - 10
Oscillators
Lecture - 30
Other Oscillator Topologies

Hello and welcome to CMOS RF integrated circuits today we are going to continue from where we left of in previous class we discussed in detail phase noise properties rather we just did a noise analysis a noise it is. So, happens that that noise is called phase noise because you know if you're expecting a square wave there's noise in the amplitude you can cut out the noise in the amplitude very easily. So, all that remains is the phase noise. So, that is why I am calling it that we did a phase noise analysis we did not really do a phase noise analysis as such.

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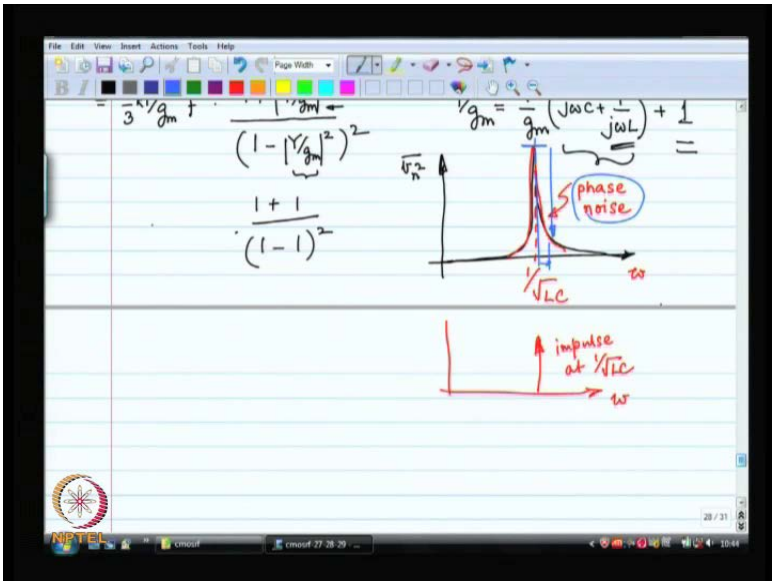

What we did was a general noise analysis and I showed you that instead of getting an impulse in the spectrum you get an impulse with a scat around it and that scat is because of phase noise. So, how its quantified. So, this is what I have and how its quantified is a you say that with respect to carrier at an offset frequency from the carrier of. So, much at. So, much offset frequency I have got. So, many d b is less of noise. So, it is called. So, many d b c d b with the respect with the carrier at an offset frequency of. So, much

from the center frequency from the carrier frequency. So, that is how we quantify the phase noise in an oscillator all right. So, today we are going to talk about other oscillator topologies. So, far we have just stuck to the 1 it is a very popular oscillator topology as such that is why we did a very detail analysis of it

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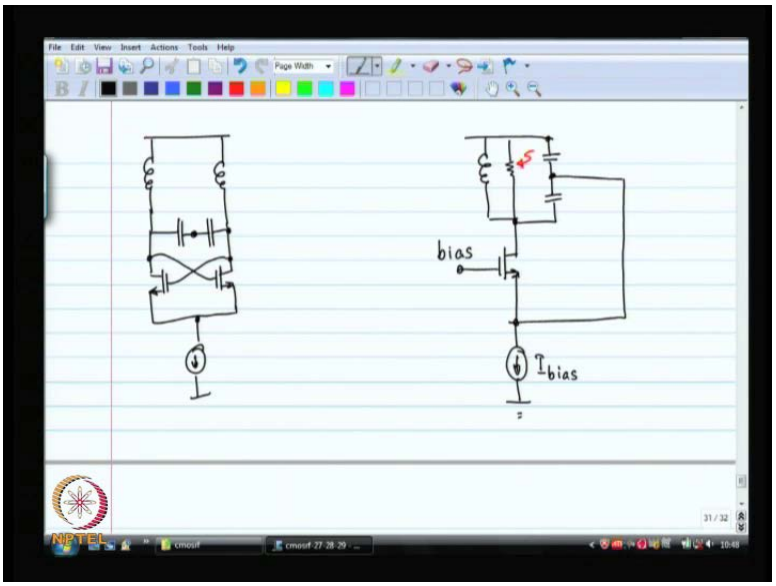

So, this is what we have done. So, far. So, this is a negative resistance based oscillator. So, you have got a tank[-in] I have negative resistor to compensate for the tank loss basically the loss is in the inductor. So, to compensate for that i've built a negative resistor and when the negative resistance when the negative conductance is more than the positive conductance of the tank then oscillation win and my poles go into the right half plane of the right half side of the s plane which means that I get oscillations.

So, this is what we have done. So, far oscillators typically every time a person create an oscillator they add a name to it. So, there is colpitt oscillator there is hartley oscillator there's clapp oscillators. So, on and. So, forth lot of different there's a pairs oscillator lot of oscillator topologies are available most popular decides the 1 that we have studied is the colpitt oscillator that is also a lot of these topologies are based on the tank circuit

So, let us briefly take a look at the colpitts oscillator. So, we need a tank tank means wherever you have an inductor inductor is really not a pure inductor. So, I am going to modeled the inductor as an inductor enchant with resistance now note that this resistor is not intentional this is something that has come as a result of placing the inductor over

there a d current losses series core wire losses etcetera copper losses right and usually this is my tank circuit.

Now, what I am going to do is instead of having this I am going to break this capacitor into 2 capacitors in series all right and I am going to take out the voltage from the and feed it back. So, it is more or less the topology of the colpitt oscillator. So, I have got a tank and I take out a fraction of the voltage on the capacitor feed it back to the source. Now, what does this do. So, as far as the small signal voltage is concerned. So, in the small signal sense let us let me redraw my circuit in the small signal sense in the small signal sense this bias current is an open circuit the bias voltage is ground potential

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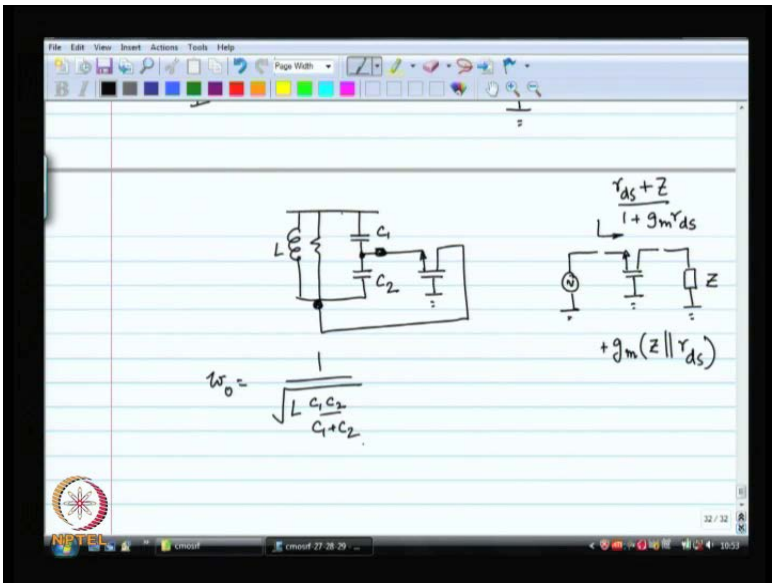

So, if I redraw my circuit this is what I have got right or in other words if I try to draw it little more I reorganize my drawing it is going to look like this right this is the common gate structure it is the common gate structure remember put your input here and you see here output there common gate structure the gain there is the gain of the common gate amplifier the common gate amplifier has a gain of positive g m times let us not call this R let us call this z this is the gain the common gate amplifier and the input resistance of the common gate amplifier is going to be what is going to be R d s plus z divided by 1 plus g m R d s z is small enough let say z is 0 then the input resistance input impedance is the approximation equal to 1 by g m if z is small all right.

So, that is what I have got. So, this is a feedback circuit there is. So, the voltage here I am sorry this this is sensing a voltage. So, the voltage here at this point is amplified by a factor the amplification in g m times z parallel R d s and its put over here now notice that the gain of the amplifier is positive which makes it positive feedbacks circuit right. So, this is your colpitt oscillator when the gain is positive when you have a positive feedback system a positive feedback system means that you've got some sort of negative resistance going on here right and that will make your system entire system oscillate or it will place the poles under right of side the s plane. So, that is basically the idea over here you can do a detail analysis it is not terribly difficult to do a detail analysis of the colpitt oscillator and you can show the frequency it will oscillate at is basically the tank frequency.

So, this is my L and this c is series combination of c 1 and c two. So, that is the typical frequency of oscillation that is the tank right L and its split out the capacitor into 2 pieces. So, that is why I am saying series combination of c 1 and c 2. So, the tank frequency oscillation is right and this is when the positive feedback is enough to precisely cancel the resistor that you have got the damping resistor that you have got all right. So, this is a colpitt oscillator.

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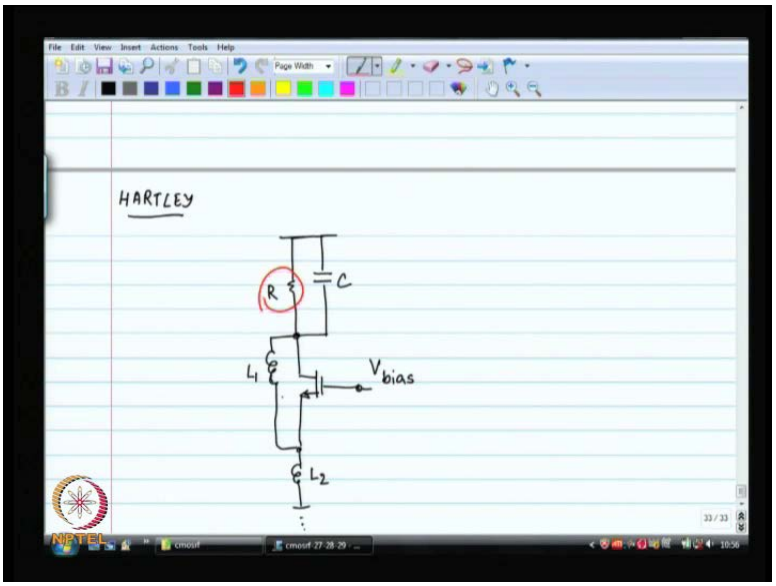

A hartley oscillator is very similar very very similar and instead of having a capacitive divider for the feedback we will have an inductor divider that is all right that is your

hartley oscillator. So, now I am not going to show the biasing over here it is not terribly easy to see what is going on with the biasing because I put a current source to bias over here all that current is going to go through this nothing is go through the mosfet. So, that is going to be a correct biasing strategy. So, i've got to put some sort of v g s over here typically; that means, that you could do potentially something like this right and once again this particular R is not something intentional this came as a result of problems with your circuit.

So, this is the hartley oscillator it is just a variation there are a couple of more such oscillators there's the pure oscillator clapp oscillator etcetera etcetera lot of different oscillator topologies exist in the books more or less they are all based on the same principle you sense the oscillation and you create a positive feedback and feed it back to create more oscillations this is basically the idea all of these are tuned oscillators and the outcome is typically hopefully a square wave that is the target. So, all of these kind of achieve that targeted you get a square wave ok

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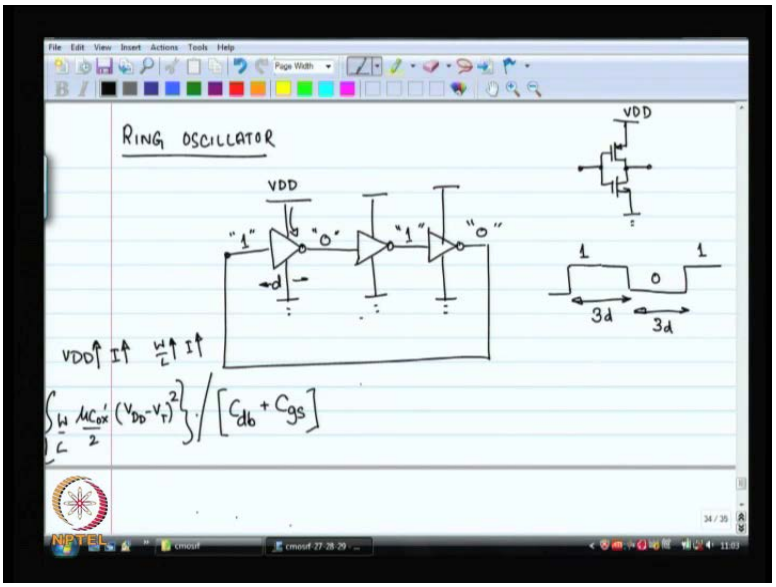

Now, another very popular oscillator is the ring oscillator it is a very popular oscillator specially in the digital world lot of ah clocks on c p u s are generated sometimes through ring oscillators. So, a ring oscillator is something very straightforward I can design a cmos inverter cmos inverter is something like this this is your cmos inverter. So, I can design a cmos inverter and I can put an odd number of these inverters in cascade odd

greater than 1 and feedback. So, this is a ring oscillator it is a 3 stages ring oscillators similarly you can make a five stage ring oscillators seven stage ring oscillator etcetera etcetera you can convert these inverters into differential inverters and you can you might as well do it differentially in which case you needn't have 3 stages, but that is secondary as far as we are concerned all right. So, this is basically the idea

So, let say that each gate has a delay of d each inverter has a delay of d where is this delay coming from this delay is coming from the amount of current that the inverter usage up and the load capacitance the load capacitance is the gate capacitance of the next stage. So, that is where this delay is coming from. So, it takes some time to current to charge up the output all right. So, that is basically where the delay is coming from let say each of these inverter has a delay of d then if this is a 1 after a delay of d this comes a zero after a delay of 2 d this becomes a 1 after a delay of 3 d this again becomes a zero which is the same net right.

So, if I if this particular wire is a 1 after a delay of 3 d it goes back to zero after another 3 d it will again become a one. So, the net period is six times d which means that the oscillation frequency is going to be 1 by six d. So, this is trivially simple to analyze if you can figure out what is d the value of d is you've done right what is going to be the value of d the load capacitance is the gate capacitance of the next stage which is basically c g s of the next stage it is also the drain to body capacitance of the of the inverter itself . So, it is something like this right. So, this is the load capacitance that each inverter sees each inverter sees the same load capacitance.

Now, if you think about it each inverter is seeing this load capacitance and the amount of current it is drawing from the power supply the amount of current is v g s v g s is v d d minus v t the whole squared something of this magnitude of course, this is when the device is on its not really correct the device is I am sorry this is when the device is in saturation the device is not going to be saturation most of the time it is going to be the linear region in which case you have to modify this equation and hence this current thing is not really correct.

But 2 first order you can see that if I increase v d d the current is going to increase. So, the current is proportional to not going to say proportional over here the current increases when I increase v d d also when w by L increases I increases c ox increases I increases

which basically means that I make the thickness if the oxide layer smaller then I will increase area larger I will no this is quite unitary mu the mobility I increase the mobility then also I will increase etcetera etcetera you can figure this out and so, that is the current this current has to charge a capacitor and that is what you have over there you get a delay right. So, this is the analysis from this prospective if we think of doing a small signal analysis let us think of lets conceive of a small signal analysis it is not really correct to do a small signal analysis because signals are large.

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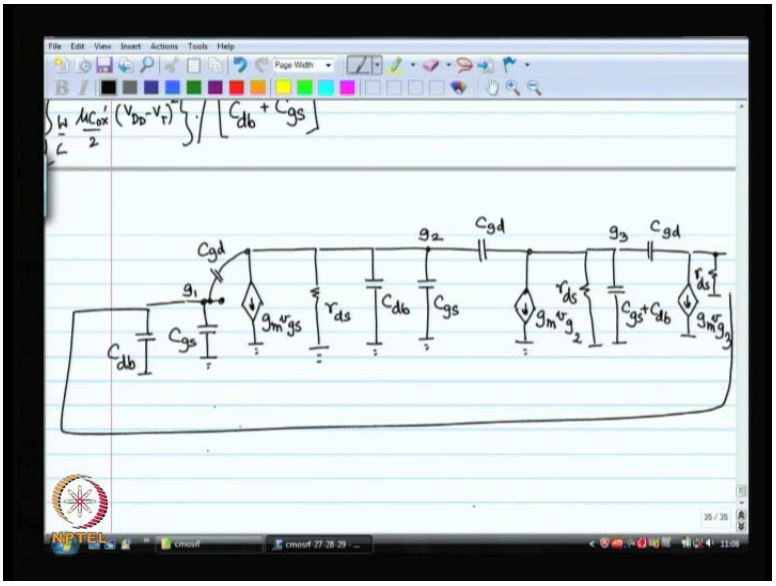

So, it cannot possible do a small signal analysis, but then again we did a same thing for earlier setups right where the signals were large we still did the small signal analysis and kind of got a feel for what is going on. So, let us do the same let us try to get a feel for what is going on each stage over here lets draw each stage is g m times v g s here g m is really the g m of the n mos plus g m of the p mos enchant with R d s R d s is really R d s of the n mos enchant with R d s of the p mos what about capacitors as far as capacitors are concerned.

I have got a gate to drain capacitance this gate to drain capacitance is really the sum of the gate to drain capacitance of the n mos on the p mos I have got a gate to source capacitance which is again the sum of the gate to source capacitance of the n mos on the p mos I have got a drain to body capacitance which is again the sum of the drain to body capacitance of the drain mos and the p mos source to body is relevant because source and

body at the same potential right. So, this is each stage and you would like to repeat these stages ((no audio 24:25 to 26:02)) all right. So, this is what you have got you got a complicated networks it is not really complicit that complicated

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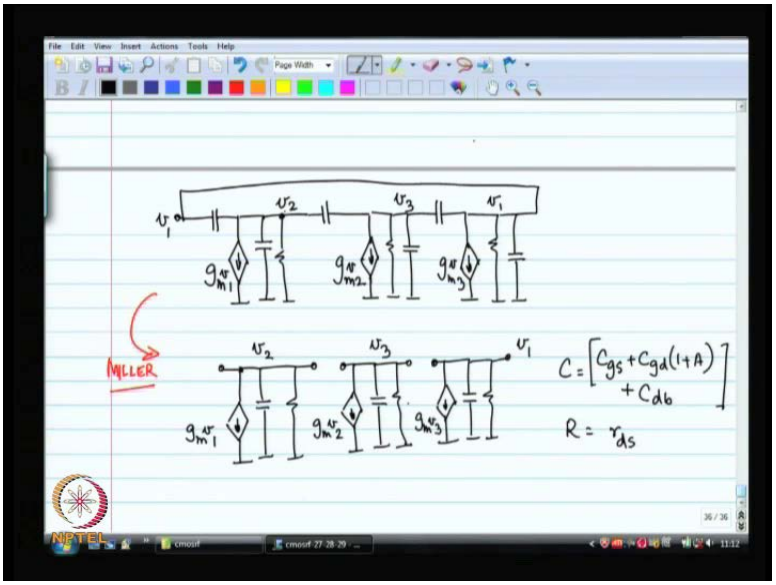

You can simplify this to this ((no audio 26:26 to 27:03)) right now these gate to drain capacitor pose some kind of problem because they are between 2 terminals and not respective to ground typically you can break this you can conceive of breaking this using miller's approximation and if I break the gate to drain capacitance using miller's approximation then it breaks up into a times where a is the gain of each stage a times c g d on 1 side and c g d on the other side.

So, each side seeing a c g d each node is seeing a times c g d each node is also seeing 1 times c g d. So, each node is seeing approximately 1 plus a times c g d right. So, you can simplify this using miller you can simplify this by just having 1 resistor and 1 capacitor at each node . So, what I have done is I have broken up the gate to drain capacitors each capacitor on each node is really c g s plus c g d times 1 plus a a g m times R d s. So, this is each capacitor that you have got.

Let say that this is a c and each resistor is R d s right let say we called it R all right. So, this is what I have got and of course, g m all of these different components are really the total between the n mos and the p mos taken together this analysis is for a small signal when both the devices are active at the any given bias point this is the analysis all right.

So, this is what I have each stage is therefore, going to to contribute a pole and there is going to be gain associated with each stage.

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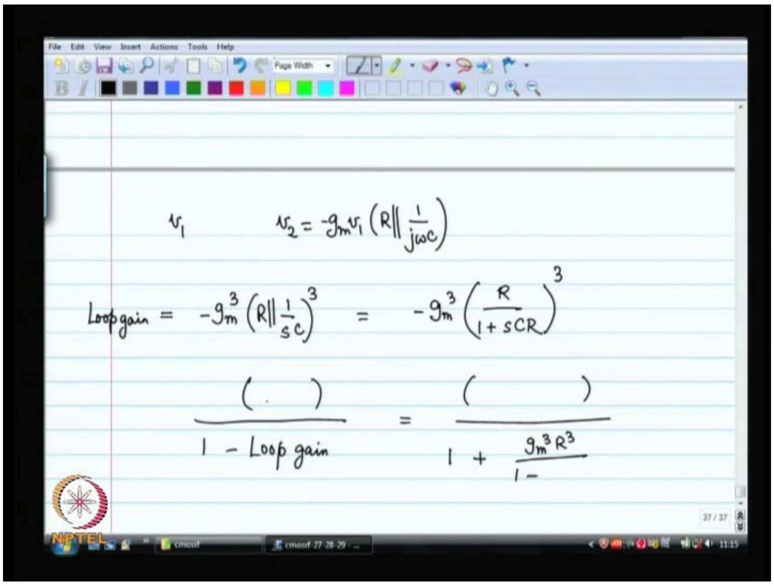

So, if if I have got v 1 then v 2 is equal to g m times v 1 this is the current times the impedance the impedance is really R parallel 1 by j omega c if I have got v 2 then v 3 is the same factor times v 2 and if I have got v 3 v 1 is the same factor times v one. So, the loop gain of the system is g m cubed times R parallel 1 by j omega c whole cubed this is the loop gain negative I am sorry there is minus sign that I have missed up all right. So, this is my loop gain and I think I would really like to convert this R parallel 1 by s c R parallel 1 by s c is R by s c by R plus 1 by s c which happens to be equal to R by 1 plus s c R ok.

Now, when you do your analysis whatever you want to find out some parameter right your expression is going to have 1 plus the loop gain I am sorry 1 minus the loop gain in the denominator. So, something you are trying to find out your denominator will have 1 minus loop gain now this loop gain is really g m cube by g m cubed times R cubed divided by 1 plus s c R the whole cubed right

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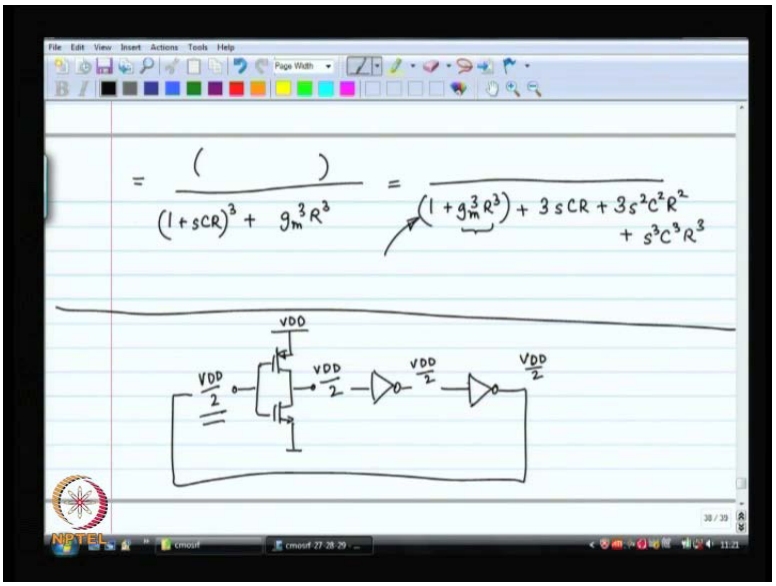

And really what this means is that you have got something times 1 plus s c R the whole cubed divided by 1 plus s c R the whole cubed plus g m cubed R cubed. So, your denominator contents this as its denominator polynomial now if this is the denominator polynomial then the poles are the roots of the denominator polynomial it is hard to find out the roots of this cubic equation its quite hard to find out the roots, but if you do your analysis you will find that pair of roots fall in the right half plane pair of conjugate roots will be there in the right half plane. So, that is basically the idea of this if if I had just 2 inverters in series with feedback then first of all I wouldn't be getting the negative sign I would be getting the positive sign here that is the problem ok.

So, it is not going to create negative feedback it will work as a latch it is going to create some positive feedback at d c it will work as latch all right. So, this is basically the analysis of the small signal model of [-a ring] of a ring oscillator now why I did this was to hint at the fact that suppose suppose there is a equilibrium suppose you have designed your inverter very carefully you've designed your inverter very carefully you have chosen width and length of p mos and n mos devices is very carefully such that if v d d by 2 is the input then v d d by 2 is the output precisely ok.

Now, I put 2 more such inverters the second inverter has an input v d d by two. So, its output is going to be v d d by 2 the third inverter has its input as v d d by one. So, its output is also going to be v d d by 2 and I feed it back where is the oscillation there is no

oscillation if you think of it this way, but wait this is the exact situation under which we did our pole zero etcetera analysis right this is the precise situation beautifully bias all the nodes are at v d d by 2.

Similarly, I use small signal models all the devices are active etcetera I use my small signal model and I see that this is going to be the denominator polynomial of the expression for any particular voltage or current now if that is the denominator polynomial then there are some roots on the right half plane which means that whatever that quantity is it is going to start growing exponentially and with sinusoidal voltages it is going to go exponentially and if its start growing exponentially then it is cut off balance. So, this v d d by 2 is no longer going to remain because something has changed perfectly balance something start moving away because of the poles being on the right half plane and as a result it is no longer going to be at perfect balance everywhere.

So, this is basically the idea this is why we did the pole zero analysis to prove that this thing is indeed going to oscillate did not really completed because I cannot find out the poles of a cubic the roots of a cubic by hand, but I give the way all right if g m times R is large g m times R is some number like twenty right. So, keep that note it its part of this discussion what about the phase noise as far as the phase noise is concerned we did ah similar small signal analysis for the tank circuit remember and if I do a phase noise analysis of this particular oscillator of the ring oscillator what you are going to find is this ((no audio 40:00 to 40:53)).

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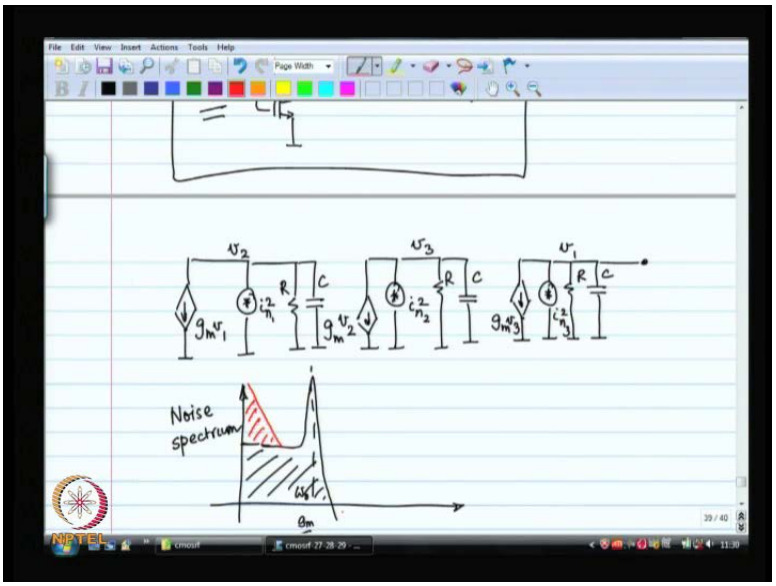

This is going to be my scenario and let say that I am going to take the output from here now the way we do this is we take each noise source at a time and then work it out each noise source we are going to take at a time and then find out the output because of each noise source and then add them up add the means square all of these noises together and that will be the means squared noise voltage the total means square noise voltage at the output that is how we are going to do our business all right.

Now, what you can see over here is that I n 1 squared is going to go through some sort of a low pass filter R c low pass filter to create v 2 that v 2 is further going to go through another R c low pass filter to create v 3 that v 3 is going to go through another R c low pass filter to create v 1 right that v 1 is of course, is being feedback now if this is the situation then what do you expect the noise voltage spectrum to look like at the output qualitatively if I have noise at the d c let say I n is a d c noise current.

So, that will create a v 2 that v 2 is going to create an amplified v 3 that v 3 is going to create an amplified v 1 right the net result is going to be that I am going to get some noise at d c of course, at the desired frequency of oscillation the noise is going to shoot up ((no audio 44:00 to 44:53)) at the frequency of oscillation the noise is going to shoot up, but what I want to suggest over here is that if you do a small signal analysis of the noise you are going to find out that there is going to be noise at d c it is a come sort of low pass filter with a cutoff frequency of 1 by R c.

So, noise will be there all over from d c to 1 by R c to a frequency 1 by R c or. So, so all of this is called phase noise now compare this to what you got before to compare this to what you got before we did a more detail analysis of course, right now I hardly did any analysis I just said qualitatively it looks like noise will be there at d c over here there is no noise at d c its clean at d c we saw that noise at d c is perfectly equal to zero this was my equation for the noise we proved that noise at d c was perfectly equal to zero that is because of the band pass nature of the L c circuit.

So, the L c circuit is a band pass circuit right L c filter it is a band pass filter. So, the band pass nature of the L c L c circuit allows noise through at 1 by squared root of L c it does not allow noise at any other frequency over here qualitatively if you look at it this is not an L c circuit this is an R c circuit that you are using R c circuit does not have band pass characteristics it has low pass characteristics.

So, noise will be allow right through from frequencies starting at d c now of course, if you take into account only thermal noise this is how the spectrum is going to look like if you take into account effects of flicker noise 1 by f noise then this is actually going to grow at d c this is also going to appear as phase noise. So, everything over here all the noise is phase noise its it cannot be possibly be amplitude noise the amplitude noise is a squared wave right.

So, this entire all the noise that you are seeing is really expressed at the output as phase noise or jitter uncertainty on the period of the oscillation. So, jitter and phase noise are basically the same thing you can mathematically correlated 1 to the other and you can see that for a ring oscillator you get a huge quantity of jitter because of 1 by f noise because of the very low pass characteristics of the oscillator whereas, as far as L c circuit is concerned 1 by f noise is of no concerned because at d c noise is completely filtered out. So, no frequency noise is filtered out 1 by f noise does modulate does get modulated because of the linearities, but that is a different mechanism altogether. So, you will see effects of 1 by f noise even in L c oscillators, but not to the extent that you see in ring oscillators ok.

So, we want times make a system for a cell phone accurate frequency is of great importance to us we want to compete with a atomic clocks we definitely do not want large quantities of jitters. So, this is the ring oscillator systematically because of the very

nature of the circuit the low pass nature of the circuit allows noise at low frequencies. So, that is bad we do not want to make ring oscillators when we want to design for a cell phone where we want to compete with atomic clocks crystal oscillators quartz crystals right.

So, this leads us to the design choice of L c oscillators almost invariably you will see L oscillators at the heart of oscillators in circuits for radios circuits for cell phones. So, inductor is a costly component, but it got to be used right. So, with this as our background we have studied phase noise mechanism for the generic n c tank oscillator with negative resistor it is a very generic oscillator actually it is. So, easy to make and. So, easy to design and understand that is it very popular there also exist the colpitt oscillator the hartley oscillator differences that both of these the other techniques the named oscillators use 1 device. So, that actually quite nice if you want times make these oscillators using discrete devices I do not have 2 devices to spare, but rather make with 1 device.

So, colpitt oscillator hartley oscillator these are older oscillators when devices were of great demand were of high price and all of these are popular oscillators topologies they all used some sort of feedbacks some sort of positive feedback mechanism at the chosen frequency of oscillation all right. So, with this we are going to move on to the next topic the next module rather ok.

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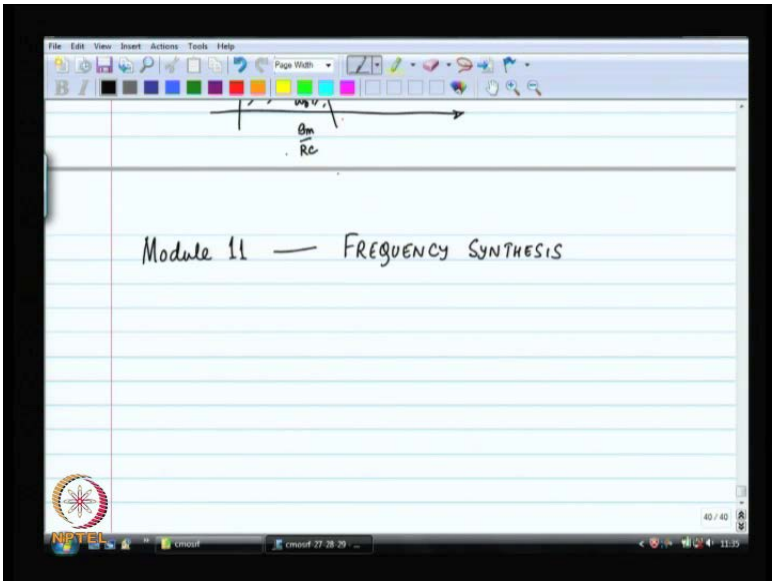

So, let me first motivate frequency synthesis for you in a radio system in a wireless system there are 2 things 1 is you need a pure frequency ok.

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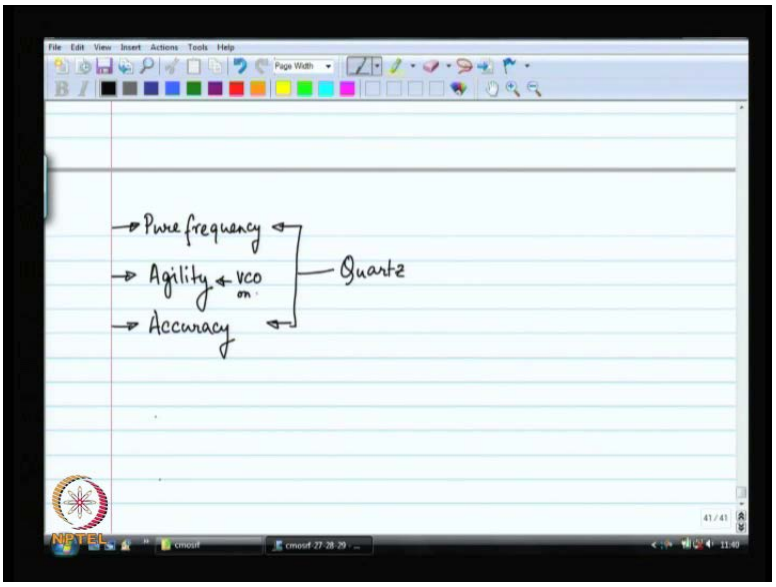

Jitter in the time period of the oscillation is bad phase noise is bad phase noise is the same as jitter you do not want to have any phase noise in your system that is number 1 number 2 you want to make an oscillator which when demander can move around. So, let us take an example you switch on your cell phone the oscillator tunes to a particular frequency which everyone knows is the pilot frequency where the base station sends its information I mean instruction initial instructions random max's channel right.

So, it oscillator will tune to the random max's channel first then the base station will instruct the cell phone to tune to a certain frequency immediately the oscillator will have to tune to that certain frequency for specific instruction then the base station will tell the cell phone that look you have to go to this particular frequency because a certain other user has switched on his cell phone in your neighborhood you do not want to interfere with him. So, immediately you switch channels ok

So, basically the idea is you keep on switching channels from time to time and you have to this at a very rapid rate I am going to call this agility your oscillator has to be agile it has to able to move around as rapidly as demanded by the base station the next thing is your oscillator has to be accurate what do I mean by accurate if the base station tells you go to the 1 gigahertz you have to go to the 1 gigahertz precisely you cannot go to the 1

gigahertz plus 2 hertz or you cannot go to the 1 gigahertz plus 1 kilohertz that is not acceptable.

So, this is a third thing. So, there are these 3 components you need a pure frequency, but of course, phase noise is no good you need to able to be agile and the third thing is you need to accurate when you talk about what is the precise frequency this you're oscillating at. Now, we all know that as far as a pure frequency is concerned if I try to build something on chip then the inductor will have loses lossy inductor low q the quality factor of inductor is like five maybe ten if you've done a very good job ten. So, as a result you'll have a lot of phase noise on the other hand a quartz crystal can give you a jitter of ten parts per million that is very very good in terms of phase noise it is a very clean frequency.

The next thing is as far as accuracy is concerned what crystal can be treated as a reference if the manufacturer of quartz crystal tells you this crystal oscillate at 26.001 megahertz it oscillates precisely at 26.001 megahertz it does not oscillate at 26.001 megahertz plus 5 hertz ok. So, as far as a pure frequency and accuracy go quartz crystals are unbeatable as far as agility goes your voltage control oscillator is definitely agile it is just that you have no idea of what that precise frequency is also you have very little control over the phase noise in your system.

So, we need a mechanism to combine the quartz crystal which is external with the v c o on chip and get the best of the both worlds we want agility, but at the same times we want a pure frequency we want very low phase noise and we want great accuracy we cannot tolerate random frequency ok. So, with this in the background we are going to stop and we will continue with this discussion on frequency synthesis in the next class.

Thank you.