CMOS RF Integrated Circuits
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Module - 08
Low Noise Amplifiers Design
Lecture - 24
LNA Noise Other Possible Topologies

Welcome to CMOS RF integrated circuits today's the twenty fourth lecture and we were part of we were working on low noise amplifier design and we had come up with a certain topology for a low noise amplifier and today we are going to evaluate what is the noise performance of that particular amplifier and following that we are going to investigate other possible LNA topologies and we will see how far we go with this. So, the topology of the LNA that we came up with look something like this where am I basically this this was my final LNA topology alright input is coming in to a mosfet into the gate of the mosfet there is source degeneration through inductor that gets amplified that gets converted into a current.

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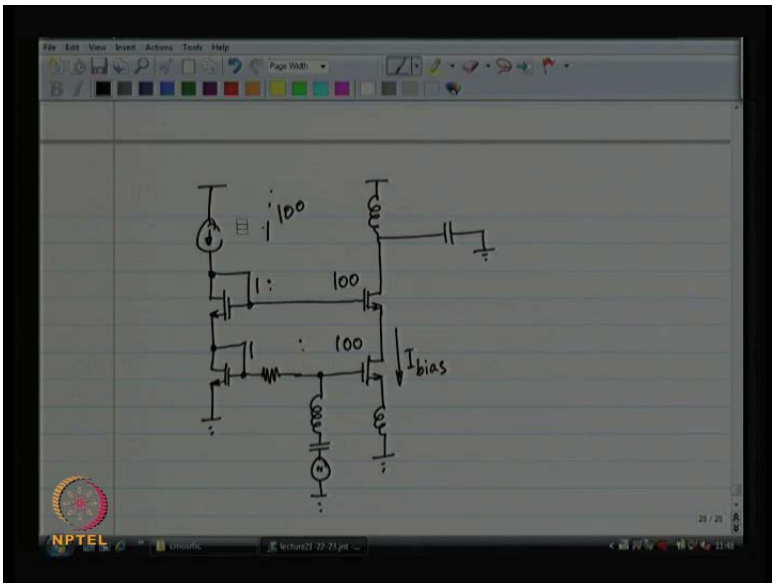

The current is converted into a voltage through a cascade mosfet which is placed further on and the load is also inductive this is done for matching purposes output matching purposes because eventually most probably what you are trying to drive as a capacitor is

a capacitive load. so this was my basic topology that I started from there are going to be other issues to look at like biasing etcetera.

You can take it back to your unlock circuits classes to understand biasing issues a crude way of biasing would probably look like something like this this is current source a current mirror we want to certain current. So, this would be the way to generate a current mirror and over here I have my inductive load and probably my final load capacitor all that is fine this the top device is my second device, but my first device if I place an inductor on the source side nothing changes as far as d c goes because an inductor is a shot as far as d c is concerned.

And I also want to place an inductor and connected to my signal source if I do that if I connected directly to the signal source like I have done over here then what is going to happen is that the signal source is d c voltage which is 0 volts is going to propagate. And as a result the gate of the mosfet will be bias start 0 volts which is not something that you want. So, you put a blocking capacitor over here alright now in this case also the small signal voltage over here because of because of this current source the small signal voltage at the gate of the current mirror is 0 volts which means that the small signal voltage at the gate of the mosfet is the 0 volts.

So, it is not going to work. So, you have got put an a c block over here. So, an a c block could be a large resistor it could be another inductor you try to avoid inductors. So, you put a large resistor over there. So, typically this could a very crude way of biasing things if you want to do things better you would optimize further and converts this current mirror into better topologies etcetera etcetera. Uh this is also wasteful in terms of current. So, if you plan to have I bias flowing over here and you by and you put a 1 is to 1 current mirror then you are consuming 2 x the current right. So, probably you want I bias a fraction of I bias let us say I bias by 100 and you make these w by L in the ratio of 1 is to 100 ok

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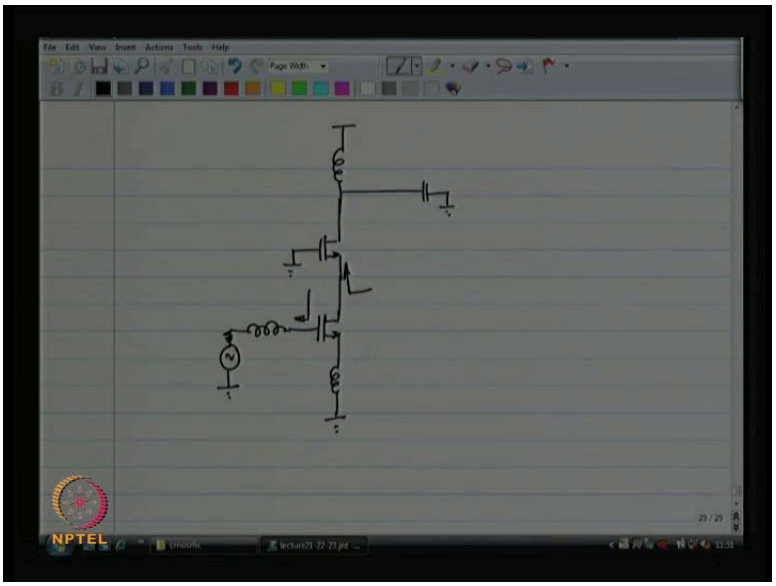

So, this also could be done anyway this is an aside this biasing is just an aside and this is not really the meet of our discussion what I want to discuss today is the noise performance of this particular LNA. And as far as noise is concerned what I have got in my design is something like this this is my load this is my cascade device over here this is small signal ground as far as the cascade is concerned and as far as my input device is concerned I have got an inductor connected to my input voltage source directly I have thrown out that capacitor because hopefully it is large capacitor which is going to make it short.

I have also thrown out the biasing resistance bias t that I had up front because hopefully that resistance is. So, large that looks like open circuit if you prefer to put in a inductor there that is also fine. So, these are called chokes RF chokes right. Inductor that you put for biasing purposes which looks like open circuits at RF frequencies that is RF choke. So, this is my circuit as far as my LNA is concerned my signal is concerned this is what it sees now when we are going to talk about noise we have to realize that my signal has resistance associated with it that is number 1 number 2 is looking in here looking from the gate the model for my because it is a matching network the model for my voltage source is something else.

The model for my voltage source is the appropriate input resistance and the appropriate voltage right. So, this is what we have done in the previous class and then I said that we

need to model the noise of each of these mosfet. So, to model the noise I said let us make a first approximation to make our life easy. To make our life easy let us say approximate the input impedance of the cascaded mosfet looking into the source of the cascaded mosfet.

Let us say that you see 0 hopes its very reasonable approximation its very reasonable and. So, what I am basically saying is that let us say that the second mosfet is irrelevant it usually as irrelevant let us say that. All I have got is this alright and the mosfet produces its own noise let us focus on the channel noise of the mosfet. So, the channel noise of the mosfet I have got a mean squared noise current over here which is an addition to the channel current alright.

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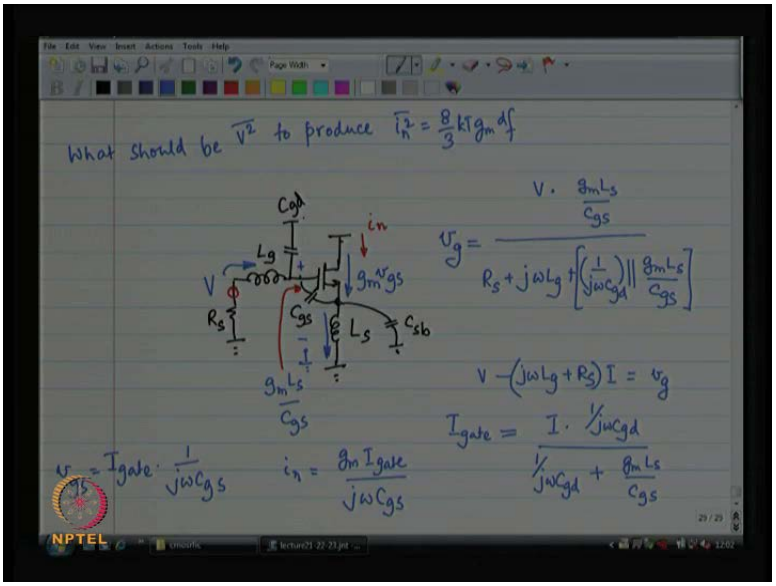

So, this is what we have got and in additional to this we should not forget that the mosfet has its own parasitic capacitances there is c g d there is c g s there is c source to bulk c drain to bulk is irrelevant because both sides of both drain on the body both are ground. So, drain to bulk capacitance is not relevant as long as you have good ground. So, this is what we have got. Next step I am going to delete my input voltage source completely its only a resistor now this particular resistor will also have its own noise voltage that is the source noise as far as the noise figure is concerned it is the total noise divided by the source noise that is the noise figure. So, this also has its own noise voltage alright this is

what we have got and now we have to find out what is the channel noise when I refer it back to the input voltage source.

What is the channel noise when I refer it back to R s. So, this is basically the question in other words what should be a voltage that I need to apply over here. So, what is V what should V x x such that the current over here is I N what should V x V such that the current over there is I N if I know V x then V x squared will give me I N squared that mean squared also correspond ok.

So, what should be V x such that I get. So, much channel current this is the basic question and to answer that what you have to do let us forget about this channel noise right now mosfet is noiseless let us say the mosfet is noiseless I apply a voltage V x what should this voltage V x V such that the current in the channel of the mosfet is I N this is the basic question right.

And let us work it out. So, if I have V x then V x is going to undergo a voltage division input impedance looking in . So, looking in from this point I see some input impedance that input impedance is really given by this quantity remember right of which we found that it is dominated by g M time L s by c g s. There in any 2 are not of a terribly great consequence over here. So, the input impedance looking in over here is g M times L s by c g s it is a resistance that you look in over there now you're basically going to do a voltage division and that will tell you what is the voltage over here with respect to ground, but that is not enough for me it is not enough to know what is the voltage with respect to ground I want to know what is V g s because when I know V g s g M times V g s is I N right.

Now, the next thing to understand is that this current plus g M times V g s is this current alright and given this 2 we can figure out what should be my V g s what is my V g s. So, so the first step as the first step I can figure out what is the voltage at the gate the voltage at the gate is given by V times g M L s by c g s divided by R s plus j omega L g plus let us ignore c g d for convenience let us say c g d is not relevant at all no c g d is necessary for matching ok.

So, 1 by j omega c g d instant with g M L s by c g s this is the gate voltage alright now once you know the gate voltage what I am saying is that it is very easy to find out what is the current going into the gate the current going into the gate is V x yeah V minus this is

the current going into the gate of course, c g d is also part of the show over here. So, I get it is very easy to compute I from this.

I get is really I times j omega 1 by j omega c g d divided by 1 by j omega c g d plus g M L s by c g s now this I gate this is the gate current this gate current is dropping across c g s alright it has no other place to go it goes across c g s and it creates a voltage across it. So, I gate times 1 by j omega c g s is equal to V g s and I N is V g s times g M alright. So, now, you know I N in terms of v.

Do you know I N in terms of V yes because I know V g in terms of V if I know V g in terms of V then I know I in terms of V if I know I in terms of V then I know I gate in terms of V if I know I gate in terms of V then I know I N in terms of V once I know I in terms of V then I can figure out what should be the V to produce I N equal to I what should be V squared. To produce I N squared equal to eight by 3 k t g M d f alright this is the story now you know what should be V squared that V squared plus the source noise is the total noise divided by the source noise is the noise figure.

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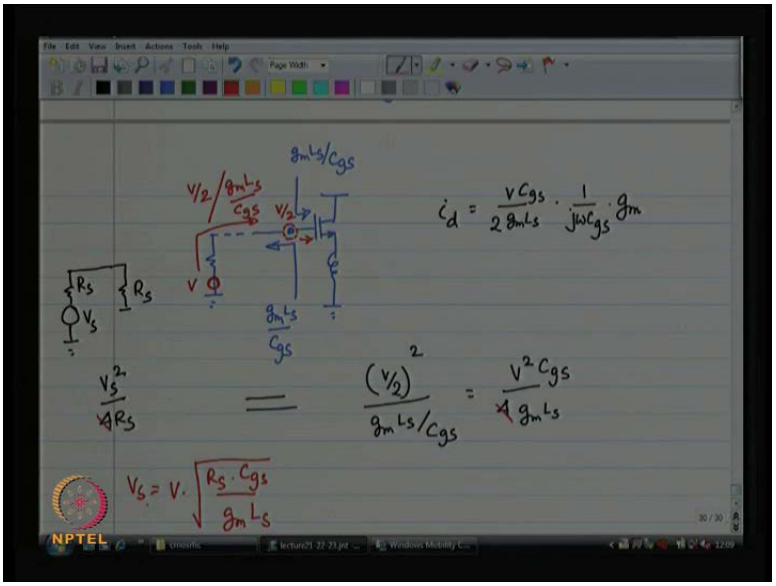

So, there are lot of computations involved I am not going to attempt a closed form solution for this because you know it is too difficult too many manipulation going on and the closed form solution may or may not give you any real insight into what is going on over here what is what you need to understand is as follows. A certain gate to source voltage is needed to have a certain current now I have a matching network I have made a

matching network to make sure that looking back from the gate I see what I see looking into the gate.

So, looking into the gate looking into the gate this is without c g d etcetera I c g M L s by c g s a resistance remember this is what we did my matching network is such that looking back from here I also will see the same resistance g M L s by c g s otherwise I haven't got any matching. So, all of those gate inductance c g d all of those and R s all of those can be lumped into 1 big resistor with have an equivalent of all that is 1 big resistor which is called g M L s times L s by c g s.

So, this is the first thing that you need to observe. So, if that is the case if I am going to apply a voltage over here I will get half of the voltage over here right what is my current going to be my current is going to be V by 2 divided by g M L s by c g s all of these current is going into the gate which means that these it is dropping across c g s which means that the gate to source voltage.

This is the gate current this gate current is going to drop across c g s. So, V g s is. So, much which means that the drain current is. So, much alright this beautiful I have simplified all of these nonsense into this simple understanding ok. With the help of the matching network of course, now you are working at the match frequency you are not doing arbitrary frequencies over here omega was death we did not know what is the value of omega omega could be anything this is a very general analysis you do not have to bother about the general analysis.

Let's work at the particular frequency where the LNA is going to operate the LNA is going to operate at the match frequency and at the match frequency this is what is going to happen the drain current is going to be. So, much times with have an equivalent of the voltage alright. What is the corresponding voltage that you had to apply when to transfer the same amount of power over R s. So, to transfer to have the same amount of power as far as the source is concerned your network looks like this you have done good job with matching.

This is what your network looks like as far as the source is concerned right. So, V s and R s they are delivering how much power to R s to your load to the LNA V s is delivering V s squared by 4 R s this is the power deliver to the LNA here the power that I am getting is V by 2 squared by g M L s by c g s. Now, these 2 have got to be equal. So,

really this 4 is going to cancel with this 4 and R s is going to come on the top. So, V s squared by V squared equal to R s times c g s by g M times L s right. So, V s is equal to V times square root of all of above. Alright it is like this to get a certain current I N to get a certain current I N squared I need to apply a certain voltage for this thevenin equivalent network.

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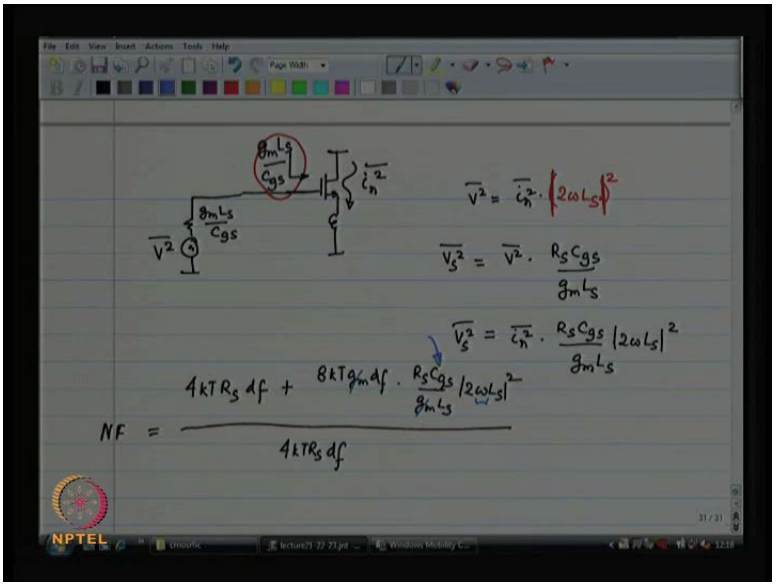

Let me try to give you the jest of this. So, to get a certain I N squared I need to apply a noise voltage to this thevenin equivalent of the source side network with the matching right and that relationship that relationship is really very straight forward alright now of course, there is j over here and when you squared the j its going to give you a negative sign, but do not be bother by it really has to be the absolute magnitude squared of this which means j will go away.

So this is step 1 step 2 is to understand that to get a certain V over there your source has to have a certain source voltage and that relationship is given over here this is the equivalent input referred noise voltage that you need it to apply in the first place. So, as far as your noise figure is concerned your noise figure will be 4 k t R s d f plus I N squared is eight k t g M d f times R s c g s by g M L s times 2 omega L s whole squared divided by 4 k t R s d f.

So, this is the approximate noise figure rather noise factor then twenty log of this field give you the noise figure. So, this is the simplified understanding of what is going on the

simplified of what is going on is to operate at the match frequency at the match frequency if you look at the source looking back from the gate of the mosfet you're just going to see the same resistance that you are seeing when you are looking into the gate of the mosfet right.

Of course I have done some approximations here what is the pro[ximation]- big approximation that have done the big approximation that I have done over here is that this is g M L s by c g s it is not exactly that it is g M L s by c g s plus a few more components plus g omega L s plus 1 by g omega c g s right.

In which case looking back into the source should give you the conjugate of that and appropriately you have to modify your mathematics, but it is definitely easier to solve your understating to to proceed with your understanding this way than to solve the general equation and get lost in the mathematics. So, this is what we attempted first we tried to solve the general equation we got really lost in the mathematics in spite of making several approximations right here also I made the same approximation which is not really precisely correct right.

And then I made several I took several steps I did not solve any of these steps whereas, over here I solved all the steps I made that 1 same approximation solved all the steps and I came up with the concrete result. Now, this gives you a better picture of what is going on and what needs to be done as far as your LNA is concerned to get a certain noise figure etcetera. So, to get a certain noise figure you have to optimize certain parameters at a given frequency.

Alright. So, what what what can you work with over here g M is going to cancel away. So, you cannot really work with g M L s is not something that you want to work with L s depends on the matching properties right L s is not something that you want to really be working on as far as your device is concerned. Uh omega is given omega is the frequency of operation of the LNA the frequency at which you did your matching c g s c g s changes when you change the device geometry. So, c g s is definitely something that you are going to work with the larger the c g s the more noise figure you are noise factor you are going to get ok.

So, no surprise larger the capacitance is going to be the more noise factor you are going to experience. So, this kind of completes our understanding of the tuned low noise

amplifier. So, this is how we normal design a tuned low noise amplifier. So, you start up with a certain current that has been given to you and given the certain amount of current you figure out what should be no given the certain amount of current.

You first figure out what should be the trans conductance what should be c g s of your device once you have figured out what is g M what is c g s then the rest is easy rest is just treating and finding out the w by L ratio and [clapping] anything else and of course, you have to design the matching network at the input and the matching network at the output side.

So, what could be other topologies for the LNA this particular low noise amplifier that we design it is a very sharply turned low noise amplifier its tuned at the frequency of interest we have also done special optimizations you put source degeneration inductor it help as far as noise is concerned because now the resistor is artificially created and not directly created by a physical resistance. So, over there other options that you might have are to use the inductance available within the channel of a Mosfet.

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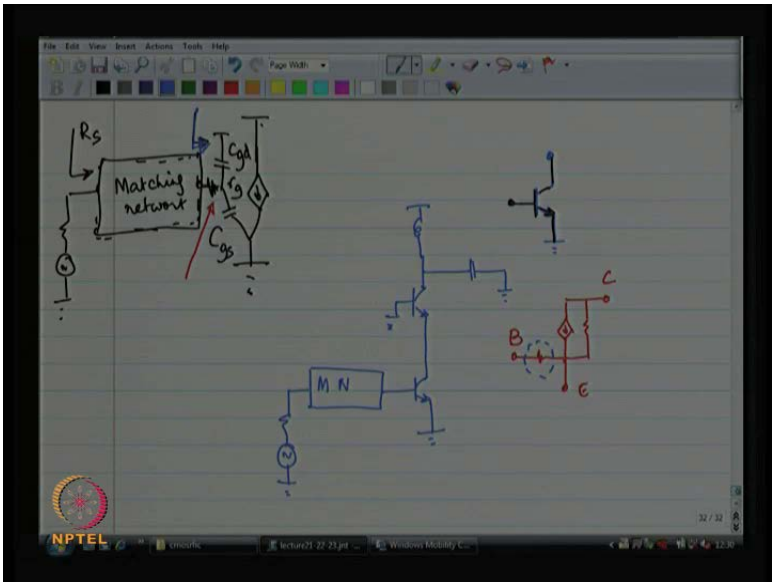

So, the mosfet model has a couple of things besides the capacitors the mosfet model has a great resistance it also has a channel inductance. So, your could use this particular property of the mosfet model to your advantage and try to develop a matching network at on the input side. So, your plan is to develop a matching network over here. So, that when look in to the matching network you want to see R s. So, what I am saying is

considered the following consider that the mosfet is not just g M and c g s. So, the normal mosfet model is this let us say that drain is at ground small signal ground.

Or you are driving a small impedance with the mosfet. So, the drain is almost mosfet ground potential. So, this is the normal mosfet model R d s is irrelevant over here because both sides of R d s are at ground small signal ground see source to body is relevant because source is at ground body is at ground drain to body capacitance also irrelevant because drain is at ground body is at ground.

So, this is the regular mosfet now as far as the regular mosfet is concerned the input impedance is a pure capacitor and if you have a pure capacitor as an input impedance then you cannot match it to a resistance through any matching network. It is not possible to design such a matching network you are always going to see a capacitor or you are going to see something which is lossless there has no power power consumption in this right. So, the idea is do not think of the mosfet as just a capacitor some wise to think of the mosfet as just a capacitor it isn't.

First of all there is gate resistance what is gate resistance it is not the resistance between gate and channel it is the poly of the gate it is a distributed resistor you are applying contact somewhere and charge has to spread all over the gate and it has go through a resistance to do. So, effectively you see an R c times construct. So, you get an effective lumped resistance value that is the gate resistance it usually a very small resistance who knows what its value is going to be could be a couple of homes first of all there is some gate resistance the next thing is. So, as soon as you have got gate resistance your input is no longer a plain capacitor they input is a resistor there is a resistive portion to the input portion of the. So, design your gate is actually consuming your power ok.

So, you can design your matching network for this particular purpose that is you could make sure that the power consume by the gate is equal to the maximum power that can be delivered by the particular source. If you do. So, what kind of noise figure do you expect if you do such a thing if you just make a matching network to match the impedance that you see over here to R s source resistance what kind of noise figure do you expect to are come up with finally, you expect to come up with a noise figure of your own 3 d V or half noise factor of half why.

Because the gate resistance is going to generate noise the amount of noise that the gate resistance is going to generate referred back to the source is going to be equal to the source noise because you have matched the source noise resistance to the gate resistance.

That particular ratio has already been used to design the matching network. So, it is just going to a step up by the same factor and as a result the gate noise will be equal to the source noise. So, you will get a noise factor of half right away. So, you do not even have to think about the channel. Now, you think about the channel which is going to add further noise referred back to the gate. So, the minimum noise figure that you can get out of this kind of circuit is 3 d V it is no good not particularly exciting alright you can use by polar junction devices ok.

I would not confuse you, but if you do use by a polar junction device then you do see a base resistance, but that base resistance is not a resistor this gate resistance is a resistor it is coming because of the presence of a resistive gate distributed resistance on the gate poly is there right. Poly silicon it is coming because of that its generate noise it consumes power the gate is going to consume power and generate noise as far as the bipolar junction device is concerned you will see the model for the bipolar junction device transistor could be something like this.

Ok, but this resistor that you see over here is not a real resistor it is not really a resistance that is physically present over there and as a result you do not expect to generate noise like a real resistor does. So, there is suckle difference between these 2 although the models look very similar is not much different as far as the model is concerned right.

There is no difference as far as the model is concerned probably there is an extra there is capacitor less in the b g t, but as far as the understanding is concerned both are very different in the b j t k there is no physical resistor over there that is going to generate noise in the mosfet case there is a physical resistance on the gate of the mosfet. It is going to generate noise it is called the gate noise right. So, these are other possibilities. So, basically you can just have thinking about the b j t you could just conceive of designing something which looks like this right all you need is a matching network to match the resistance that you see looking in to the base emitter to the source resistance.

And then the same computations follow after that you can have a cascaded device after that you can have cascaded device after that you can have anything else for further

amplification you need an output matching network would have something like this right your this base emitter the resistance between the base emitter is not a physical resistance it is not go to generate its noise alright. So, you can make no noise amplifiers with b j t as well mosfets are always prefer because if you are going to make c mos RFIC then you should be you should stick to mosfet and if you stick to mosfet then.

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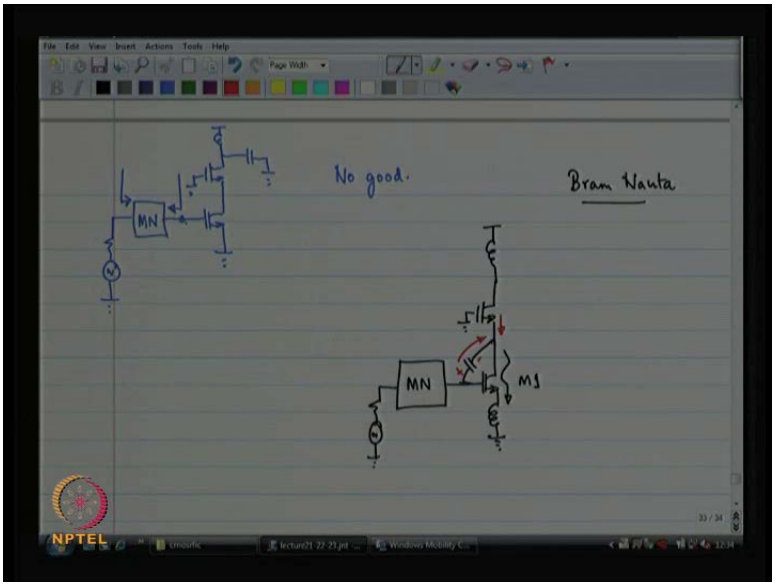

This particular circuit is no good that is all I am trying to say over here this circuit over here is not going to have any benefit right why because looking in here you see in R s looking in here you see the gate resistance plus complex conjugate of plus the conjugate of the rest of the stuff and the gate resistance is a noisy. So, the same noise is transferred to the source. So, you get about the 3 d V of noise figure right away. So, this is no good other variations include.

I can attribute uh some of these variations to gentleman named bram nauta you can look up several papers written by this particular gentleman all about low noise amplifiers noise cancellation techniques. So, he can actually cancel the noise produce by this channel by coupling it in the reverse phase into the next stage. Its it is not very easy to understand what is being done over there, but . So, the noise current the noise current by this device M 1 is responsible for a certain amount of input referred noise. So, the noise current by M 1 is responsible for a certain amount of input referred noise.

Part of this noise current is going to come is going to decide to come from the capacitor part of it is of course, going to be sourced through the second mosfet because it is a low impedance noise, but if I artificially place a second capacitor over there I can have some noise coming out in the other direction from the other direction.

Now, if I do. So, then that can create a voltage that is proportional to the current with the ninety degrees face shaped right the voltage will lack behind the current the current will lead the voltage alright. So, this kind of strategy is used routinely these are noise cancellation techniques you can look up several papers written by this particular gentleman and further study these techniques alright. So, I am more or less going to summarize over here.

So, what we did today was basically to understand the noise of this 1 mosfet we did not even look at the second mosfet the noise contribution of the second mosfet is going to be divide down by the gain of the first stage and hopefully that noise is not going to become significant. So, the significant noise contributor over here is the first mosfet second mosfet also have its own noise contribution, but its effect is going to become much lesser. So, that is why we kind of did not even look at the second noise source why what is going to happen the second noise source

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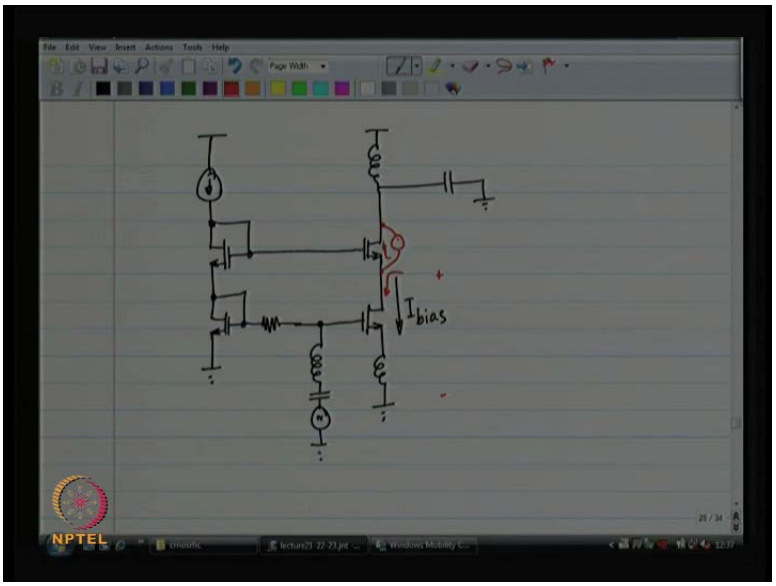

This is a noise source right where is the current going to go the current can go into this or it can go back through this the impedance looking downwards is very high the

impedance looking upwards is very low such going to prefer to go into the low impedance load. So, as a result the voltage is develops backwards is very little. So, if you develop a low voltage across this then it is reasonable to expect that particular noise source to contribute very little noise then you refer back to the input. So, this is what I am trying to say and tha[t]- this is why we did not even bother analyzing the second source alright. So, the first noise source first mosfet you could choose to think of it as a noise source do the proper analysis and get lost in all of the calculations.

The second approach is to have an understanding that act the matching frequency the inductor and the in the inductor the inductors together are such that the source resistance matches with what you see looking into the gate and with that approach we computed a noise speaker. So, this is where we are going to stop there are several other LNA topologies I refer you to paper written by this gentleman for a very good designs very competitive designs over broad band etcetera. So, please take a look at paper written by the gentleman it is not going to be possible to cover everything in this particular course.

Thank you.