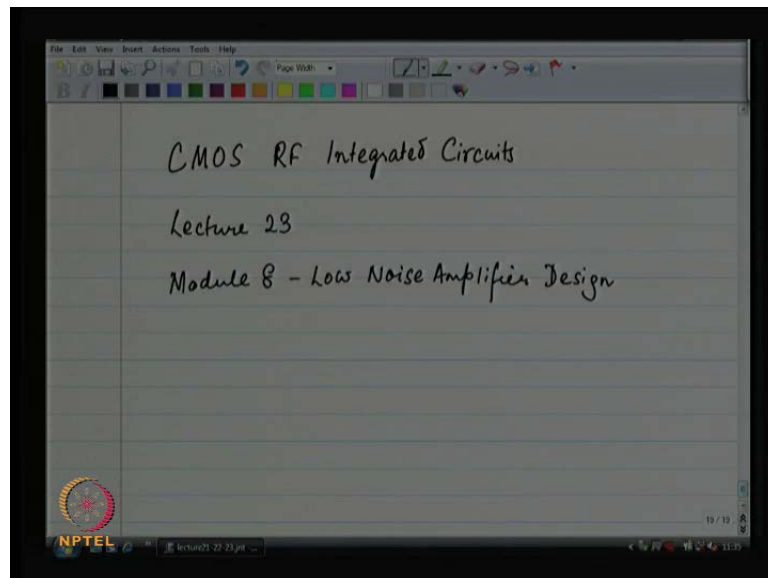


CMOS RF Integrated Circuits
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Module - 08
Low Noise Amplifiers Design
Lecture - 23
Motivation, First Cut Design (Contd.)

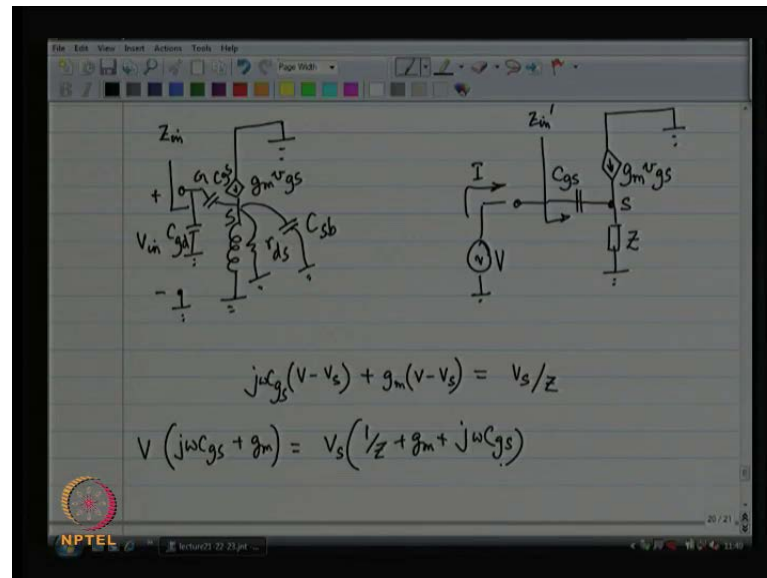
Welcome back to CMOS RF integrated circuits today's the 23 lecture we are going to talk about continue our work on the low noise amplifier design.

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So, what we were working on in the last class we had I was proposing the following I was proposing that

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Let's have the mosfet and the problem with the mosfet is that the input is capacitive, but what we are going to do is we are going to degenerate the source of the mosfet and what I propose to show is that the g_m of this particular cell if I apply V in over here then the input impedance I can get is a not necessarily capacitive that is what I propose to show there is going to be resistive element here.

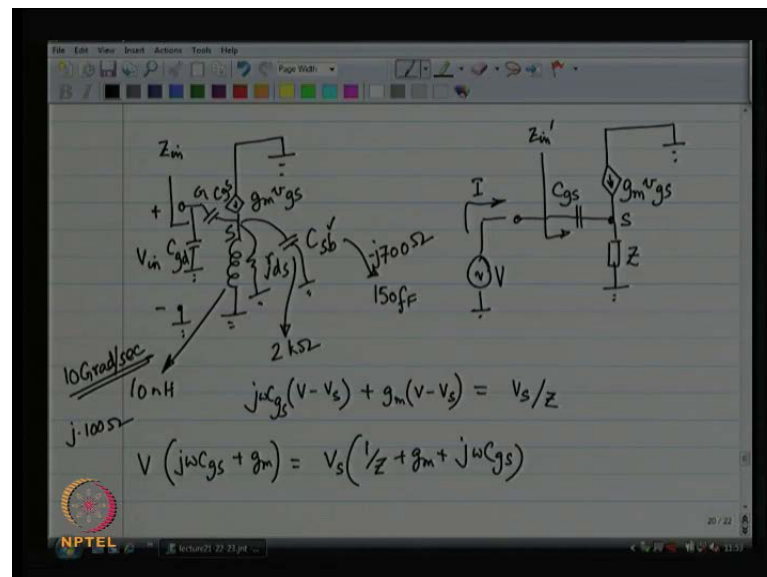
So, first lets show that and then we are going to move on to a L N a design. So, I have the I need to find out the input impedance. So, I apply a voltage at the input and I need to compute what is the current going in. So, to do this I am going to replace the mosfet with g_m enchain with r_{ds} now the r_{ds} is between the source and ground. So, I am really going to put it in over here then in addition there is C_{gs} there is C_{gd} and there C_{source} to body C_{drain} to body is irrelevant is irrelevant because both terminals are of C_{drain} to body both terminals are at ground drain at ground body at the ground. So, it does not really right.

So, this is what we are analyzing now I am going to simplify this a little bit and finally, this is what we have got. So, if this Z_{in} and this is Z_{in}' then really Z_{in} is Z_{in}' enchain with C_{gd} . So, let us just compute Z_{in}' and later on we will figure out what Z_{in} is Z_{in} is just an additional capacitor C_{gd} alright. So, this is what we are working on in the previous class and this is my source terminal this is where I applied a voltage V

and I want to measure the current I that is going in and to do this I need to find out what is the voltage at the source right.

So, whatever is the voltage at the source let me do kirchhoff's current law there. So, V_s minus V_s times $j\omega C_{gs}$ is the current going in through the gate plus $g_m V_{gs}$ is the current going from the drain that should be equal to the current going out of the source which is V_s by z right and you put all the V_s terms together. So, what you are going to get is $j\omega C_{gs}$ plus g_m on 1 side times V_s is equal to V_s times $1/z$ plus g_m plus $j\omega C_{gs}$.

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And this is going to further simplify and you will find out that V_s/I do not need to do that right now I is really this is I and z in prime is equal to V by I which is equal to 1 by $j\omega C_{gs}$ into 1 minus V_s over V let me know if I am making any mistakes V_s by V something that you have computed. So, you get z in prime equal to 1 by $j\omega C_{gs}$ times 1 minus $j\omega C_{gs}$ plus g_m divided 1 by z plus g_m plus $j\omega C_{gs}$ which further simplifies into 1 by 1 by z plus g_m plus $j\omega C_{gs}$ times $j\omega C_{gs}$ times 1 by z alright and then multiply numerator and denominator by z . So, you get 1 plus g_m times z plus $j\omega C_{gs}$ times z divided by $j\omega C_{gs}$ which simplifies to z plus z into g_m by $j\omega C_{gs}$ plus 1 by $j\omega C_{gs}$ alright. So, this is your z in prime and z in is this in addition to capacitor enchant C_{gs} d enchant which is not terribly difficult to find out if you know what this is right ok.

So, what do you see over here what if z is an inductor we started by saying that let z be let say z is a capacitor to start with or do you want z to be a resistor right now z is a combination of c s b r d s and whatever is placed at the source. So, let say z is a resistor. So, z can be a resistor in which case you have got a resistive component over here you have got a capacitive component here and you have got a capacitive component over here and then you will have a another capacitive component enchant with all of this fine

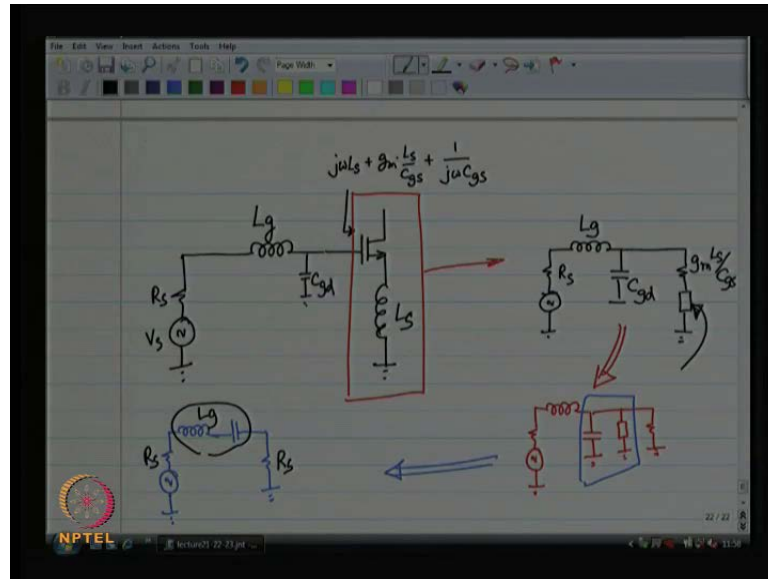
This is what happens when z is a resistor we do not want z to be resistors because resistors generate noise we are making a low noise amplifier. So, we would like to avoid all of these resistors alright. So, then let say z is a capacitor if z is a capacitor what have you got you've got a capacitor over here plus what have you got over here 1 by j ω times 1 by j ω . So, you have got 1 by minus and this is what you've got which means it is minus ω squared times this right.

So, this is going to give you a negative resistor components it is a bad new negative resistance means there is some sort of positive feedback going on something is source of power over here strange things are going to happen it will lead to instabilities do not do this do not make z a capacitor if if you make z a capacitor its very likely that your design is going to zoom into instable in unstable behavior. So, the next option for us is z is an inductor which is what I propose. So, if z is an inductor and this is an inductor what is this.

This is going to be z resistance this is going to look like a resistor its beautiful there's no resistance in the picture, but input impedance is as if is a resistor. So, this quantity if z is j ω L then this particular quantity is going to be g m times L by c g s alright and now it is just a simple matter to choose j ω L to choose your L such that these quantities resonate with each other at the. So, you want this to be resonate with this at the chosen frequency then you have got a pure resistor. So, over here right they need not to resonate actually you just need a resistive component.

In any case you have got c g d enchant with will right. So, your final resistive component will be different they altered by the value of c g d final capacitive component is also going to different reactant component going to different and then you find out what these reactant components are what the resistive component is and then you create your matching network to match to that

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So, this is basically that going to be a strategy I am going to have a mosfet degenerated by an inductor and this is going to generate some this is going to be behave like a g m cell in front of the mosfet I will need a matching network right and over here I have my source. So, typically this matching network will content 1 inductor probably actually 1 inductor should be able to do job I mean you have this is your typical L N a input its gonna look like this and let us just look at what what there is to it. So, looking in this point I have got $j\omega L_s + g_m L_s / C_{gs} + 1 / j\omega C_{gs}$ that is what I have got looking into the gate.

Now, question over here we said that z is the parallel combination of r_{ds} c_{sb} and the inductor and now i've just replaced z with just inductor what going on it is a wrong right you're right its wrong, but for an engineering approximation you can just pick L let say L is 10 nanohenry I will just give you some numbers to work with let say inductor 10 nanohenry c_{sb} is under 100 and 50 femtofarads and let say r_{ds} is 2 kilo ohms and let say we are talking about the frequency of 10 giga radians per second alright.

So, at 10 giga radians per second 10 nanohenries is going to behave like 100 ohms j times 100 ohms. So, j times 100 ohms and enchant with 2 kilo ohms is j times 100 ohms what about 150 femtofarads 150 femto times stand giga. So, 10 minus 15 times 10 to the 9 is 10 power minus 6. So, 1.5 milli simons. So, you've got about 700 minus j 700 ohms over here.

So, minus $j 700$ ohms in series with plus $j 100$ ohms is. So, if you put a larger resistor in series with a small resistor parallel combination is smaller than the small is close to the small resistor. So, the small resistor is j times 100. So, the parallel combination of all of these three is just the inductor right. So, that is why I just picked as an engineering approximation let say that the inductor wins what is the capacitor wins if the capacitor is larger then you have if the capacitor dominates this story then you have trouble you are going to get unstable behavior you do not want to capacitor to dominate you want the inductor to dominates. So, choose your inductor accordingly alright.

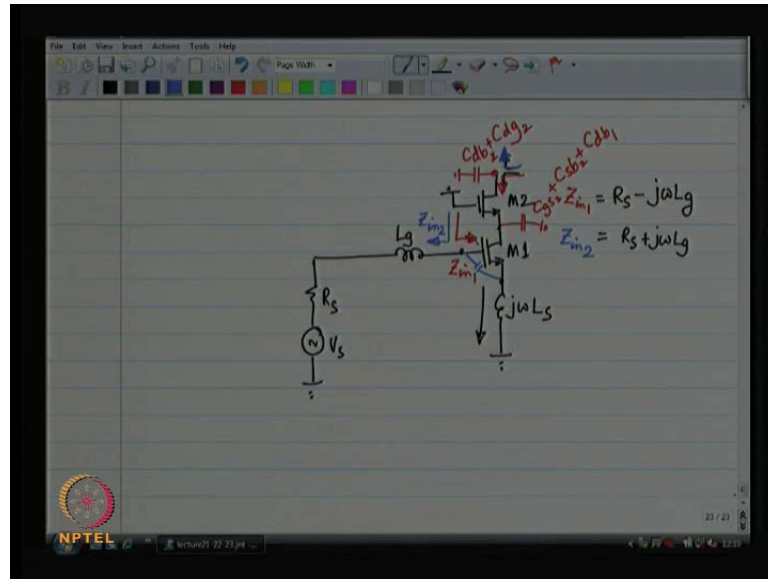
So, that is why as a first approximation I have said that input impedance z is just $j \omega L$ right. So, this was a first order approximation that we did substantiated my approximation fine. Now, you also have $c g d$ over here right and you have to do the matching. So, you have got an inductor in series with a capacitor is basically some reactant element.

So, this entire thing is being modeled as ((no audio 20:00 to 20:35)) some reactants over there and now you do series to parallel transformation when you do series to parallel transformation what happens to the resistor the value of the resistor is gonna to change its going to go up or down by the q its going to go up by the quality factor [-right] of the component and the value of the reactance is going to pretty much remain unchanged value of the resistor is going to to go up by q squared approximately fine then.

So, this is going to transform to this you've done series to parallel transformation then you are going to do the once more you're going to lumped all of these together and then you are going to do a series to parallel transformation I mean parallel to series transformation I am sorry right and finally, what you are going to get we will look something like this now it is going to be your job to figure out the values of this inductor and this inductor that you started with.

So, that at the end of the day you get matching. So, you have 2 degrees of freedom you have to fix the load to be equal to R_S that is number 1 and number 2 you have a frequency to work with at the chosen frequency you have to do the matching. So, you have to pick L_g and L_s accordingly now of course, L_g need not to be a inductor it also potentially could have been a capacitor we do not know until you work it out all the way fine is this good. So, far. So, good alright.

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So, this is how my input going to look like now what about the load the load also most probably it is going to need output matching what about gain how much gain are you going to get out of this . So, suppose have done your output matching how much gain do you expect how do you find out the gain whenever you have source degeneration. Source degeneration is a kind of feedback right. So, the voltage at the gate is approximately equal to the voltage at the source in the small signal which means that the gain is basically going to be this load impedance divided by the degeneration impedance that is going to your gain approximately am I right now this kind of gain is no good might not be good enough. So, what we do is we would probably like a cascaded stages over here ok.

So, what we probably like over here what you would probably like over here is to have a load the first load to be a low impedance node. So, this drain should be at the low impedance node what else why else you want drain to be a low impedance node remember when we did our analysis we assumed that the drain is a short we assumed that drain is the short and we did our analysis if the drain was not a short if the drain was the load than your analysis also would change right life would not be. So, easy alright.

So, low impedance is over there is desirable. So, suppose I have a low impedance you're the source of a mosfet is a low impedance node. So, I am I would like to have a low impedance node over there now all the current that comes out the drain is therefore,

going to come out through the source. So, the short circuit current all of the current is going to go in as opposed to going through r_{ds} right you do not want current go through the r_{ds} you would rather have the current go through the load which is the source impedance then all of that current now can be transferred to a high impedance load which means that you are going to get the full gain of you can have a large inductor over there alright that is going to be my strategy my strategy is basically going to be to have a cascaded device on the drain of the first mosfet of the input mosfet alright and then I am going to put a node at the drain of the second mosfet. So, what kind of load do you want at the second mos at the drain of the second mosfet you want a load which is matched.

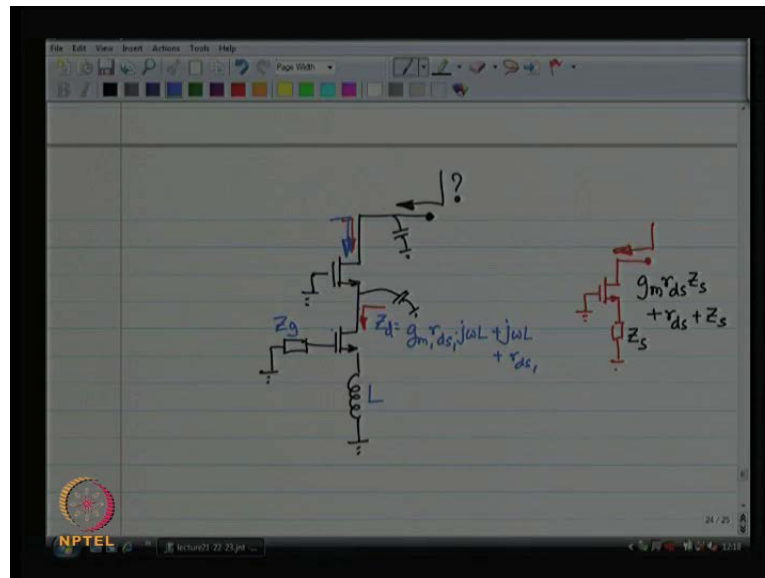
So, there is this impedance you want the impedance looking into the node to be the same that is going to give you the maximum possible power transfer maximum power transfer alright now what is the impedance looking downwards from the drain of m_2 what is the impedance at the frequency of the interest what is the impedance looking downwards from the drain of the m_2 question before before we do this what is the impedance looking in here its some sort of capacitor in series with R_S right and that capacitor is hopefully going to be resonator out by L_g right.

So, the impedance looking in there is the same as the impedance is the conjugate of the impedance looking the other way am I right the impedance looking in to the gate from this particular point is the conjugate of the impedance looking this way because if it is not then you haven't done proper matching at the input. So, at the chosen frequency the impedance looking into the gate of the mosfet is basically equal to R_S minus $j\omega L_g$ because if it is not then you haven't done your matching alright . So, far. So, good alright.

So, as far as computing the impedance looking here is concerned that impedance should be equal to the conjugate of the impedance looking downwards. So, the next question is what is the impedance looking downwards from the m_2 . So, when I look at m_2 the drain of m_2 has some capacitance to ground $c_{drain\ to\ body}$ there's also $c_{drain\ to\ gate}$ alright the source of m_2 has some capacitance to ground c_{gs} and c_{sb} as far as m_1 is concerned the drain of m_1 has capacitance to ground and the drain of a m_1 has capacitance to the gate the source m_1 has capacitance to gate and the source m_1 has capacitance ground which is already lumped into $j\omega L_s$ right. So, these are all the different things.

Now, when you looking to a terminal from alright let me further make 1 more approximation let say that the drain of m 1 is at a low impedance node. So, really the c get to drain of m 1 is almost like a capacitor to ground which is already taken care of in z in 1 and. So, on and. So, forth ok. So, we are going to keep that out of the picture alright now o g s is also taken into account fine. So, what we have got here are 2 transistors.

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So, this is what we have got alright and how do you find out the impedance of this you use your 1 of the 2 formulae a 2 favorite formulae first of all we need to know what is the impedance looking in over here what is the impedance looking in over there how do you do that remember 1 of your 2 formulae right. So, we are going to use that particular relationship to attempt to find out what is the impedance looking in. So, suppose this impedance is z then can you find out the impedance looking in over here its easy it is a same thing again right just that now its z enchant with a certain capacitor that you have to work with alright, but before that lets find out for z_s is it three really is that formula really applicable because right now I have got something connected at the gate.

The gate is not a short anymore. So, I have got something on the gate let say what I have got on the gate is z_g let say this is l . So, I need to find out what is the impedance looking in from the drain and how do you do this. So, I apply a voltage over here and I need to find out the current over here. So, if there is some V_g s. Is there any connection between is there any connection over here because if there is then they potentially could develop

some V_{gs} well that c_{gs} is really not very important because I have approximated that c_{gs} to ground that particular node the drain node is at a low impedance.

So, I have really taken this out of the picture. So, there is no coupling between drain and the gate this suppose to [lump-] to ground which is already lumped inside z_g right there is no coupling between gate and the drain which means that if you apply a voltage only on the on the on the drain then nothing is really going to go through there is not going to any gate current.

So, the current over here is zero which further means that the voltage on the gate is going to be zero alright this is. So, if the voltage on the gate is equal to zero or almost equal to zero it is just rationalized once more. So, what I am saying is that c_{gd} I have lumped it inside z_g because if I do not then my computation becomes very very difficult alright even this impedance computation becomes not. So, easy to work on. So, I have lumped c_{gd} .

I am engineer I like to do approximations. So, c_{gd} is first of all a small capacitor. So, therefore, its contribution should be less. So, I have lumped the effect of the c_{gd} inside that z_g and there is no coupling between drain and gate right. So, there therefore, no current on the gate if there's no current on the gate then the potential on the gate is going to be zero if the potential on the gate is going to be zero then we have got a old setup and once you've got the old setup then you know you can work [-on] work work it out your formulae will be as expected is this ok

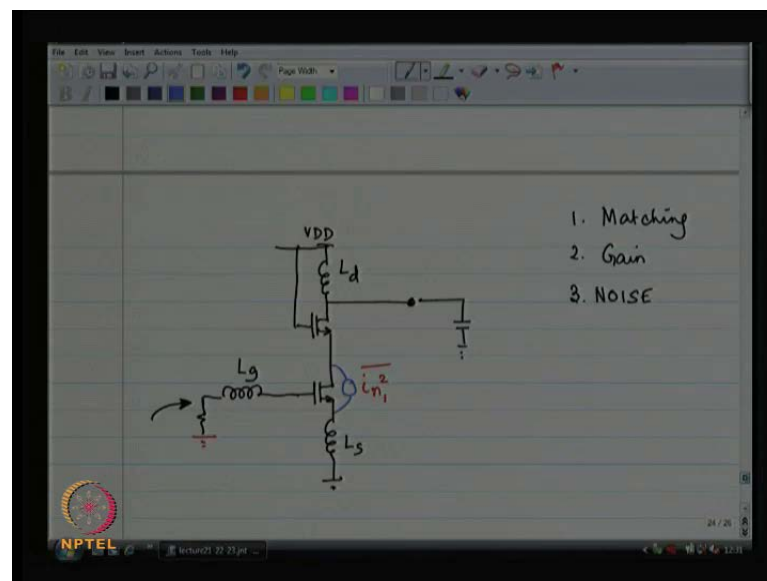
So, this is my logic and as a result what I am going to get is that this z_d is going to be approximately equal to $g_{m1} \times r_{ds1} \times j\omega L + j\omega L + r_{ds1}$ now this impedance is primarily an inductor a huge inductor in series with a small resistor alright. So, z_g is primarily an inductor further going this inductor is going to be in parallel with a capacitor right this inductor is going to be in parallel with a capacitor.

And therefore, that I mean hopefully that capacitance is not going to be terribly large which means there is still going to remain inductive which means that impedance looking into the drain of the second mosfet is going to be primarily an inductor. So, the the impedance looking in the final impedance looking into the circuit is going to be primarily an inductor you can work out the numbers once you have the numbers you can work out exactly what in what and you are going to get that that is primarily an induct.

What does that mean for us what does that mean; that means, that my load can be a capacitor which is terrific because I would like to drive a capacitor I would stage after the mosfet is going to be the input of the another gate input of the another gate is capacitor I love driving capacitors I would like drive capacitors I mean I I really like this.

I really like the fact that the impedance looking in overall at the output is highly inductive because then I could drive a capacitor right and you can work your way and find out exactly how much inductance you need to drive that particular capacitance right and if you need lesser inductance hopefully you need lesser inductor you would not need. So, much then you need to put another inductor in series with this entire huge inductor and make it resonate with the load capacitor that you're planning to drive . So, this is the story alright. So, my final L N a design typically contains tuned L N a design I typically contains three inductors. So, this is a typical tuned L N a design alright

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This is a typical tuned L N a design all of these values need to be carefully chosen. So, that you get your input and output matching at your chosen frequency of interest right and at there any noise generating components over here. So, we have worked on matching. So, both the input and the output need to match for maximum gain right. So, you have worked on that next thing gain we have worked on the gain this g_a [-in] this gives me this amount of the gain because if of the cascade stage I do get very decent amount of gain out of this alright.

So, we have worked on both of these qualitatively right once you get into the design you have to actually set and work with the actual numbers and then you will be able to design the real components may require simulation because sometimes the number becomes too difficult to handle, but we qualitatively understand the role played by each of these inductors role played by each mosfet why what we have done is what we have done in this particular design.

The third thing noise this is a low noise amplifier. So, I have to talk about the noise remember we have discussed our previous designs based on noise performance. So, we had a couple of designs before this we had this we threw [-out] through this out because of the noise performance we had this because we threw it out because of the noise performance. So, how does this play and it comes to noise.

What are the noise generating sources here inductor generate no noise wonderful we do not have to think about all of these inductors at all. So, the only noise generating sources over here are the channel of m_2 the channel of m_1 there're might be some noise in the gate of m_1 this is an addition to the channel noise this gate noise is coming because of the distributed resistance that the gate is the gate itself is made up of polysilicon material which is distributed resistive element alright and there could be some gate noise of the second device is as well. So, all of these elements will translate into noise ok

So, what is a story lets work 1 by 1 lets first look at what is most important to me $1/N^2$ square is in mind going to be a most important let see what the outcome of this is. So, this particular noise source is across the channel of the first mosfet. So, the way you analyze noise is there there could be 2 possible ways first of all you have to null all the other noise sources all the other voltage sources alright.

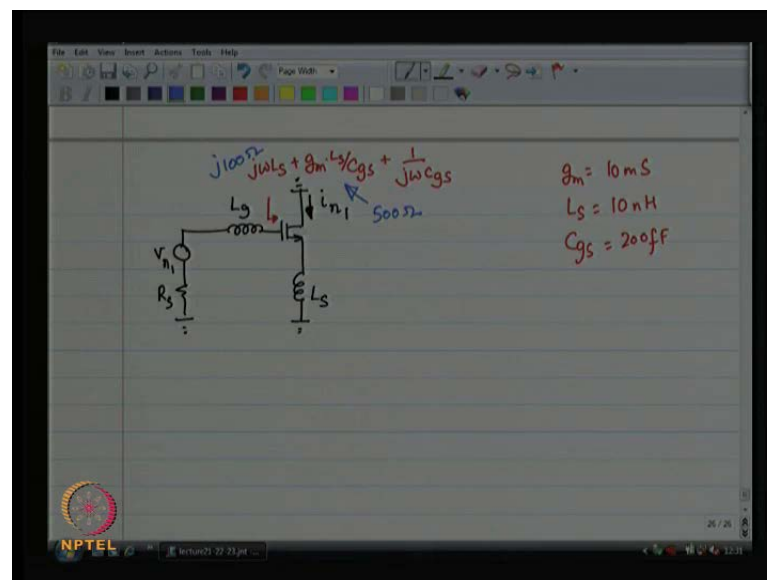
So, once you do that. So, I null that particular voltage source or the source resistance of the voltage source has some noise right noise is the noise source alright. So, when it comes to the noise figure computation this is just going to give me $1 + \text{something}$ right $1 + \text{total input referred noise} / \text{total source noise}$ I am sorry total input referred noise divided by the total source noise is going to be the noise figure noise factor. So, that is why the source noise is also important alright.

Now, this $1/N^2$ square lets worry about it first how are you going to work on it. So, there are 2 possible ways strategy number 1 is find out the noise that it generates at the output

divided by the gain of the L N a and that will give you the input referred noise strategy number b is try to refer it back to how much voltage I need to try to find out how much voltage I need to apply at the gate to generate that particular noise on the channel.

So, these are the 2 strategies I am going to prefer the second strategy because the first 1 is very too complicated. So, what I am going to is first we are going to null out all the other noise sources and I am going to attempt to find out what is the voltage that I need to apply over here what voltage can I apply over here such that I get. So, much current in the channel this is the question right and to answer this the remaining the the second mosfet device L d the node etcetera etcetera can be chanted out of the picture.

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So, what we have is something like this. So, let me apply a voltage over here. So, to generate I N 1 what is the voltage that I need to apply over there that is basically the question and how you're going to do this we need to know what is the input impedance looking here we've already found out what is the input impedance looking there right. You've already found that out that particular input impedance is $j\omega L_s$ plus g_m times something like this alright.

That is the input impedance looking in over there if you choose if you choose g_m to be something like 10 mS L_s to be 10 nH C_{gs} is let say 200 fF then what is the middle component resistive component 10 mS

times L s by c g s L s by c g s is 10 nano divided by 200 femto. So, so I get about fifty kilo ohms I am sorry 50 kilo times 10 milli. So, I get about 500 ohms over there.

J omega L s was j times how much I have forgotten did I rabid off no j times 100 and 1 by j omega c g s is going to be something much much larger aright. So, it is going to be capacitive and there is going to be a resistive element over there I think we are running out of time over here our 1 hour slot is almost over, but really what we are going to takeover in the next class is how we are going to compute I_N I am sorry what is V_N such that I_N and then again we have to square it means squared noise we need to certain mean squared noise. So, what is what should be the mean square noise voltage that I need to apply at the input right

So, we are going to continue this computation in the next class that is when you are really going to see what is the benefit of having this kind of a structure the what the role what is the role of the inductor over there so that is also going to be something important that we are going to demonstrate with this computation with this note on this note I am going to to stop and ah we are going to continue from here in the next class.

Thanks.