Analog Circuits
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Lecture – 15
Differential Amplifier

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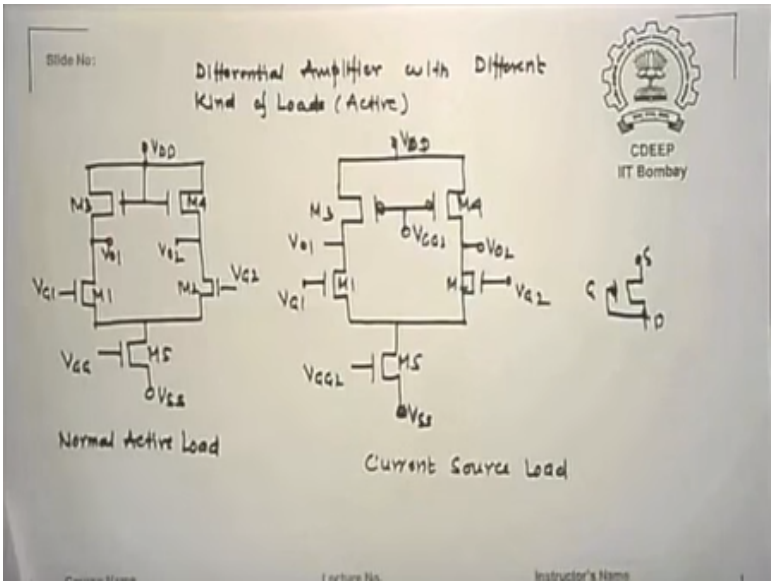

We were doing differential amplifier and we are already looped into the large signal analysis and now, today we shall see some of the active nodes. Different kinds of nodes which different can be, can have and how do we calculate the difference gain and the common mode gain. So, the first one which I am going to calculate is a normal active mode in which N3 and 4 are in saturation by a force that the gates are both are N channel but as I said they can also P channels. For this differential amplifier which I just showed with a active load.

The equivalent circuit, you can start looking from that circuits again if you see the figure, please keep this figure up, so that you know what I am saying. I am referring to this figure okay and there are M1, M2 are the drivers in which inputs received. M3, M4 acts like loads and M5 is the current source, okay.

So, with this, for this amplifier and since we said the difference mode is always used that Vgs1-Vgs2 which is equal to Vid/2 each of them +VID/2 at Vin1 and -Vid2 at Vin2. So, difference is

Vid/2- of- Vid/2 means Vid so essentially the difference can be divided half on the input 1 and-half on the input 2 so that the different signal remains Vid.

So, if I do that from the gate side, if you see at the gate side there is a Vid/2 signal which is going to be your Vgs1. This is my source of the, it can be the source for both M1 and M2. One can see from here, the source one can keep saying here. This is our source and down there is the transistor M5 which is your ISS current source and it has a resistance of RO5 it has output resistance of RO5.

Now, if this is your RO5, which is going to the ground and each signal is also provided to the ground. Please remember, signals are from Vid/2 is taken positive and down ground is the second terminal. So, this is your second terminal. For Vgs2, the signals are – Vid/2. Therefore, the same, the opposite signal signs+-, this is+-, this is+-, okay, and this source then is a common for both M1 and M2.

By simple thinking , it is, the drains are, gm1 Vgs1 gm2 Vgs2 sheltered by RA1 and RO2, is that clear? This is same 2 circuits together I am putting in one way because source is common, so I am going together on the both circuits. Then for the Vgs3 and Vgs4 please remember this is something interesting, these transistors are connected at the outputs here VO1 and VO2.

So, this is your VO1 and this is your VO2. So, a transistor in saturation, will receive some signal. You can see from there. Say, there is a potential going to be here and this is going to be grounded, so there is a VGS available for both the signal, as if is going for both M3 and M4. Is that point clear? If there is a potential here, they act like a Vgs for M3 and M4, okay.

So, those signals, if you look at it, can be represented as, gm3 Vgs3, gm4 Vgs4 shunted by their resistance RO3, RO4, but the interesting part is, this potential across, since, please remember this gate is common to both and going to the ground. The potential here essentially is VGS3 and VO2 is Vgs4. This is drains, these are drains of M3 and M4, okay. Since this potential is Vgs3 because you are connecting gate through the drain, okay.

So this is again Vgs3, which is also VO1. This is drain, this drain. Since the potential across is gate and drains are common, the potential VO1 is same as potential Vgs3, so maybe Vgs3 is VO2. So what does that mean? This is equivalent of odd of the potential drop across a current source is the same potential, then what is the equivalence of that? There is a resistance there of what value, 1 upon GN3 and 1 upon GN4.

Please remember this is a simple circuit theory, if the potential is Vgs3 and the current source is Vgs and current source Cgm Vgs. It has a resistance of 1 upon gm as straight as that. If I use this equivalence, also I, I do some interesting things. You can see since Vgs2 and Vgs1 are in opposite sense okay -Vgs2 is going to come. The current through RO5 is in opposite sense, if this goes like this, essentially the Vgs2 because of minus, one current goes like, this the other current comes like this. Is that point clear, Vgs2-Vgs1, yes.

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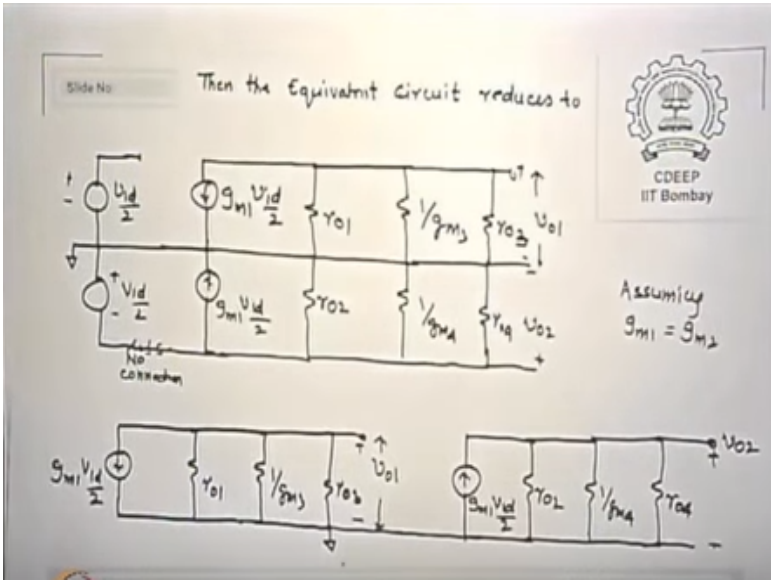

So this current is going through this, in this direction. This is - so added the current is coming out of this on the RO5. Generally gms are equally, Vgs ones are smaller, okay. Very small value, they may not be exactly same but maybe because Vgs1-Vgs2, this current sources are equal if gms are equal. So, what does this mean, how much current is really flowing in RO5? 0. Is that point clear? If gms are equal and Vgs1 is V-Vgs2 current through RO5 is 0 and this fact I will use everywhere now, okay.

If this is grounded physically by us and no current closer is, what is the condition for the source? It is equally grounded, please remember AC ground and do not connect it to DC ground. This is the equivalent of an AC ground. As I am sure no gm1s are same as gm2 and other signals are opposite sense. Then, automatically we say there is hardly any current in RO5 and since there is hardly any current in RO5 this potential is same as this potential, is that correct?

No current means, the potential here and the potential here must be same otherwise current will flow. Is that correct? If we say no current, the potential at the 2 ends of RO5 must be same, no current, is that clear? This current, go through this direction in RO5, this is- sign so this current comes out of this and if gms are equal and Vgs1 is Vgs2 by magnitude, the 2 currents are cancelling in RO5.

So, there is no current in RO5 equivalent leasing. Of course gms are different they will flow but otherwise and even if they are different they are very small difference will come okay. So practically what we say, drop across this is very small because very little current can flow or 0 current can flow. So, this potential must be same as this potential. This is what AC currents are, AC drops are, -Vgs2, is that clear? That is why it is - , is that, that condition is for difference mode signal amplifier.

We are looking for DVD deeds, is that clear? So essentially, it is a difference mode amplifier the currents will be in opposite sense, is that correct. So, if I use this theory which I did here, then I have a very simple circuit which is what the circuit analysis people do. They will just forget about RO5. Put your source of this transistors as to the ground okay, we have removed RO5 from here. Equivalently saying, this is ground, this is gmVid/2, gmVid/2.

This is RO1 RO2, 1 upon gm3, 1 upon gm4, RO3 and RO4. Do you see 2 circuits? Actually they need not have been drawn one over the other. This is independent circuit and this is independent circuit in between there is a ground just to save space. I showed you one ground, this one, the one, the opposite one, is that clear? These are 2 independent circuits, is that correct?

The VO1 and VO2 are independently seen by us, is that correct? Since the source is common, I am using common line here, one on the up, this side and one on the other side. So, this is drain, this is drain. Please remember, these are drains of both the transistors, outputs of M1 and M2, okay.

Now, if that is so, this is a parallel combination of RO1 1 upon gm3 RO3. This is a parallel combination of RO2 parallel 1 upon gm4 parallel RO4. Same thing I just want to show these 2 circuit can be as if independently shown to you, because this is source which is grounded, drains of, essentially we are saying same.

Essentially, so that is the source of a channel but which is connected to the same terminal, okay? And, therefore we say that they are commonly called drain of M1 and M2, okay. This is drain of M1 and this is drain of M2, but where I put the sign opposite now. Current source, It is going here and this is going there. That is right, if it is, then I will write - you are right, but here I did take do that, is that clear? I did this same thing here.

It is going to the drain, this is coming from drain to the ground. This opposite sign has been taken care, so if I am having these 2 circuits, what do I calculate? VO1 and VO2, how much is VO1? Quickly show me, -gm times, this load and this is +gm times this load. This is + sign is this way, this is + gm times this load is the output, -gm times this load is the output is VO1 is that clear.

So if I calculate both of these, which I did, you saw yourself again. This is only to show you how to solve circuits. So the gain of first is equal to Vid/2+ is VO1/Vid, gm1 by so much. Similarly, so if I write this expression solve it is, -gm1 upon 2+gm3+go1+go3. Why I put gs? Because 1 upon R+1 upon R+GM you have to invert it again, so expression becomes long enough so, many times add conductance, If they are in parallel is that point clear?

Whenever conductance, you have parallel things, you can convert them into their Gs and add them out, okay. Essentially when you want to know R, you will have to do one upon again, okay,

but this is much easier to do, conductance. So AVD1, okay. Two I have taken care through this I think. Just keep whether it is, so similarly I can calculate AVD2 that is VO2.

I calculate, the trick about this game is, if gm3 is much smaller than go. Will it be right to say so? trans conductance of an amplifier will be the order of 10 to power -2 or -3 amps per volt, okay? Whereas, what will be the order of conductance? -6 or - even higher, ok? 10s mega ohms or one by one to tens of mega ohms. So when I shunt a smaller resistance by larger, larger can be neglected. So roughly one can say, that is why I say roughly, it is 2gm3. If I substitute gm in this formula at ISS/2, at ISS/2 all then I am going to get is, gain is W1/W3. Is that correct W1/W3?

Similarly I got this; yeah 2 will come, because this 2 is appearing here, okay? I should have put 2 here, but that is same, that will any other difference it will get added. What you are saying is right Vid is Vid/2 - of -Vid/2, so if I calculate for this they will sum in the difference of Vid will anyway come and I actually add the 2 gains, 2/2, but same for the other one also.

So, by the way, when I take the sum of this, Vid/2 - Vid/2 will be get subtracted out anyway to get you Vid, is that correct? So if I get AVD, what is the, when I sum this 2, I get Vid, AVD is W1/W3. What does that mean, what is the advantage or disadvantage I see in this expression? The difference gain does not have any quantity which is depending on what only, the size of the transistor but nothing else no VT no beta n-, it is independent of transistor parameter except size, except size. Is that correct?

It is independent of everything else now, not even ISS, okay? So essentially this means, that I can fix the difference gain, by what should I do in this figure? I should adjust the size of M1, M2 with reference to M3, M4. The ratio of these, why I am setting, I did not take lengths? Because lengths in all transistors will be identical unless said otherwise, lengths of all transistors will be the smallest channel length available to you, is that correct?

All integrated circuits in Analog uses common channel links for all the transistor so is in digital, channel lengths are never changed, okay. Because if you increase channel length, what will happen? Digital or even here, the time taken for an electron to go from source to drain will

increase or decrease? Increase, because the channel length is higher so what does it mean in time term, as frequency term?

It will slow down the circuit, so at no time the channel lengths will be actually reduced or increased. However, if you recollect back, I say lambda is somewhere related to this and if I want lambda to be small, what do I gain if lambda is smaller? R0s are higher. So, what do they have, what I am now trying to tell you, that use longer channel lengths, okay, if you want output resistance to be higher, but if you want larger gains, you better use larger widths.

Is that issue coming to somewhere, g m RO term is now hitting opposite to E. Increase gm, increase size, increase R0 degree, increase lengths, okay. This means there is some optimum will appear, is that word clear to you, gm will go proportion to root W, R0 will go 1 upon, L okay. Now essentially if I increase W, your gm will increase or W/L essentially if I increase, I will increase GM but if I increase lengths.

I will improve R0, gmR0 is essentially somewhere in terms it gains. So, what do you understand? When I becomes bigger, 2 become smaller. There is some, maximum, minimum will occur. So, cannot have longer lengths, cannot have smaller, much smaller lengths. You will have to adjust many times. So the idea is in digital circuits, so is in analogue, do not change lengths often.

Use common lengths for everyone and what is the available length of device, the channel length given by technology people, let us say it is point .25 micron process, the channel length is .25 microns. So, you use everywhere same lengths, is that clear? this is a sampler shank number, channel length use everywhere else.

So when I divide W/L/W1/L1 1 W2/L2 L 1 l 2 are same so it is only ratio of sizes okay but remember it is W/L ratio I am taking lengths being same I am cancelling means essentially it is the size ratio W/L after 1 by W/L of the other is that correct but length being same we only say with ratio is that clear this part is understood by all analog designers or digital designer.

When they go on the chip because that is the way everything should be uniformly kept on and on you cannot do anything like this one the circuit devices will be given by someone else they may have anything we do not know so we just go by and connect and hope for the best so no integrated circuit equivalence can be created by our bread boards is that point clear to you because discrete devices are never identical is that clear to you discrete devices are never identical.

So what is the filament I suggested in the lab to do that there they look like I see there is an array array of transistors who use in which transistors are most likely to be identical and then you can make a define to that array is that correct otherwise no way you can actually create an equivalent circuit equivalent I see in a discrete okay.

So what does that what is that trick I am trying to say so do not make it open out of discrete components it would not have a gear but gains are good bandwidths okay however which amplifiers can be used with signals discrete transistors this normal amplifier common so is common whatever transistors you have you can always use them as a normal one against age against age.

Whether you need but if you want the deform or you want to have an open at no time so our components discretely and connected okay however as I said you learn if you pick up any object which has a more transistor you can pick up inside that then difference which will be available for each source being gay each of them if there are area food there will be 12 inch+ really depends on many other pins.

So if you use that then you can make it open so try it if you can get in our lab but that is okay unless you have seen that commonality of transistor parameters are guaranteed to some extent if it is on an otherwise take one transistor discrete put here on the breadboard this will never have any gains available and then because of the mismatches it will have so this fact has to be understood.

That why I keep links constants everywhere because all Isis will have common links we never change that unless of course as I say I am looking for a buffer state in, which I want really RO to be a particular value then I am a tailor it for that specific particular device that is called tailoring and that time this is difficult to tailor because it is a extra mask as we say and if you do extra masking that means please remember in circuit.

I do not know how you are not being told any technology we go through around 20 or mass steps as we call it patterning okay each mask patterning step cost you around a million dollars+ okay so if you add one mask additionally for doing one separate process for one transistor then you are almost asking me to do additional money on the same chip 1 million dollars okay.

Of course number of chips will come out of the paper but it will cost very increase per mask and therefore in India circuit we are awarding extra mask okay but if you need it yeah it is possible okay so have not shown you the gains the output resistance how much is the output of this lamp of how much is RA1 the gm3+0 1+g please remember.

However, I look at other one at this end how many resistances I will see are at this hour this+ 1 upon gm of this ok three resistances in parallel our country conductance in series gn3+go1+go3 which is roughly equal to gm1 upon g+3 by same argument RO2 is 1 upon gm 4go2+ go4 which is simple and the RLD is essentially called some of the RO1+RO2 which is nothing, but 2/gm3 if 3 and 4 are identical oh please remember.

Now in this transistor the connection was of this kind this is diode connected this is not diode connected the gm occur only when Vg s in very same across that means rail is connected to the gate is that correct only then the potential is same this potential is same as this potential is that clear only then that Commission is satisfying that the drop across ever current source has the same voltage drop then only it becomes gm this is called a Finley, a bad connection.

The actual output resistance is 1 upon gm shunting odd is fine but that are 0 are so high so it is only 1 upon share but in a normal this this Vgs and Venus are not same so they are giving you a are 0 only there is no 1 upon gm term because the VDS is not same as Vgs is that point clear to

you so this issue has to be understood that is why this was called active source active current loads the loads for n channel transistors is that clear.

So only what time you should use gems when there is a diode connection ok otherwise known otherwise a normal transistor with also al 0 sitting is VDS is not same as Vgs is that same potential drop her gm you understood no current year then the formation a word if this is GM some V and this is V this is equivalent of a V and then this is 1 upon G you can see now B/1 upon gm is the current which is EMV is that.

So these are only equal when this condition is met otherwise it is not equal so whenever that that is the circuit I showed you I connected them and therefore this gm term appeared I will do in which case this does not occur and in that case we will remove that gm it will be only our roads is that correct I am showing you parallel because RSU, RS may come or gm may come depending on whichever is smaller among the them okay.

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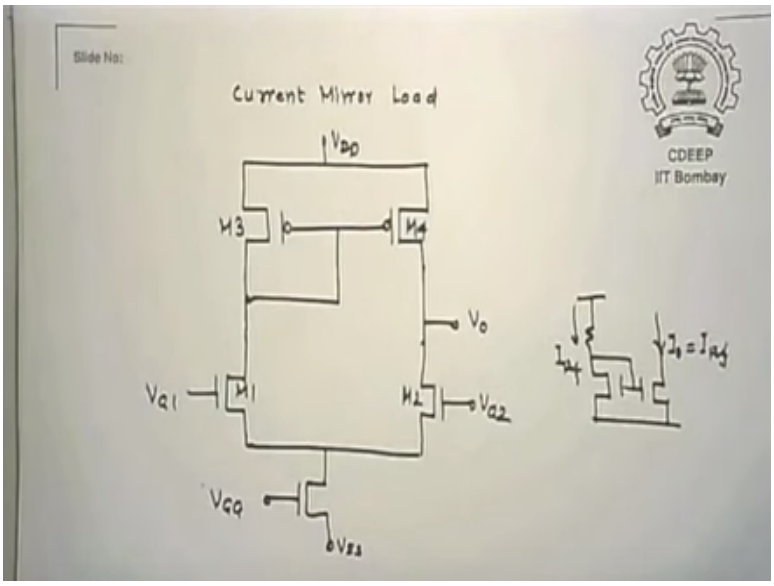

That may dominant whichever is higher than that my domain is that okay already is between the 2 terminals of VO1 and VO2-acre resistance is not a current cell fitness so net terminal the ground is equivalent of 2 times that okay so the next which is most important okay this is the most important circuit which all chips will be using okay what is the difference between the last

one and this what kind of load I am using now P even there I cannot put I use but what is the kind of load.

I are use now it is called current mirrors the gate of this is connected to the drains of this is that correct this is called current mirror so whatever current is here depends on the size being equal will be pass on into current in M3 should be equal to current in M foot provider it size of M3 say my size up M4 otherwise how much if this is double the size twice the current will flow now this current mirrors.

Which is what I have shown you sideways this is a standard current mirror which is equivalent Li put there now this is over standard as I say first stage up and open this is the first stage of a op Pam is that correct this is the first stage of an op-amp.

Which is going to be used the next stage is what we call single and an amplifier and that will become 2 stage opens this you may call first stage of M okay then we will have a 2 stage of M and we may have finally have how many third three stage okay.

But the third stage will be the buffer do you understand the difference between buffer and in common normal gain stage the buffer normally provides you currents what does it do larger currents is that correct so buffer the characteristic and report this is like equivalent li saying like this it will either provide current from here from power supply to the load.

Let us say it is the capacity load or it will discharge this capacitor to the ground through the load one so what does that means at a given time either it will source or it will sink is that correct so that is called the buffer stage is that buffer is were clear the output buffers are always designed for in which either it will source the current or it will sing the current is that correct this is the third stage of an op-amp which is the buffer stage okay.

But let op-amp come and we will come to it again so this is the first stage which we are looking into now here is something which the real circuit may look like this is your current mirror so the current is s is created from where now please remember what is the difference between last stage

and there I applied some potential Vgg here to get that current source is that clear in the last case I applied to our pipe m5 a supply voltage and I got the current source out of it.

Now I say if I do that I may as well use a current source a current mirror so here is my current which I am creating which I am now transferring to m5 okay keeping what now what I can do tricks I can use different with size here and different size here and I can adjust this value by the ratio of these 2 okay, this we already done okay.

This is your current reference VDD, but since these are equal VDS and Vgs are equal we just calculate and find how much is current here if we know this please remember in this case again PGs six and Vgs5 are same therefore the currents in M6 and n PI4 same with the size ratios is that clear this is this we did in mirrors so this is a biasing circuit, what is this called this called the biasing circuit can I replace R also by transistor shunting to the drain.

I can convert this in the are equivalent of that so I can replace are also valid on this right now I showed you a resistor but in reality I may have a transistor so I may have a current here which I can fix and I can burn mirror it into this which a R value I am looking one method is actually create same current transfer here as one to one or make any current here take a ratio of these 2 and push the current of your choice in my okay I have answer 5 million current.

I am a cleared one here, but keep a ratio of five and pass 5 millions here is that here so that is the way we can create the current sources at m5 this is a potential VP this is my M1 M2 and Vin this now few things you should know from here 3 in 1- V x Vid which is nothing but Vgs1-Vgs2, we as usual apply Brd2 here-Vrd/2 to the other gate.

We also know Vgs1=VP what is why I am saying it Vgs1 is the same as Vgi just now said the resistance of our pipe is large enough then and if the 2 currents go opposite this potential can be treated equal to Vss and right now for DC it is- VSS for AC it is how much ground so, we say VP is close to the ground is that current because I am not sure whether they are exactly identical.

So I may say okay VP is roughly close to the ground or can be treated ground so, Vgr Vgs is same Vg and Vgs because s is going to the ground so Vgr Vgs is same so we show Vgs1 is Vg1 Vgs Vg2 condition again same as just now I said is that point clear just now I solve the case I say VP can be treated equal to close to the ground ok.

If that is the equivalence we agree then we calculate this circuit should be kept sideways this I am keep using there is a potential node which is essentially VO1 which I am calling as VX for the simplicity okay is that correct why I am not calling at VO1 specifically because I am not picking an output there ok I am only picking at output at this end.

So I call that node as VX ok is that point clear this is essentially VO1, but this I am calling it because 1 means either I am taking an output I am not calling this node VO1 essentially because this VO1 means I am picking an output which I am not I am only keep finding what is the value of voltage here please remember by making this connection this is my gate this is my source can you tell me why source on upwards in P channels volts must go down ok applies there will not be possible of same direction currents.

So you can see if I connect link like this this potential which is here this is shorted this potential and this potential are same is that correct this potential RC this is what I used no because they did this value itself I have calculated the current you understood here, I am not hitting ground here I am treating- VSS as the value and we reduce this value.

So when I calculate reference current I am using VSS there so, when I am keeping this they by making of choice of this which is the gate of this I am ensuring this is positive in a greater than meeting with VSS that is what I did now and I calculate the current and I assume this transistor and saturation I am I am actually forcing the value of resistance such that transfer remains in saturation with that kind of VSS available.

If it is ground at this value may change is that correct if - where is it will change differently okay but it will force your transistor to be in saturation so what is Vgs for in your circuit keep watching that how much is Vgs for the Vs for which is the source terminal F both the transistor-

VX yes or say vVs4 and Vs three are same this potential- VX is the Vgs is that correct we know this is grounded place if I write now as I said this is yes potential of this- VX is the Vds source so this is another VX- this equivalent leasing okay.

VX-VS is Vgs yeah that is what I wrote no that is because it is a p-channel device it is a- potential will appear okay so we say Vgs for is Vs for- VX okay we are you can also call it - fair enough okay this is V as 3- Vs lyrics please remember VX is the output of first M1 M2 amplifier with m1 receiving VI D by 2 please check it what I say vo 1 is the output of a defend at terminal VX when M1 this is VRD/2 2 M2 DCs- Vid/2 is that correct.

So we know VX is nothing but gm reality by 2RO1 parallel RO3 and for York someone while asking now put one upon gn3 here also is that correct if that so this is RO1 3gm is some of this so VX is VO1-gm1 id/2 into this since RO1 3 is normally equal to 1 upon G and 3 so VX is- gm1/gm3 times Vid/2 for 1 input from the M1 side the output is Vin-G we did it for common base amplifier earlier.

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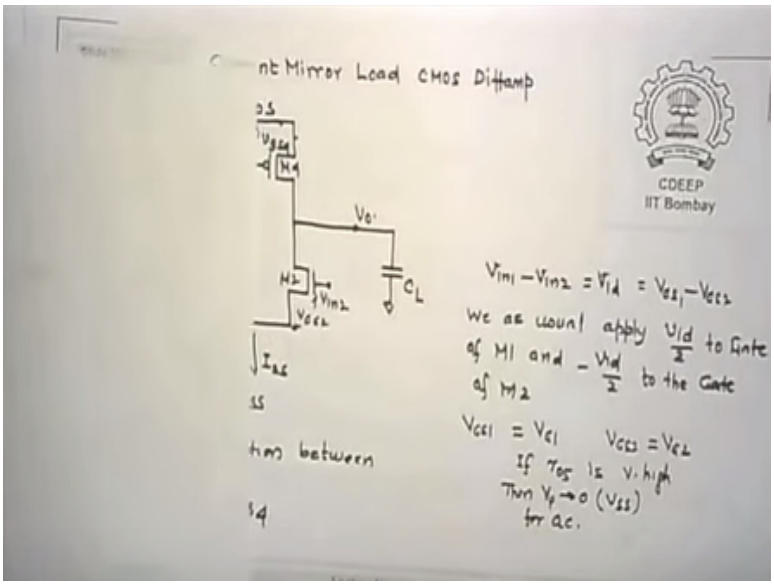

We are just writing the same expressions so 2gm1/gm3 x Brd/2 is the VX okay if that is so can I calculate Vgs4 therefore ok so having done this I calculate with Vgs4 which is gm we already buy this now I have for these M2 this M4 and for amplifier you look at this I am talking the VO

is decided by how many inputs may be I see a hamper a DAC a hamper m4 is also an input have an input and M2 also has an input.

So the output voltage by superposition will say is the available because of this+ available because of this please remember there is a signal coming at the input of M4 Vgss for is a small signal which is coming as an input there there is an input anyway here is that correct so this potential is not only governed by M for inputs but also by us are not only do them by M2 inputs but also by and for inputs is that clear to you save this value in this case is signal available to you small vgs for RBG s3 is available to you this acts like an input to M4.

So it will also amplify this in this is a given so input any row bias so it will also amplify is that correct the sum total will be the net pure value for you occurring because of M2 and M further we input her or M - maybe AC input say they know milky output, the only thing is since transistors are assumed in saturation we save your signals are small enough then what is the condition.

I am satisfying linearity superposition theorem is only valid if it is in T so our assumption is because of the condition I enforce both systems are in linear mode therefore superposition is also clear is that clear to you superposition is only and only valid if system is linear and please locate I repeatedly tell you which is the question I have been asking and yes y is equal to MX+3 is aligned.

So life looks like linear but the system is nonlinear okay this fact has to be appreciated in a whole of the life of electrical engineers this is a AC signal, which is connected here I could have m1 coming at here is connected directly to the gate of m4 is that correct currently okay enough to connect output highways can put over neatest again bar I have ever is that correct though there is an output below 0 area he is castrated okay.

So I will never bet I solve this problems our calculate VO do 2 Vrd for VO do 2-Vrd/2, I also assume all transistors like gm1=gm2 that is M1 M2 are identical and M I am force are also

identical but M1 N3 +M2 M4 I am not identical only players are identical M1 M took identical N3 M4 identical gm3 is gm4 RO3 are 4 I solve this problem that I only see this is the line.

I said VOV gs4 VO we have - yes their signal cut some kernel output is that clear the next is this so here this is due to Vgs4 do you know what why this is V useful it is curvy here is for curvy IDK tell me the expression the - me substitute cardiac this is due to Vid/2 into arrow to 4K what is the output resistance at V0 the output resistance after M10 parallel to the output resistance of 4 and there is no gm terms appearing here.

Because it is not diode connected whenever a diode connection make it gms1 upon gm if no rod connection it is only RO is that correct so if that is a as I say RO will get cancelled simply because not necessarily removed if that numbers are let us say RA is not very high in which case parallel combination must be taken care but as I told you gm will be order of -2 -3 ampere volt okay, where R is in the order of -6 - 7 4 I currently.

So essentially we are saying that are those are much larger than 1 upon G ins and therefore 1 upon gm is a good approximation in most cases, but I have never written directly I will first show you a parallel combination and then I say if this is larger I can use that term so in real life calculation where is never neutrons numerically they will get eliminated 1 upon thousand+1 upon 5 do whatever you it is a point to only.

So that number will automatically get eliminated you need not do anything you solve parallel combination the other terms will be small enough to be used in the expressions is that, but if you are sure and you can write there is nothing wrong these are too high compared to I use this that is what the electrical engineers are all about ok, what is the output resistance of this stage, so a VDD is VO/Vid gm1 upon go2+is cos.

Of course yeah, but expression they what is the upper terms are talking about what is this upper term is because of gm1 of M1 which is same as gm2 is that correct gm1 is decided by both factors please look at it what factor gm1 is decided beta - which is in given technology the size

ratio W/L into the bias current Isis there from this is fixed from the mirror side which I am fixing what is our Giotto geophone is lambda 2+ lambda 4 into is s/2 I can take is s about now okay.

I do so one thing very interesting is happening and that is why I have shown you this expression I will come back to this expression please note down this is relevant expression in our difference gained value beta and del W by L 1 divided by is s upon lambda 2+ lambda 4 they are equal then 2 lambda ok then this 2 will also be oh I just now showed you and okay, the output resistance seen at this terminal is because of this this is a root 2.

So, terming for their resistance parallel manner so RO2 4 is a parallel combination of RO2 and out of did you see gem term there no why cause it is not diode connection it is an open-ended blocks okay so I calculate this term I calculate the output resistance R zero which is our 2 parallel RO for then I see very interesting 2 functions the difference gain is proportional to W/L of M1 or M2 are equal and one transistor is identical to him to the cage or driver cell size same over the larger the W/L.

Larger is the gain is that correct larger is the size larger is the gain but one interesting feature and I am seeing this difference again is inversely proportional to root of ISS what is he trying to say that is if you work at smaller currents your gains are higher which is very very typical and normally what do we say from the power and get the game it is now trying to tell me you that reduce the bias currents.

If you reduce the bias currents differential gain is higher okay however and are also university proportional to values of 1 upon sorry 1 upon lambda of M2 and M4 if you see here R0 which is 1 upon lambda 2 by lambda for this so if you Cr2 for value it is 1 upon g Rho 2+g of 4 which is 1 upon lambda 2+lambda 4 x is s.

So the output resistance is inversely proportional to is s so if you reduce access output resistance increases if you reduce access your gain increases so why not always keep small currents power dissipation it is lemony both active and I go for open this is the place where I will come back to you.

So now if I reduce Isis I will lose something this condition is valid what I shown you is a valid statement there is nothing great thing going wrong is that correct then why are people do not want much smaller currents the net output resistance of do you want higher or lower I have not stated.

So far is that correct next stage but I have is curved you cannot decide arbitrary like this because you do not know what load you are connecting is that correct that is why too much smaller currents are to higher current both may actually hurt you very strongly it is that clear now Li but this is not the only reason there is a major reason.

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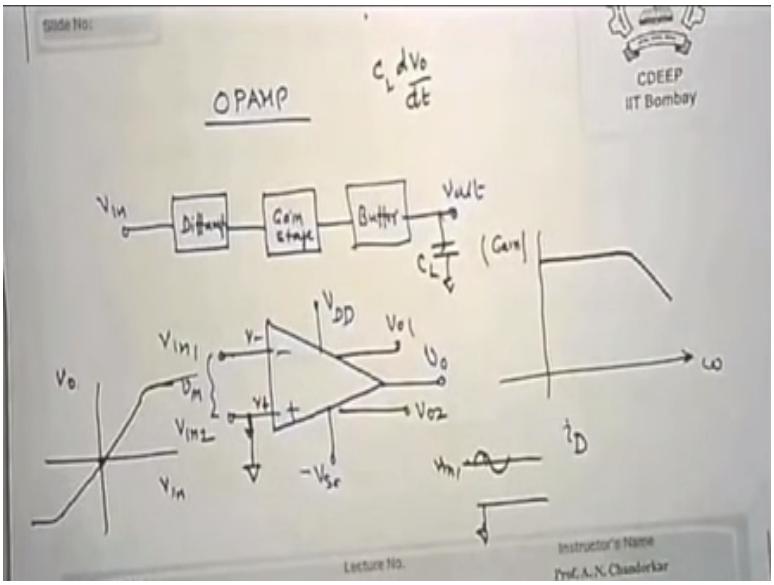

Which we will see later corporate this capacitor could charge chemical current get CA Dvo/dt and this should be supplied by the buffer currents either this or sourcing or here sourcing current cast same arrow Karen so it is come at left the DA is related hang.

So what does this essentially will tell if RSS is smaller the time taken to charge or discharge this capacitor will be larger or smaller number time smaller current will charge or discharge the capacitor slower is that correct this term dv0 by dt is costly rate DV is output charging to higher low is called dv0/dt is called slew rate and that is decided by ISS/CL.

So if you want larger slew rates which you will require for high-speed performance in connections then you must have larger currents but if you are a larger current you have different stage will have lower gains is that correct, so yeah II German happy that many but they open because your last stage connect hand that may finally tell me how much I said I will be allowed because someone will specify you is that point clear what is once precision open gives fluid it has 5 volt per microsecond that is the slew rate they will say ok.

Now to meet this new rate for the given load I know how much I said I will require and that is the is Li ler to use back so that I can use a good defense so I assess is not very much in my hand which I showed you as it I can vary I assess just power 7 here it co hot current you do throw in the open design cut this away so T3 a cold terminal is my domain enabling our input common mode range and output common output things also are functions of Isis is that correct.

So for a given open how much is the outputs impossible how much is the ICMR given to you what is the slew rate you are looking for that all together will decide and power dissipation will decide how much is your I assess and therefore how much is the gain is that correct so it is not independent of everything because I want larger against needed mounting them or I should have very may live but if you are very low loads then.

If they were you to decide outside so essentially design of an op-amp does not just say I assess come cord oh I got to any for point and parameters you have to keep adjusting so that roughly you get where you are expected to reach in the parameter this is what the design is on so is that clear I am teaching you something more on the design side because at the end of the day we are not going to use analysis everywhere.

We are going to design shapes or design component design parts, so our designer I must know where I am constrained okay analysis what does it do it gives me constraint either then I know I and I know analysis I know this changes this this changes this so if you want this please give me this if you want this so this is what designers do so at the end of your course if you learn this that electrical engineers are not going to be just using the component.

They are the ones who are going to design systems ok other designers we must know my constraints and if those constraints have to be met analytically I must know what changes want the whole course is therefore slightly changed from last so many years is more towards design values because secondly the maybe we want to push you that you are going to be designers in life ok.

Even in the banks it will be making some portfolio you will design something so at the end of the day engineers design something ok, it does then the moment coming maximum minimum is also fixed but within that range also how much lower side or higher side your viewpoint is correct if too much or too less I am a great out of saturation or go to cut off, but I showing during a sufficient rain in which I will still remain in saturation.

So, which may be low or low to I am seeing something, which may hire loath I see something ok so during designs this condition which you said is always true saturation key, see jalapeno 9 everything else is after if device comes out of saturation you are in a nonlinear zones ok so we are not going there is that correct so this point is very taken, but there is a still values lower side and upper we were to work as a analysis.

I do not care no Joe value minute output push to value all the art world by a vampire a to beware gain chaotic a are at bolt by bolt on tk8 again but it gained amplifier Kirkuk occurred moment the showered car so I had to know I must have 10 to power 3 or thousand or 500 gains, I imagine so all these values analytically I damn care what value I substitute in formula and whatever I did so this is the opening gala date on your ticket but in design I will be given specs this is what I had to meet.

So, I am trying to use some ideas how do I think I mean I do not mean I a designer things he knows analysis 100% therefore we teach you analysis from there I know each how it connects okay and then given me final this is Debbie Meyer and I took a corner then I had okay he is got liquor down to yeah hi Scott Walker calm I we are just the parameters is that clear so this is a issue.

Which I thought I must have hammer on you okay so please remember designs are part and parcels of all electrical engineer further matter engineering but more so violated okay so this finishes the amplifier part which amplifier we did this is a be found with what kind of words current mirror Lutz the first case we do have to note with diode connections but there is the third one also current sources itself that circuit.

I will not saw us on which one is the first circuit which I showed you first time may be here current sources say m3 m4 they in distances kit now again it now is well gf1 know I have ice yeah equivalent R has a equivalent are head easiest way to solve is this circuit is that correct this is RO3 this is RO4.

So it is very easy to solve a current source load is that point clear if this is simple resistors then we already solved that deform case with simple 2 resistance this is the case only advantages this will all very large resistance is a good current source means output resistance is how much for that so RO must be very high in 2, 3, 4, 6, or 7 for that because you know there is no gm term will appear here.

Because Vgs is not same as V is there is no diode connection going on that means the voltage drop is not same across the current source as the gm times that if they are same then it is equivalent of a resistor but otherwise arrow is always there of the transistor current RO- hey after that so this is equivalent of ARO here on equivalent of a arrow here okay.

Just solve it and you will get the gains for this also okay so this finishes deform as such before we quit I will not solve only well just show you what how quickly we solve this we have been telling as if the mass the fans are only going to be used, but in real life which opens are still on bipolar 741 okay these seven for one CBI market me rascal see we are talk about seven for own original.

So there are mass opens seven for one again is seven for one bipolar hope M will be better than mass of M or not is bipolar systems for an amplifier that superior to most systems or not okay basic idea is gm is gm is better in bipolar for everything similar compared to Moss yes so,

bipolar amplifiers will be superior to boss amplifier any day in fact but what is the cost I will pay for YK t converted I see but I read GM marathoner white chili up.

Now I see I am because we 200 IV micro me rocking a minimum say like each other which means at the cost of power bipolar then we say why not use the same technique in a moss and use large powers what is the problem because independently if I am using I may do that but the power supply limitation may be increasing beyond 1.5 which may go to 5 volt and volt which no mass transistor gates can sustain what is the problem if the gate gets larger voltage right.

Now if the electric field is larger than the critical field the Moss oxide may break down so I cannot just arbitrarily increase Bdd is that correct so that will have to work at smaller voltages and for this the currents will be smaller and therefore gm will be always smaller than barbers for similar things only thing at one day I will get is no power since the chips are going to have no power dissipations we will prefer more circuits on any silicon chips ok is that point clear.

While silicon chips are always presently more simply because of power requirements otherwise you give a huge heat sinks big silicon area I may use bipolar circuit as much and do better performance ok you smash make a fertilizer and I have a smell a cake it was maybe a ester is that correct which my Vgs tire current driven circuit say avoid regimen circuits so it is my sub-zero currents you scream.

I would be one I will be too however chill input should be voltage as being one and being - ok difference is still VI D by 2 okay we had you - quiet - same method currently yeah hobby current source square cross a resistance say REE meter yes, the equivalent circuit and been eyeing it was make re resistance bulletin re small re yeah Rst emitter to substrate that is normally used in many books but that is around less than 10 ohms or 5 ohms okay.

In actual calculations so if you do not use that it is much easier to solve otherwise your RS+ Barbary I got or yeah that is all more 8 mega ohm a bacteria number aid of this but I do not give me a circuit memory using of them but our books they can get so you will find they will use this term because we are actually solving full circuits.

So they will show you the RS part are small resistance which I showed you between substrate and emitter will be shown to you there so circuit will have this resistance here+ this resistance here so the emitter will see small resistance due to the emitter substrate this+ Ari's Mia is my neighbor's residential which resistance I normally neglect in analog RC RB, RB dash and RS or re they may be use in case you want accurate analysis in analytical mess with know what mine are their job of spice paste all currently.

So, automatically built-in language so you do not have to think they will come there in model okay, so they will take care of themselves you do not have to worry on that since you are doing numerically opening both up under camera but on in Armco yeah but is GV they are all the time following a current matrix for a given voltage matrix with given conductance matrix nor scale me a calculate coke.

Which be modeled a wonderfully I am go cat active I am so sick day for any come out put up a that is what spices or you must have seen you just give an input file and hope for the best it may not be the best unfortunately that is where the problem is, see you.