Analog Circuits
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Lecture – 14
Differential Amplifier

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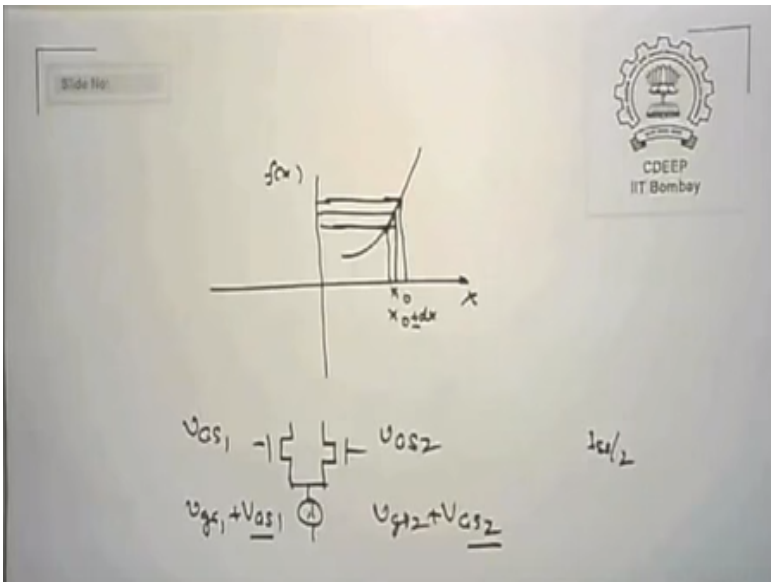

Last time there are some, very small problem. Let us say I have a function of FX versus X and it has nonlinear relationship. I have a function FX which is nonlinear with X and if you see very carefully there so I will fix a value of X0 here, and I take a slope here at this point so for a small variation between say X0 and X0+-DX.

If I see linearity maintained, then I would say the output will be proportionately linear at these points. Exactly linear therefore proportional, equivalently saying X0 is your DC value and +-DX is the AC signal, so AC signal does not make Vgs-VT currents. Current are essentially DC current which is capital Vgs minor proportional to minus Vgs-VT.

Around which AC signal just super imposes. Therefore it does not change the status of the transistor just because small signal overrates on that, is that clear? Last time someone was asking is small VGs changes what will happen that is our assumption that in the range in which I am looking for small signal at +-DX as the word I use and not X.

Then I say in that range the x0 remains as a constant at around X0 and therefore currents are only proportional to DC. In the case of define for example, I said if you are small VG, vgs1, vgs 2 it is essentially Vgs1+Vgs 1 this is Vgs2+Vgs2 and if the transistor is biased to RSS by two on this side then Vgs1=Vgs.

So, DC is essentially the capital Vgs, the signals are small and Vgs1 Vgs2 which we difference we call VID and some average of the two we call common mode. So do not get confused every now and then that small signal to last signal unless stated otherwise, then all this is nothing to do with this circuit in a circuit for example the AC value does not change the bias point. That is the assumption we are making. Is that clear? That AC values are small enough therefore they do not change the DC operating points, okay.

That is how we solve all our circuits. If that also keeps changing and there is no question of we, then with the signal analysis will call out large signals, but my signal is varying large enough all around and may be linear or non-linear, we do not care. Then we will solve accordingly, but when I solve a small signal circuit, I essentially say DC operating point is fixed around which AC signals are super imposed.

Therefore do not change the operating points. Last time some query came, so that once for all be clear to you that there is nothing called small signal varying the DC of operating point okay, so the RSS/2 remains the DC values is that okay.

This is general, this is nothing to do with what we were doing last time but just to tell you that in future do not get confused between the two words and for example, just for the making that point clear and you need not write all of it here because this is just copied from Smith and served on Smith's book. This is just because that day there was an issues so I thought that maybe I will discuss last signal operation for the deform.

Which we discussed last time or we say Vgs1-Vgs2 and someone asked how it is equal to VG1-VG2. It does mean essentially saying that sources are the same potential so the difference of VG

and Vgs is same. I mean, they will be same. In choice of biasing be assured that is IS VS S were so guaranteed by us that both transistors are on, are in saturation then we write two currents IDS1.

If you are the circuit diagram maybe I can quickly show you a little shown here. This is our SS this is minus VSS if needed, this is RD, this is RD, this is my BA1, this is my VO2, okay. This is my Vgs1, this is my VG2 or VG1. This is what the circuit I am talking about as of now, this is a typical deform which is shown here which you have a circuit already on your paper. So, I calculate I show right now lambdas are 0s.

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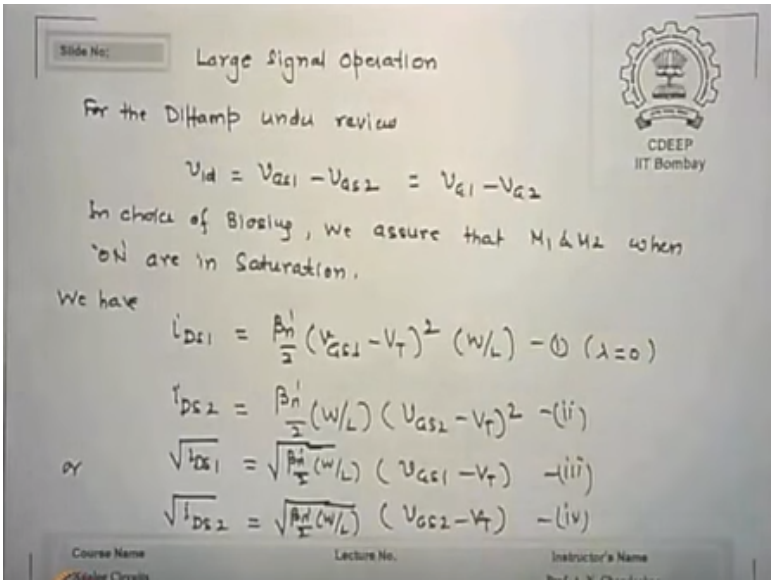

I told you already if you add a lambda term what creates the problem, the current becomes nonlinear because there will be a VDS term will start appearing in the other side, 1+lambda VDS and it is a nonlinear equation and numerically can only be solved, okay. Otherwise analytically, I am not saying it is impossible, you can, these are all with the nonlinear terms but how much to linearize are straight again.

So, I can assume that lambda is 0. As far as analytical calculations are concerned, will use lambda not 0 for what purpose? for every other purpose I may say lambda 0 but for one thing I will not assume lambda 0. For calculation of R0 because 1 upon lambda already is essentially R0 otherwise I am saying R0 infinite, okay.

Which is not really true R0 is finite. All other things assume lambda are small enough and can be 1+lambda VDS term is 1. So, I get the currents in the two amps, IDS 1 and IDS 2. Write the equations as they are. Then, I will take it under root of this IDS1, under root of IDS - so I get beta n- W/L, beta n- W/L , Vgs1-VT, Vgs2-VT.

Thus, under root of the two saturation currents of the two arms of the M1 and M2, This is for M1, this is for M2. So, while I am trying to do it, I am trying to do some math on doing this I want to get some, this value related to VGs once. I already made an assumption that we have already said that VID is VGS1-VGS2 or equal to VG1-VG2.

Which I am trying to go back to that value, is that clear? I will just make under root of both the currents and got these expressions.

However I already said, VGS1-VGS2 is VID because we already said DC values are equal, all that is saying is AC signals. So, this is still small signal VID, is that clear? This is still small signal DC is cancelling.

So, IDS1- IDS2 is beta W/L by VID. However, we know the net current is RSS so IDS1+IDS2 is ISS. Squaring, now this time I square, so I get beta N/2, W/L I will introduced inside beta n- into VID square. I expand this so I get IDS1+IDS2-2IDS 1IDS2. Square of this, expansion which is beta N/2 into VID square, but this sum of IDS1 and IDS2 is RSS, so I substitute ISS-2 IDS1 IDS2 under root of that is beta N VID square.

Why I am trying to do it, second it will be visible when I show this. Please note down what I say, I just get the currents, take on the roots subtract it and square again, okay? Nothing great, no mass were thinking, why I do it, is the next slide will show you.

So, if I now substitute, I go back into my IDS1 term and IDS2 term using the expression which I just got, I can prove that IDS1 is RSS/2 +- beta and ISS, VID/2, 1-VID by square. This is a quadratic equation solving and this is what we did, okay. So, by this I can get this current and

this current IDS1 and IDS2. Did I get the point? I just resubstituted the last equations which I got. I got two IDS1.

So, I can solve this equation now and using this, I can evaluate IDS1 and IDS2 - in terms of ISS beta and VIDs, two equations I got for IDS1 and IDS2 - now one interesting feature from here you can immediately see, you write these two equations and see what I have, the way I have written them. If you want in between terms all yourself this is given in S address with book.

So the point I am trying to raise from these two equation is if BRD is 0, what does that means VID is 0 means? That essentially I am saying, common mode we are received. Is that correct? Vin1 is equal to Vin2, so VID is 0, okay. If VID is 0 that is this term is 0, I get IDS1 is ISS/2, IDS2 is ISS/2, okay.

So what does that is essentially saying, when there is a common mode signal or that means there is no AC signal as if running through, equivalently say, half the current will go to the M1 and half the current will go to the M2 that is what we started with in this provable, that half the current moves in to one arm, the have the current goes into the other arm if you are at the same inputs are given which is obvious.

If VGS1 is equal to VGS2 - both will draw equal currents, that current is the ISS. So, half of current will, so even this equations essentially is trying to tell that, they at VID equal to 0 but if VID is much smaller why these conditions have been brought. I want to know how much VID. I should be allowed for such condition to meet, okay.

Please note down, this is one interesting condition which we got IDS1 is ISS/2 when VID is 0. However, each current is ISS/2 which is ID1 or ID2, which I can write beta n- by W/L Vgs-VT square which is beta and VOV square.

So it says ISS/beta n, sorry is equal to VOV square and then I substitute again IDS1 IDS2 in this form, okay. So I will get VID/2 by VOV VID/2 by VOV VRD/2 by VOV. Just substitute this ISS

by beta n equal to VOV square back into same expressions and you get these two equations. No, for that I have got the relationship between VOV XS body which is a DC excess voltage, okay.

We are not looking for, that is what I keep, I am keep telling you do not confuse between ACs and DCs. This is a DC current, I am talking about ISS is a DC current, is that, is the AC power. So do not confuse every now and then, okay. So if I now say why this conditions were, again we say earlier this VID 0 but even when VID/2 is VOV IDS1 is IDS2 is ISS/2 that means even if VID=VOV under this equation is 1.

You have a relationship with IDS1. That means again DC currents will flow, okay? Now, this essentially what I did in case VID/2 is much smaller than VOV that is capital Vgs-VT. Please remember, capital VGS-VT is the DC value, is that clear? If VID which is your AC signal is much smaller than VOV then you can expand that expression and ISS/2 ISS/VOV x VID, IDS2 is this. Since this content AC+DC, small AC current is proportional to VID is that point clear.

So under what condition linearity was held for AC, that the small signal VID must be much smaller than capital VGS-VT is that point clear? The day 1, I started with you an expression this, is the condition as long as you are in a DX range linearity is held is that correct? If you increase it because the curve is nonlinear, one cannot guarantee that these expressions can be used, but the condition is if you have a DX variation which is VID is a small AC signal.

Which is much smaller than the DC value then we say the AC currents are proportional to the different signal. So, whenever you bias by ISS, says that at half the currents flow that is, M1 M2 are identical, RDs are identical biases will be same at that condition, I these small AC currents will be proportional to different signal. This is what, so condition under which this was true.

When VRD is much smaller than the DC difference, is that clear? This issue is very important again, why VIDs are not very large because even with the last signal be gone, the conditions can only be linearized when we say VIDs are much smaller than VOVs. That means the AC signals are much smaller than DC values at which you are biasing, is that clear? This part we did in bipolar earlier and your mass earlier, small signal, small signal.

Where we say small signal is a condition in which linearity is maintained. Why we are looking linearity? Because for an amplifier, common, any common source emit any kind of amplifier, what is the thing we always say? Gain is constant that is GMA is constant and to do this we must have linearity, is that clear? To make it linear, condition must be met, is that clear to you?

So this is not really the solving part or this is not that we need to do this, this is just to prove my point, that you cannot have large signals with linear zones, is that clear? As the first slide shows, if you swing a signal from here to here, you cannot say they are linear, GM, the slope is varying all through, okay. Slope is varying all through.

So, in such cases outputs will be proportionately nonlinear terms will appear and whatever term you wish you can pick up from them but essentially no linearity can be guaranteed, is that clear? This issue is what makes interesting all AC analysis away from the DC analysis. Yes, see the total ACs currents are much smaller compared to DC current, that is what I am keep on telling time telling, that variation there is a small enough to neglect.

If the net current will be only the DC current is that clear to you because the average value, the way it is, 1+1- average at 0 at net current at any given average time is only ISS is that correct this is the way it is calculated. Instantaneous current yes ISS+I but average current is always ISS. This is the net current AC+ DC, subtract DC currents is the small AC current. AC current is proportional to AC different signal.

Which means linearity is guaranteed for this region and to move this you are meeting that the AC signal difference must be much smaller than the DC difference voltage is that condition clear essential it is really small so essentially saying VGA should be much larger than the input signals is that correct Vgs, which is biasing the transistor capital.

Vgs should be much larger than the signal which you are actually amplifying is that yeah that is my amplifiers are small signal amplifiers is that clear they are called small signal amplifiers yes

yeah really will matter where it will shift the idea is that in this region, where VGs - VT is holding the linearity is holding that is how we started with this assumption.

If that that the car goes away essentially what you are saying is true but every time very high fixture around that i can assume linearity is that that but if that signal expands then i am not sure whether it is linear or not any point on that along that small signal they always look as if linearity hood even if it is nonlinear as far as the total curve is concerned a may disappoint is that clear and when we are in saturation any point as long as this value is higher than the signal.

You are using linearity and region is holding for you obviously the day when we started out on this residence at you is that clear okay surrenders and i keep saying you is not that we are not interested in wire signal amplifier some other amplifiers later we may see if time permitting they are called large signal amplifiers.

They may operate in Class V or Class C across a be operations, but today we are only looking for classy operations so we want to now do a small signal analysis of a differential amplifier a typical define as we already have discussed has to and transistor m1 m2 whose sources are connected and they are given a surge current of Isis okay right now I am assuming all these are equal but in reality this is not a compulsory condition.

They can be RD1 and order as well but for the simplicity I am assuming that low voltages on both sides are equal please remember this is not a compulsory condition but much easier to sell you can solve without that and you will get nothing great will happen even if they are separated now here is the method I gave you two methods to solve okay.

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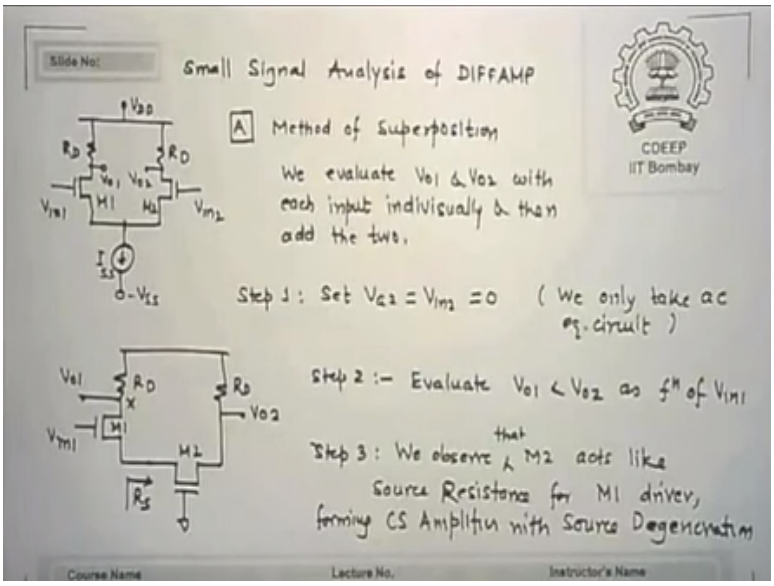

The first method is called methyl or superposition so there are certain things in which please look at the outputs are based to our VA1 and VO2 please look at it this is Vin1 and being two other inputs be a1 and VAP are the outputs at the two drains of M1 and M tools okay, now we will shake the method of superposition.

What does it say I shall wait eleven exists are going to 0 and get VO1 way to value with reference to input of V in one okay then so remember when address and so it came to exist then what is the a1 do add the truth is that correct this is called method of superposition so we start with this condition we are our little given new steps said VG to V X to 0 this is the first superposition I say one input signal is reduced to 0.

So we only take AC equivalent circuit DC pod right now you forget Isis we just ground later now if we shall meet again equivalent circuit and we say this terminal is grounded please remember this circuit is now shown here this is not dead okay this is an AC circuit no DC values are shown there this is named and this is your BA this is your view one that is called this point VX and V R because many bits called exp are so I thought maybe if you read per se any bit which has a node x and y written here.

You may as well use this I am not sure which boot but maybe one of the book because we normally use VXVY so I thought maybe you might have okay so this is your M1 this MP

transistor please remember from here this is DC so we go here and this VM2 is grounded is that point clear M2 gate is grounded M2 gate is grounded is that clear M2 get is grounded going to 0 ok then you are our D and this is your view is that ok.

You know a DC part this circuit will show you this is grounded this is just to show you how it can be slightly tilted nothing great please remember if there is no DC value there is no parents anywhere is that correct is that point clear DC is under there either by saying there is nothing can happen ok but I said I am only looking for AC equivalent.

So, I am removing DC power for solving ok now I can see from very interestingly I want to find VI 1 and VI do with reference to input of A+1 this is what my step two which is but by I am looking for that means I want be able in terms in terms of in 1 so the next step we observe that if you see carefully you see under this amplifier first all D and one input VN one what NP is doing for it where M2 is connected to em once at the source of M1.

So, essentially if there is an equivalent resistor of M to see in here whole it at like either source resistance degeneration of common source amplifier with so degenerated is that clear so I will then say ok why not I evaluate equivalent resistance here okay for M2 and then say okay our one amplifier with source degeneration okay.

This is the trick I use is that point here this em--to ha is seeing some resistance for this n1 okay I want to know how much is that resistance which I will call source resistance of and 1 and if I know that then I say okay with the covenant source amplifier degenerated a plugin allows correctly yes RS equivalent LI is the gain of a common source amplifier.

This shows degeneration is that correct or essentially GM Rd upon 1+GM are else is the gate for these amplifiers is that yes I will just calculate these things this is not given in so Brad this is mine so one thing that will be exactly there how do I cal cannot this resistance this is a method which I will do to turn it on you but I repeat this time once and next time I will never use it I show you right now.

How to evaluate the source resistance seen by a man okay yeah, I because I am posting as source to that instead of this I will use already to there okay just see my equivalent circuit and you will find this one, no I am not saying it is a AC grounded the reason why I am telling that there is a voltage here right now, which I do not know how much is that because of signal I am getting a signal voltage here.

There is an AC signal going on there that cannot be ground there is a current flow there is a resistance R out so there is a drop going on so I cannot call it ground there okay then this is a DC current so what path infinite resistance is that clear so you have point of view even if it is taken it does not hurt no current in that path on ok please look at it is for my employ on doing this is essential and being for EM to the dirt ass is grounded they look at them toe with dead grounded common date okay.

Let us say between gate and show there is a potential V1 between gate and source there is a potential V1 shown like this corresponding to the output of that will be at the dance then suicidegm2V1 GLVV1 shunting R0 this is the equivalent of a transistor is that okay this is the economy better to answer you may raise younger women be okay.

As you and follow me from the drone of that is an enclave the resistance all day is not connected to the source, but to the ground is that correct is AC ground at the VDD okay so this is the wrong at the VDD please remember always is not connected here all day is connected to thee from the upper side to the ground all 0 is between drain and source but alder is not between drain and source because source is not grounded is that clear.

So, if you now say I apply a potential VX at the source ok and say Rx is the current which is entering here what is VX how do I find out resistances I apply a voltage source ok and find what is the current flowing or V so V X bar X is the resistance seen at this terminal is that clear so I apply VX RX and the met current out of this should be same as violets because there is only this is there the new please remember loop is completed through this path.

That is why it was grounded is that clear is that clear since is named and this is open circuit so no current gain go in this side only column can go through this and formula comes out at our X and flows so out my this loop equation always is this drop+ always minus this current Apple iOS is this current minus this current GM+ G and B times VX.

Now only thing I have to understand VX from this terminal of this terminal is ground, please look at it this terminal and this terminal is ground, so between these two terminals what is v1 value minus VX is that clear this is again what I say U is this loop is now connected this v1 is nothing but minus VX so VX-VV1 and therefore, the current through eyes this is always rd x IX-GM+ GM v VX x R0.

Essentially, what I am saying current through R0 is RX+ these two currents times V1, so this is that current through R0 I repeat as I shown you this current is through our 0+ drop across this+ drop across this is your VX please look at that this voltage is dragged across this+ drop across this rather 12 this is our X already okay.

So this is oh it is already dropped across our 0 the current through R 0 R 0 is rx- these 2 currents GM+ G and D times V1 which is like this into VX substitute that here and solve for this expression so VX by Rx is all D+ R0 just solve this how much is the value I suggested you this error should come is this our source of m1 this makes from VX/RX will get you all D+ R 0 upon 1+gm2+G and BR0.

This equation say VX by RX k VAR ba Jana VSA okay so all equations so VX/RX will be equal to all devours you know 1+gm+GNB x R0 is that okay double this value this is the source resistance as seen more mom is that okay this is the source resistance as seen by M1, so if I get my our source for MMM.

So, as I like expression modified work a bit later it is colossal EC equation minute I will do+ R0 upon gm2+GNP+1 upon gm2+gm be yeah same expression through a split scope nominee is how much tell you how many of our how much typical values of all these will be I said you

many days 10k to 40k okay not more how much will be a 0 typically 100k to tens of mega ohms depending on lambda an idea okay.

So, typically I will do there are 0s are very small rd/r0 that very small, so this first term is unit any small is that correct I will be by r0 is small and as compared to gm to and D so we saw this term and neglected so they say GM to and that is a GND is also very small compared to gm2 then it is source is only 1 upon gm to the audio life flank job you will see a tandem do it and from the.

So, said you want to have impedance of that it is nothing but 1 upon gm the resistance seen by a common gate transistors the Lebanon is only 1 upon gm is that clear that Phil are they are lit again but general value will be added will be much smaller than R0 & GM Bs will be smaller than gm so we say it is nothing but 1 upon gn2 this is your circuit.

Now, I am looking only for transistor M2 is that correct this transistor I am looking for equivalent up so this circuit will remember for this resistance EMOS coming from here is that correct so if you read that then my expression is this is the debt, which is grounded for okay.

This is my source where I am applying this voltage VX okay corresponding the time instead of in allfm2V1 and gmDV1 as the current sources at the drain side denser side shunted by R0 and this alder is going to the ground through VDD okay and then I will calculate solve the equations cache a flower nothing great in that and get the value of already by also gm there is Forex and that is the value.

Which I am interested in just for delta Vgm is the value of trans conductance appearing because of the substrate virus okay why because of this substrate bias is that clear gm they may be present it brother substrate bias Jimmy may not represent if there is no substrate bias in general rated it.

If there is no substrate bias that is between the bulk and the source if there is a bias reverse bias then there is a additional depletion charge appearing because of that that will change VT s and

their corresponding value changes gm is that correct okay in our case gate was grounded okay and deposit that through the blame it was getting grounded finally okay.

So because of that that was shown you can use videos as the value and which will come b1 latter as the term will because this value is nothing but the value which you are looking, which is Vgs okay so I have this view so is that okay please remember the equivalent circuit of my default on the left side with VN1 is now I will be with the source resistance of 1 upon gm2 if I do not get no I will do.

Now 1 upon gm1+1 upon G until ascension it is - G Omega upon 1+gm1 RS which can be also written like this okay now what is the one super positions are ethnic I everyday Nicola Winacott Peron I also need to calculate they are too now you can say that empty start looking the circuit again anything major transistor and one this cable input high output has remember the term.

I am talking the NP transistor Moss as if it is driven by a source follower of m1 I repeat now you can say that m2 is driven by m1 as source follow it and how are you check if not I will explain you like next time if that is so I must say I am to whose gate is grounded all do each other view and it is driven from MN side of a source resistance of LTV and a source will be left n means voltage source of ETV and that miss EM mental equivalent.

When I was so Swift nominal does it not equal and resistance ever broken a is the equivalent for this okay clearly you can say VT 1 is nothing but V in one because that is the input available to you and all T1 is nothing but 1 upon GM s also neglected so if I now found out the best VAP please do it again yourself.

I repeat this is as if the N1 is will presented by now equivalent of voltage shows the nemesis+ it is Thevenin resistance the seminal source for source follower will be same as input which is very involved and the resistance will be essentially 1 upon GM of that transistor remember family everyone will appear here but that other one is higher.

So we forget so we have been is as far as this is concerned GMP maybe you can call it are you - but I do not, you are one we are going to say like that yes other amplifier gain Nicola mean vo2 by V in one if I do some mischief correctly I would say this is also equal to 1 upon gm1+1 upon gm to the present RS/1 upon gm1.

This is 1 upon G and two arrays are much higher divided by G M Poirot everywhere please remember derived ah gm2RL2 on the denominator and collect the term smaller turns neglect Kia so this is already upon this so what is this gain at the second terminal but this has two input at M1V2 at reference to Vin1 all know how that we calculate VI1/VN1.

So the difference gave us how much but doing what do we call difference gain the VO2 VI1-VO2/Vin1Vin1 is the difference gain same currents are same voltage at this is+ minus of minus would be just the well of that please remember same value has come there for here with a minus sign okay so minus of minus twice what already upon this if you saw gn1=gn2=gm then this is nothing but –gm RD.

Now no common sense amplifier again get nothing - GM already so define game wicket noir GM early is that correct deform the game be same amplifier yet now at GM aldi but this is another what is the step right now is only using vane on so that means view Rankin is same equivalent Gareth ahead Giamatti - sign more - opposite of that can they say now same thing can be repeated for we in two identical situations okay.

So how much we can get for that VO/-VOM will be similar value okay and that the net gain will be how much subtract that over the 2gm-a-gmRD will be the gain of a difference amplifier can cannot Vo-/Va-va-va1-VO by the same technique for the other arm now okay go brown Goro walk away again I had currently it will become 2gm.

This is one method this is not the best method I will make the methyl up with the current Oh quicker corrector, you have to verify karma but otherwise it will give you very quick results but there are conditions to do this okay this method is called half circuit analysis please remember.

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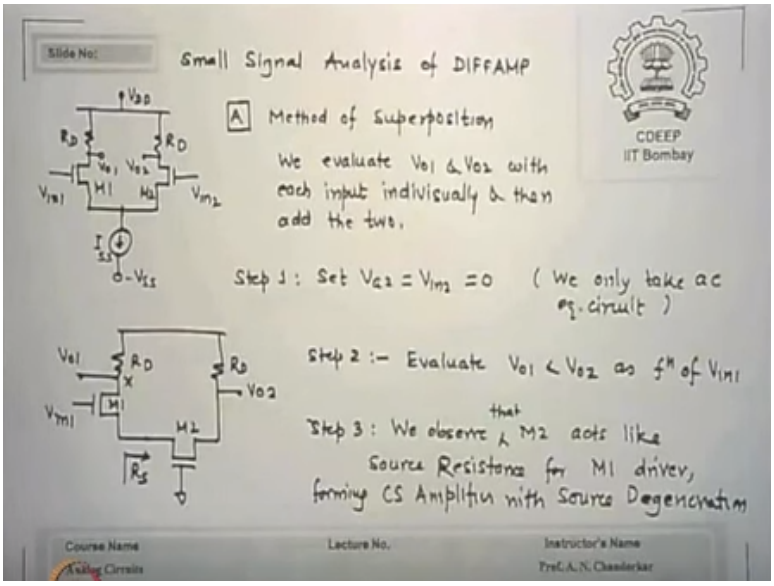

This is very few people get I am not sure just of the hair so them out are given in the appendices where you have a lemon here a typical circuit is shown here which is called symmetric circuit remember this is not necessarily given in citrus myth but may be given eyes I have table Isis d1 and D2 shown here for example this is my d1 this is my D okay.

Three terminal devices which receives inputs VN 1 and v2 has I ran out two currents and the net current is of course I1+ I2 is IT now this symmetric circuit has something condition we are now putting and that is very important let us say there is an equilibrium value of gain one called v-0 not output please remember I am not talking about put output is V0 is the equilibrium value M is value and real men change it is essentially.

What I am saying if this is your average value be 0 VN changes by either Delta V or by minus Delta V is that correct this Delta R old is a small that has to be understood then are they are the average value of v-0 at time six girls+ Delta V n at times it goes to B there are little values therefore it can take v-0 minus Delta V N or v-0+ Delta Vn as the two values it can pick up okay please remember.

The game is this condition in symmetric circuit is this this is what allows okay if that is a change in this by Delta V n the change in vain tools minus Delta n is that point clear if one input rises by some small value this certain input must go right this condition has to be made the invent less

going to go to is common more and Vin1-V x should be same if these difference and common mode signal have to remain same any change here must be opposite change in D.

This is called symmetric circuit is that point here change in V in one if it is+ chain went will be equivalent Li minus change in Raymond is negative then change in winter is positive they were always so that the sum total evaluates equal if you substitute them both will cancel and you will only get being 1- being two constant is that point clear view man - name - is always constant u increases decreases the difference will always get cancelled okay.

Then, that this lemma says if the circus still remains linear that is gm constant then the potential at this point P note point P best not change is that point clear the potential at this node P remains VP will solve this problem which you are asking I repeat if there is a three terminal device which receives signal which is if this increases this decreases.

This increases this the same amount then this voltage does not change okay this is what Lima is all about now we will show you the Lima proof equivalent me saying if there is no feminists equivalent resistance of d1 Saudis V t1 and our t1 is resistance this is more P for you which are the potential VP this is VT2 orT2 for the M2 side and let us say I is the current flowing from this side to this side we also assume RT1=RT2 for simplicity.

We can prove otherwise but just to show you here about BP if this voltage - drop across this and this voltage is IT 2 minus this minus V2 I sum this two equations to VP is VT1-VT2 if RT1 is equal to RT2 but we also know VT1-VT2 is V ID which is VID/2=VP now you can see from here what did I do VT1+Delta VT-VT2-Delta it a comma the first muon increases by Delta V T the other one decreases by Delta VT.

The difference between the two is VT1 changes from ET1+Delta BTV2 to changes V2 to Van del WT Delta VT Delta VT will VT1-VT2 will remain and okay so what is this point I am trying to say that the circuit is symmetric and this one is symmetric is not shown here and that is what essentially means unit area before you McConieh on for you see on your left on the right you have symmetric circuit is that here.

So I can grab that point I can say I have two circuits independent one and so when I am this side and each source other policy is grounded as if then I can solve game for this game for this and then I say okay if I get VXVY for this I can always get VX- VI by which is this is called half circuit analysis what is the condition I met I told you circuit should be symmetric okay.

Someday that is measure of this it should be mirror of this if that is so you can read the circuit and if you can build the circuit I can independently solve the two circuits okay that means if a is constant symmetry is only possible if VP is constant that is what I meant it better soap but this time the step please remember this is Vgs1 now condition is please remember the first case Vgs1 what is Vgs2 will be best for symmetry - Vgs1 that is a condition you must meet ok.

If better so VX/Vgs1 is minus gm1Rd parallel Ro 1 P1/-Vgs1 is -GN2 Rd parallel Ro 2 J on already ok I always parallel realities for R1 ro2 so we are smallness V bar upon 2Vgs1 is equal to minus R gm NRD + sum of the two while using this to both side can you think it is cut the annual ni if they are equal then that 2 will appear to gm I will do arrow will appear.

So, I want to cancel from there okay this tricks so if I saw G m1 is equal to G m2 is equal to GM RA1 equal to other two and are these are same then this become 2gmRd parallel Ro 2 2 cancels so minus GM Ro parallel RB which is VX minus v upon 2 vgs1 ok I want to say which is nothing but VX-V is Vgs1-Vgs2 which is nothing but please remember to Vgs1 can be written as Vgs1-Vgs2 because Vgs2 is -Vgs1.

So to Vgs is that clear how did I get these are equal because I say Vgs1 is - Vgs - okay so I out Vgs1 + Vgs1 and the second we just wanna go out as - Vgs2 so it is Vgs1 mine but this is nothing but your different signal is that correct this is nothing with a difference voltage VX-VY is the –gm (r0 parallel RO).

So this is the gain of a define how much is that gain minus gm times are they parallel or do any fathers are larger than it is minus GM hardy when you go back it if I have common is that correct this is called half circuit analysis similar thing we can do for now the question is which is many

people ask me so I normally show you some the symmetry in here you have example because then you will appreciate what I said let us say where one is not equal to V into that by minus sign or whatever it is ok.

So here is the condition if you say their name is not equal to V into as such what you thought earlier I cannot know interesting game this V+1 is broken into 2 voltage sources wave number 2 and wave 1/2+ minus+ minus series connected a the a diamond will carry in one here then happen but who are the sources immunity but my half of opposite polarity+ and minus is that clear that mean Isis.

When there is no source but I will still predict+ 1/2 and -V x / 2 same thing I play in this side there are you mental+ more miscue half of is that clear click sailor take out memorize anything about Corona so I square half here half tickle a bit opposite Rica is going to pour half of ketamine, Whitman do you think something is visible from here.

If you see this circuit how can I say willing to bow to class signal up, this we are about to say yeah then you say my rank at the Vin1 + being to bite okay it is cannot love you hurt these face associations are actually not changing anything that is given here is that punk layer just divide half of same series Monaca opposite Rocco.

They are same no but using this I can now make a fun of this circuit and I can solve independently now this is equal and machine there is a voltage source of EMF - feeling together EMM bless same argument is opposes side view into – Vin/2 and V1+Vin2 is coded as a game key lime in your differential JB - up look at the MM-PM2 with a minus sign being 1-Vin with A+ sign ok.

Since this ring 1+VN2 is common to both I connected them here and put it down it is uncanny on behalf is zombie then you Nancy this is vld bell - and this is - we already right - so define the requirement and now there you may occur the ocular this is Val D/2 this is – we are opening event or not equal I still made it somewhere every detail inputs, but what is the additional term appeared the common mode turn appear now okay common.

Let them appear now I want to say if you have drawn the circuit do not think too much there are just some on but we are saying as VN1 and V into no difference whatsoever so here you see please remember I can really say V1 is doing 1-V into and+ V, but not VN2 is this, so this is my different signal.

This is my common mode signal I gather certain I want different signal killer gave Nicolini all superposition that the common mode killers gave me cutting off your game call some carding is that method clear I have two signals difference mode signal power mode signal I will find the gain for both signals ball and add them by super positions okay if I do so I get V0 is VX-V rod which is V1-V2.

which is the difference signal is vein 1 minus V 2 then V 0 By Vi D is half GN parallel a weight upon recovery expression and if GM 1 is GM 2 equal to GM over 1 Ro 2 VA by the ADIZ GM Rd parallel R 0 which is my difference gain is that correct which is my difference game if the source is ideal the current source is ideal what is the common man says actually an unmanned no signals are same at both ends is that correct.

So, row 1 will be equal to VO2 so difference of U and V 2 will be 0 so that is a cm common mode gain 0 because VO1-VB will be always 0 if VN1=V x is that clear if the any types are same and the transistor is M I mean circuit is symmetry both outputs will be same that means if outputs are seven then difference is 0, so SEM is 0 so what is the game finally.

What you are using when the condition was not made - GM already so it does not compare surrogate they should be that even if they are not equal kinds they can remain equal kinds whether that essentially means in cash SEM is not 0 then the net gain may be not be same is that clear in this condition we are showing that the sources ideal the resistance across current source is infinite okay is that clear.

DC current is flowing that ACH 0 alpha is infinite if not then there will be some potential will appear there and that will modify then the ACM may be positive and then you will have to

actually get the gain of a Vin DN+CM as well is that correct difference mode signals whether equal are not still can be same gm Rd but for now I will do what is the term which will in case when it is non-ideal case what is the term.

We are looking for I want to know what is the ACM value with reference to ADM how much it is whether ACM is 0 then I would say the ratio of a DM by ACM is infinite okay this is called common mode rejection ratio ideally common mode rejection ratio is infinite okay what does that means at no common signal will be transfer only different signal will be amplified is that clear.

However in reality SM is finite the CMRR will be not infinite but maybe 10 to power 3, 4 or something 80 DB, 100 DB or and 120 degrees currents okay, now we want to find if a cm exists how much is the real value now if the current source always is not ideal what does that mean Montague means what is the color audio current souls the shunting resistance is not infinite but finite okay non-ideal means our SS across the surface is not infinite okay.

I will check around source with a voltage output impedance is infinite okay, but it is not true in that case now I look at for the common mode what is happening we LCM which is equal to V in 1=V into due to symmetry VXVY is V ay 1-VO.

So here is - we have Y1 - view - please look at it the way are now going use voltage law same slow connect you say no VX=VI so I connect same potential inner half asymmetry a VX is same as V by symmetric circuit head VX is dy signals are same symmetry outputs are same we difference may be 0 but difference is 0 by shorting I am making VX-VY is 0 is that clear difference between VX and V Y is 0.

So I shot them ok all common signal to both HV Vin cm and they were an RSS now if you look at this circuit carefully these two transistors how do they look to you they look and a circuit one transistor is this the other transistor is this both are getting same input drains are connected source are connected care is a built on the 30th parallel may have sorry equivalent but if this is say m 1 and m 2 it is K equivalent register on the stove over M1+M2.

How is rewrite current for each that says linear or any beat on to beat on into w well everything else is common so if I add the current passing through this+ current passing through this what is the total net net current Weiss which is equivalent is saying the transistor equivalent current is twice the width of that one transistor is that point clear.

If you are a transistor approve of you instead of 1W this is 1W this is1W each is carrying equal currents together we may say you have one transfer, which carries which adds to that positive it is that correct so we say an eminent and assuring MVT are same everything else is same betas are same then we said so neat twice two bits okay.

So the transistor has twice the width is that clear this is called equivalent transistor, what is it called equivalent transistors in parallel two transistors are in parallel there bit sums okay so this is essentially this circuit then reduces to okay then I will show you this I will do that also palette yes although I wish all day.

So equivalent resistances are about this is RSS, which is cannon this is which is equivalent at twice the rate of call MNM - transistor okay now is cause I-J method is key trick ski as I have looked a periodic and then improving internal we say bits are equal WM Club ablative W all says by-is Isis we are gm= this gm eminent is this J1 is gm- is this, so the gma, you wanted to prove I wanted to search.

So, I showed you its prevalence 12 expression for giants please remember these genes have been calculated on what basis for each transistor for the current is how long DC current all says bow to please remember this is never to be missed that only makes symmetry otherwise does not make any symmetry okay shop J dr. new transistor with how much twice that of individual assuming others are all values are equal okay.

I just showed you substitute there and you get to Jim is that is that point here okay so why am I a common source amplifier which shows disseminated by one what resistance RSS you were a low-energy is not all did I to source resistance RS s gm is now 2gm okay, so then via VNC

MMM common mode gain is –gm already upon 1+2gm RSS please remember to gm we are on a applies to GM RSS which is equal to essentially if you say gm/1 is this is larger than 1gm.gm cancels.

So, it is sorry already by 2RSS may be cm is it not finite because RSS is not infinite so all do about when I assess is certainly not 0 or not 0, but some finite value so the common mode gain is now the ratio of the load resistance okay oh sorry I also made a mistake what is the mistake I made how is aria yeah like to hearing to get this correct thank you.

Thank you very much I need I had some wrong thing okay so I should write like this okay if I want to improve a term which is called CMR add the UDN/ABCM which is the ratio of difference game to the common mode gain and since it is finite and we want to keep as high as possible what is the condition I should meet all this should be small all RSS should be high as much as possible.

So, a check current shows up here currently with no common mode rejection ratio higher yes the not a difference output we are looking we are looking only for the common mode outputs but that is what is it it will get rejected at then but not funny that is what I am trying to say each hiss now vo one which is not which has a finite value in fact that is what we are saying otherwise we would say a common mode would always get rejected independently.

Now, we say all of it is not rejected very small but they may be account or outputs along with what we are saying difference can be a one+ two smoke which common is that point clear is that funny which is not neglected now perfect difference is still same is that that is alien DNA still independent of what cm is doing it is that correct, but I have never be said RSS is infinite say where I want to say we assume is 0.

We say it mean d0 yes this is division only we calculated equivalently is that clear that is what we say ABCM is not 0 now which means there is a finite common mode rejection ratio which eyes are at 100 DB to 125 how much is 7 for one you measured so what why Allah tells you

monitor for do not input resistance output resistance and CMRR of course there are a few new appears are all another but they are little more higher order anyway.

We will know them open in defining what did I say start the day one depend with the first a wave photon so we are now trying to see once you understand the is your output hello carbon damages then/co is that correct and the brain stays I put it a buffer and then we call it as operational amplifiers.

So the first input stage of FM is a difference amplifier and that is what we first looked into okay is that okay before you quit there are they know do this analysis next time but this is the other interesting things in duty circuits a difference amplifier may be melamine have a resistive loads what is the reason why resistances are not used in integrated circuits here we are so it resistor if you achieve 40 Giga resistance may take 2MM/1MM area.

So no one is going to put in a no power charger this lever back A, so we will always use this transistors as resistors so here is the three kinds of nodes which we use in the case of difference amplifier and where for op amps you got the normal differences put the caramel and five what is m5 is giving an hour giving AVgg voltage, which is some voltage I just what is this M5 connect this will give me current source.

So I can fix the current source by adjusting Vgg is that correct I can fix the current source by adjusting Vgg, but there are people understand n3 and n4 where I do transistors for m1 m2 - shown here m3 and m4 whose these are all n channels as of now but they turn with each other some connection will be modified.

When we say they are in channel devices the gates are common and gates are connected to the drain VDD what is the when I say gate of it in channel transistor is connected to the drain what are the status of that transistor permanently saturated because VGSH VG, sorry Vgd and VDS is same okay therefore Vgs-VT will be almost smaller than videos come with me that kind of Vgs please remember this is my videos this is my videos.

So, same potential is exist across this so vgs -VT will be guarantee clean less than VDS is that okay therefore m3 m4 will be always in saturation so what is the typical value of such resistors will be transistor in saturation resistance either they are common they are such an otter already Vs are there is simplified at a very large.

It is a large resistor of core value can be adjusted by what the current, which I will pass and length w oils are used for M3M okay I can change the resistance values okay this is called manual active mode would give me somewhere p-channel country Claude Rains government instead of M channel.

Then, the definition should have gone there like this they should go to the shore side is that correct they should go to the I saw a level up of course for a third I would connect now that connection is can recall that this is yet essential is diode connection okay this is a factor this is essentially is a buyout connection this is drain this is so this is good for a p-channel okay.

This is called normal at T nodes I can all such port instead of directly going to VDD which is Vgg1 and if it is Vgg1 and pulsed a telepathic oh if I put a Vgg and M5x like what current source so M3 & 4 acts like current source okay that is like current source so this is kind of current source nodes as soon as I put up Vgg, there and I have just that value.

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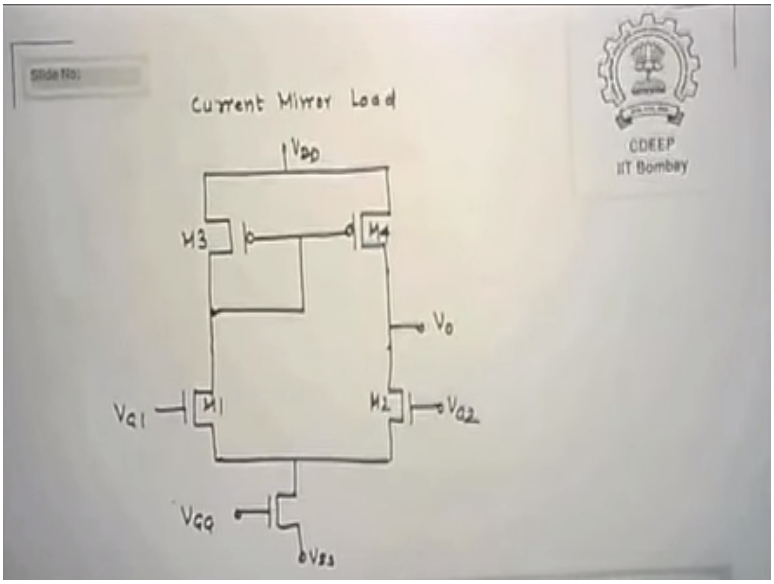

I can fix the current in n 3 and n 4 okay so I will say it is current source this rather doubt going to another column source over this is called current mirror load this is the connection which all analog opens will use this is the point of low lows all opens use is this connection clear to you the gate is connected to only one side of the drain where each other can do you recollect mirrors let us our mirror what did you do in mirror.

If you WI a partial reference a the r0 is our reference depends of course if the W of all are there till you multiply it this is Karen Miller is that correct this calendar is mirrored to this as soon as I made this connection get going to the drain of this side I am making it current mirrors now okay currents in this arm and current in this arm are me right now is that correct current in this arm is same as current in this arm the world they are also an output resistance.

So, the output resistance of mirror is their equivalent load for M3 M1 and M2 is that clear this is the third kind of load which I may use an almost 90 percent of opium loads are current mirror loads is that correct and the only disadvantage of this is it only gives single embed outputs is that correct by the other other terminal even a way connected to the gate okay.

So, it gives you only single ended outputs okay so tell me it is a different with single embed outputs why did I do this what did I tell you in open what should be the next stage there will be a gain stage how many inputs it will expect from you one input is that correct so I created a one single ended output out of this the next stage is going to be a single MN amplifier here then stage I need an input now okay.

So, I will created an input out of this okay this is a typical design input I a difficult different stage which is the first stage of an open yeah a disadvantage is many at times I am really looking for difference gains in this there is no difference game is that correct okay so maybe I will do a figure, which may be interesting to show you the Minerva that will open a scribbler figure mm I did not get that input item J.

There is no possibility yeah be awkward if I do sell a possibility or severe is that clear 2 inputs to outputs are we just as the colony because except the ornament and may difference outputs are

required you would prefer this is that correct because in this the gains may not be very high in this the gains are typically of the order of 10 to power 4 to 10 to power 5 an open-loop gain.

If the order of the order of 10 to power 4A 10 to power 5 80 DB 200 DB gain is available to you open-ended why open-ended there is no feedback open-loop a real circuit resolution MLA at input ha ding a disco ground this is under feedback now so we say V0-R2/R1 times V, now it is independent of what they have done itself and this is something interesting I repeat I will be come back to this circuit by doing this circuit.

The output is our gain is independent of their transistor our parameters, so filament alone of you can circuit may come together is that ok now will meet again you.