CMOS Analog VLSI Design
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Lecture – 07
Basics of MOS Amplifier (Part-3)

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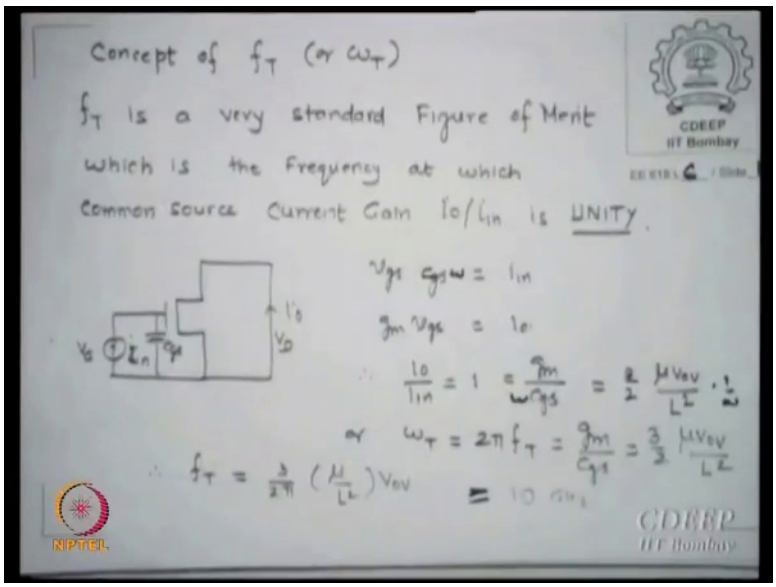

We were looking other day about the maximum frequency at which a amplifier or analog circuit can function and we gave a concept of what we call as the figure of merit frequency which is essentially called f T. And we did derive let me showed you that typical f T is g m by C gs related to g m by C gs and if I put the values leaves. So, concept of a figure of merit frequency which is call f T, and we defined it by saying that it is equal to g m by C gs, the C gs term essentially coming from input capacitance.

If there is any additional capacitance, it will be g m by c n actually, but right now I am only using C gs. So, for a device it is only that capacitance which I have written, but for external circuit may have some more capacitance is there. And if I write this transistor f T which is 3 by 2 pi mu by L square V ov typically this may ah be much higher than gigahertz one-tens of gigahertz typically it may be as high as 100 gigahertz. And we always say that the concept of the maximum frequency at which a circuit can function relatively correctly or you can say correctly means our modeling which we did is based on the lump models of the device is valid at that point.

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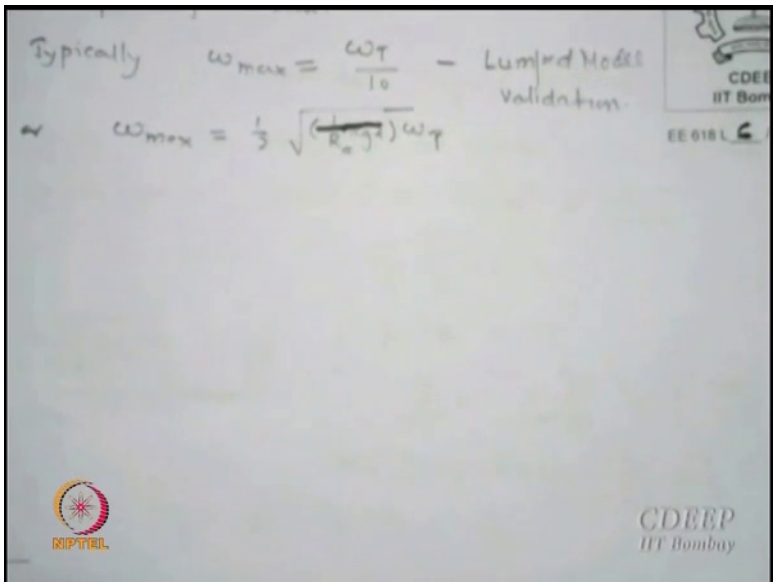

We discussed last time the typical frequency could be tenth of the f T. Now, the other method I suggested that you can take a geometric mean at the pole frequency and their W T and it may come close to the value of tenth. So, it is not that the either one it is wrong or right maybe little more accurate than this, but 10 is good enough approximations. We also discussed that day apart for this is what we did I am just trying to recapitulate in the f T valuations we always see that we used a model which is called large signal or large channel model or long channel model for MOSFETs.

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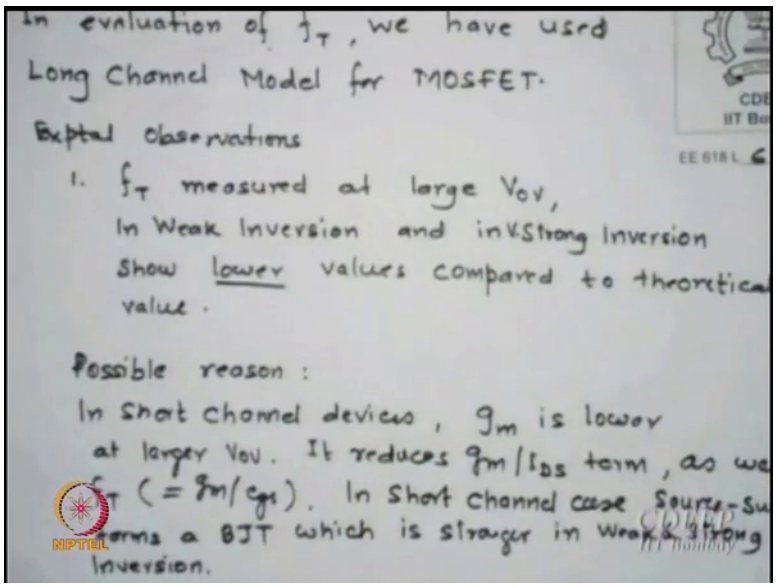

And there will say that larger the V ov as the function shows f T will be larger; however, this was assumption that device is always in reasonable inversion, but if it is a very, very strong inversion or a very weak inversion, these assumptions are not valid, and therefore, f T relationship with V ov is suspect. In fact, the problem starts now that whenever you actually go down to short channel devices; the definition of short channel device also varies from people to people and device people have some other way of telling.

But for you can take from me a short channel device is called short channel I mean MOSFET devices in short channel, if the channel length is of the order that the depletion layer widths. If it is in that order then we say you have a short channel devices or if you are a technology minded person, typically similar scaling is done for all length and widths. So, one can say if the channel length is some way is similar numbers like the junction depth of the source and drain, then you are also in short channel.

So, this is a definition which is a arbitrary to some extent in major think which we will see in a short channel is and that actually changes the other parameters. There are many short channel effects, some other course you should learn about it, there n number of things which you can talk about. From the circuit point of view my worry is E y is now stronger and I am kept I am saying E x is too strong compared to E y which may not be now valid they may be comparable. So, both field may cross there will be effect from both sides.

So, there is this short channel word is only as I say the definition and take it in reality whatever the experimental they are chose that is the shorter. Typically one can say 0.35 micron or even 0.5 micron, device can be said to be in short channels. So, most of the analog circuits are now actually working on short channel devices, but may the digital technology going to 90, 45, 65, 45, 22 and 16 nanometers, you are really going into short and short and shorter channel devices, and the worry is will become even much more than what we actually saw at 0.25 for 0.18.

So, this fact that we are looked into a f T that in a short channel the relationship between f T as well as g m by I DS is it is suspect. So, one should not really go too strongly saying that V ov is a good parameter of design which we have been talking very you know casually address of that is the end of it. Once I know this I can do everything; but

in reality, this is not the best parameter of the design. So, we will come back to that part again.

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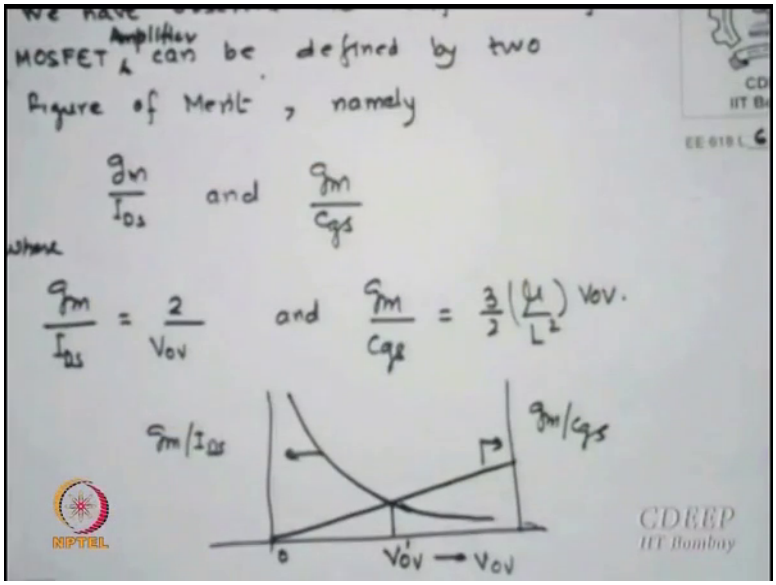

But here is some two figures which makes my point clear if you are the point, which I am now making it is interesting for a MOSFET amplifier, therefore two parameters decide the performance; one is g m by I DS, the other is g m by C gs. Now, if you that is the expression I wrote that is what point I am trying to prove again to you. If I plot g m by I DS against V ov and also plot g m by C gs against V ov to you said these are two figure of merits. So, I plot as a function of V ov. You can see the g m I DS is inversely proportion to V ov, so it actually show some more accurately does not follow linear it should be lit linear, but it is not mean that is what I am trying to say. It goes partially like a square function or under root functions. And if you look at the g m C gs term, yeah it does arrives roughly linearly with V ov.

Now, if want to maximize g m by I DS gives what, g m by I DS gives you performance of the power that decides the power. Now, if g m by I DS is one parameter of power as your spec then there is an issue here. If you want to have g m I DS an control and at the same time you want to higher bandwidths, so you want larger g m by C gs. Now, you have a problem larger g m C gs will have lower g m I DS, and larger g m I DS will have lower g m C gs that mean there is some way optimization is going or optimal value is where they cross probably.

So, this V ov dash is somewhere where both are reasonable now this is going to be the value in fact, so can you push this curve up, if we can buy someway then we say we have this V ov dash little better control; right now if this is very small than control itself is very small. However, this has to be understood that V ov is I effective varies we are really varying most of the performance of the circuit. So, this should not be treated as good a design. If you use even a third figure of merit which what I suggest sometimes if you multiply g m C gs into g m I DS and call it both you want optimize multiply it and call it third figure of merit.

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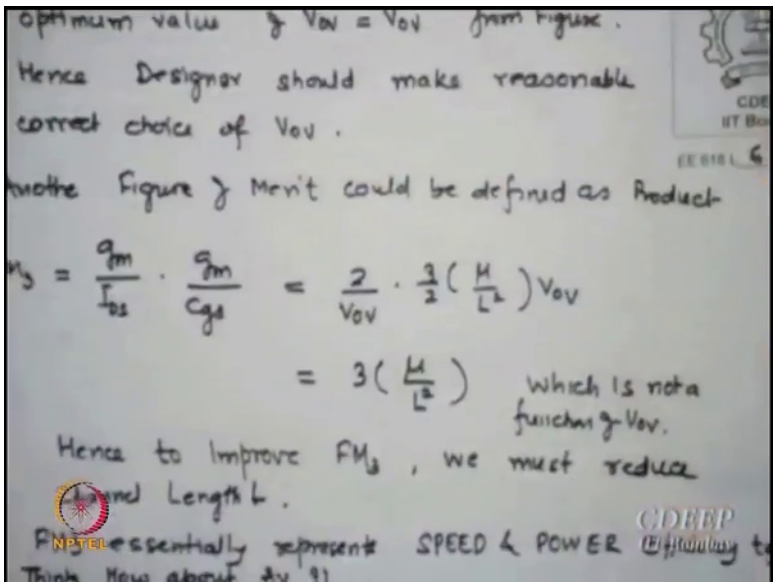

And if you see now if I substitute those expressions of both g m by I DS, and g m by C gs as 2 by V ov and this, it gives me an interesting expression we say 3 V by L square (Refer Time: 08:37) technology. Channel length is decided by technology nodes; however, that number you can change because I will need not work on this shortest channel device or longest channel device lengths, lengths can be in my control. Now, this essentially now I am trying to say that this figure of merit has nothing to do with the V ov.

So, choice of V ov we have now last because you suddenly thought that if both have to be optimized, then you need not worry too much about which is not true in fact, how much current I will push we will decide the gain. So, now the issue is that F M 3 may essentially represent power and speed, but it does not talk of gain. So, V ov as a

parameter which we have been in so far talking in all my analysis so far V GS minus V T is all that you may have to control is not the best stuff design parameters is that correct, and because of that I always suggest that this is not a fair deal.

So, let us see what we can do afterwards and this is an issue which I have thought as a designer you must keep in mind that V ov is not the best design. There is no great correct expression between V ov and g m I DS, g m C gs into V ov a same age; there is no relation bit strongly with any other parameters with V ov exact ones. So, this is like a fetch factor you are trying to fit somewhere and getting answers. So, what can be the other possible design spec or design parameter, and we will declare it the latter that which one should be actually used it possible.

So, this fact which I said you that this is last time I should I showed you this is from the last slide I should I showed you, but I just remember that this was not shown, so I thought you should remember that my V ov concentration is not really a great contribution. So, we will see modify latter that is that any other thing we can use as a parameter instead of V ov and that is why I am trying to show back this two slides which I. Is that ok, everyone?

Student: (Refer Time: 10:44)

Yeah, but length I can always double it triple it; I can do anything based on that. I can have point let us say nanometer technology is 65 nanometer, I can pull 130 nanometers also lengths. It is not that I cannot reduce then the technology note, I cannot pull it down to say for 65 nanometer I cannot have 45 nano actually 65 the channel length is not 65, some other day technology course this members are nothing to the channel lengths. 45 nanometer have actually 25 nanometer channel lengths, 25 nanometers actually 12 nanometer a channel lengths. So, this numbers are also not very true, but these are called roughly you can say these are channel lengths. So, you can always go below up to the minimal channel length available for you taken up, but you can double it triple it that member is in your hand is that ok.

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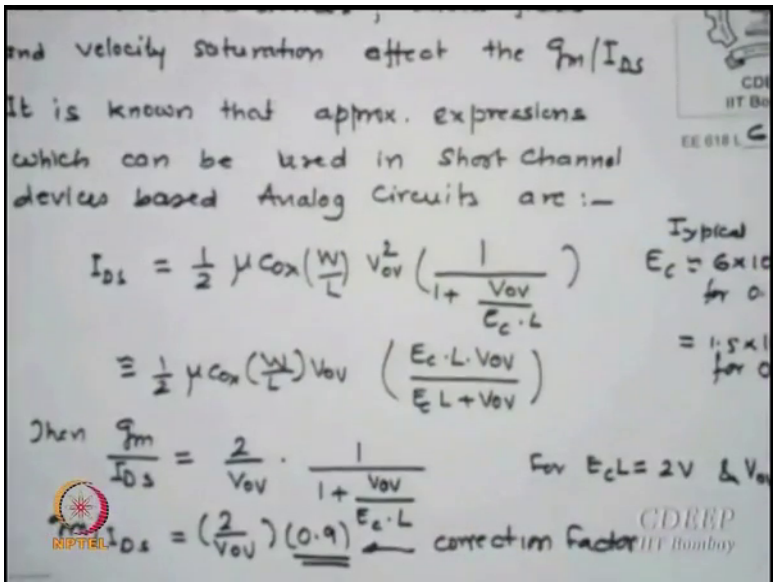

There are also issues in the short channel, which I did not say. So, I will I thought that today I will finish that part. In a short channel device, as I just now said the lateral fields and velocity satori effects both affect g m by I DS terms. It is known that approximation expression which we used earlier for long channel can be modified for a short channel analog circuit performances. I write this current slightly modified by an expression which is one upon V ov by E c L, where E c is actually called critical field, and it is different for different technology node. For example, for 0.25 it is 6 into 10 power 6 volt per centimeter; for 0.13, it is 1.5 to 10 to the power 6 volt per centimeter.

So, if you see this, can you see from here E c L into V ov E c L into V ov what does that show which kind of expression it is showing? If I substitute E c L here and I get this expression, what is it showing timer combination of two terms one upon E c L and one upon V ov. So, now, there is an addition V ov we are only looking for now there is a additional term in short channel has to be taken care which is E c by L, E c into L is that correct.

Now, this additional term will modify and if I have done some calculation for a gained value typically if E c L is 2 volt for a V ov of 200 millivolt, the g m by I DS becomes 0.9 of the 2 by V ov term. So, in a long channel, what you are used 2 by V ov. In a short channel, you may have to multiply it by 0.9 this is for one specific case for a given technology for given lengths, this E c has to be actually obtained and then used to find

how much this coefficient should be 0.85, 0.8, 0.9. And therefore, you can see now the g m I DS available at long channel is not available to use in short channel. Is that clear? So, these are the design issues which as a designer we should keep in mind.

Student: Sir, what is this E c?

E c is the critical field where mobility starts actually strongly dependent on the fields. Strong dependence though V is always function of E, but a stronger dependent when a we say is called critical fields.

Student: And then 0.25 node, 0.13 node.

Yeah for technology nodes. So, for 130 nano meters, this E c is 1.5 10 to the power that is what was a for a different technology node.

Student: Hm.

You will have to evaluate E c more accurately, E c into L. And that value you have to substitute there, so you find this constant factor we will change for different technology nodes is that.

Student: This term is always there (Refer Time: 14:53)

2.

Student: (Refer Time: 14:54) or is it.

No way this is true this is some extend till you go to very, very strong inversion or very weak inversion this expression is true. But the at least it has taken care of increase electric fields laterally, which earlier we are not looking. So, the additional field which we were talking about is now taken care through this term. V ov was done we are assuming only channel from the top, now you say there is a additional source of charge can come. So, this fact could be taken care in our analysis.

Please remember some of these expressions are more what should say analytical expression. What does that mean that I had derived under certain assumptions every time? So, not all assumptions are true in all times. So, in reality what should we do we will see what can be done. Then these are reasonable way of doing it, why I am saying

reasonable because at the end of the day, you will work on some CAD tool, which is like a spice for example.

So, where to start at least you know correct guesses can be given to the input files, but this at least gives you some idea physics what has happened there is that clear? Some physics has been understood that as you base there is an additional term may appear which will reduce g m I DS. And this is very relevant in calculate why g m by I DS decide power for example, and now you can see power may actually have gone down some or in some case gain may go down whichever we will look at it, we will see that part.

So, essentially unknowingly we actually thought that long channel expressions are good enough, but in 2012, I think that is not fair so I that is what I said few years ago I never showed these, but now I thought you should all know that in real life things are changing. And you must know more physics to bring closer to what can the experimental result show. However, I will tell you at then this when I finish my design here, I will show you how exactly we should do in fact.

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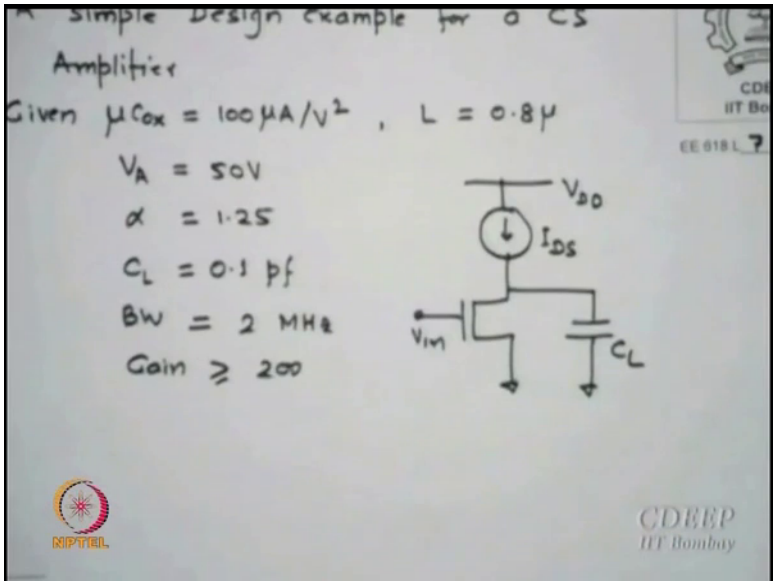

Now, I will actually give an example of a very simple amplifier, which many times we are doing, but some values may be now given. Since, our course have no formal tutorial as such I thought at least some problems I will solve, so that you will have a idea equivalent tutorial at least for 10 percent of my time. Let us say I have a simple MOS

amplifier which is biased by a I DS current source and the data given to me is the mu cox values 100 microamps these are all random numbers these are not specific in real life. So, these are some contrived numbers. Channel length is 0.8 microns, so this is quite good long channel approximation 0.8 is sufficiently long in channels. The early voltages is given to you is 50 volts, the technology fetch parameter alpha is 1.25, the load capacitance is essentially 0.1 puff, the bandwidth required for this amplifier is 2 megahertz, and I am expecting gain to be higher than 200 trivial, but important.

So, what are the specs I repeat the early voltage is 50 volt, channel length is 0.8, mu cox is hundred microamps for volt square, alpha is 1.25. If alpha is not specified what will you choose 1; if alpha is specified use that value if not given just use 1 or just do not use alpha any ware then essentially saying that. C l is 0.1 puff, bandwidth is 2 megahertz gain greater than or equal to 200, this is a spec given to us for a given technology node. And we want to find what can be find from there, what is the thing which have not been given to us and which is what we are designing the size of the transistor that is the design, length I know, but width. If I know my width, I get the design of transistor and therefore, I get the all this specs to be available for actually performance, so that is fine.

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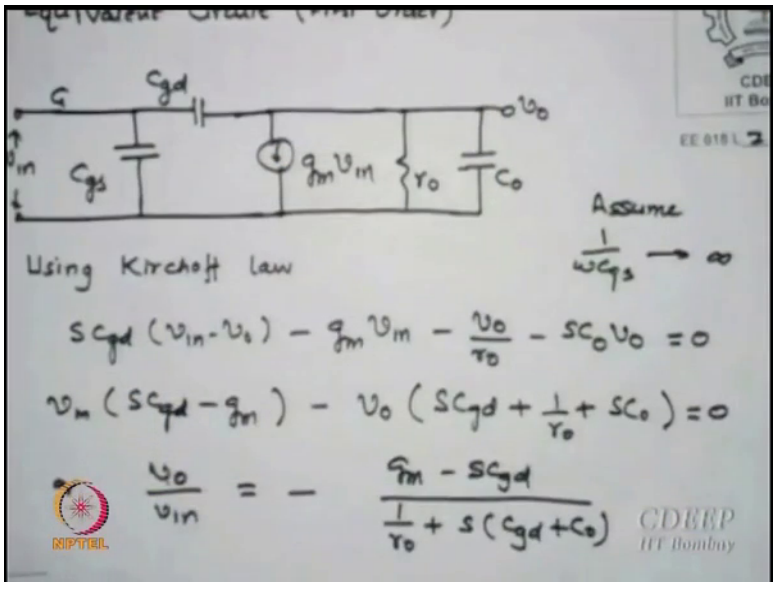

So, from thus simple amplifier, we can give its equivalent circuit there is a C gs as the capacitance and C gd. Right now since I have not specified anything on the C gs my assumption therefore is 1 upon omega C gs have at 2 megahertz is large enough to be

open circuited. So, I do not worried too much about if I am given them use that if I giving what is the value of C gs is use that right now because I want a simple solutions to show. So, I neglect because this frequency is higher.

So, I am not looking that it is much more than 2 megahertz it will be bandwidths. So, I am not looking for that value. This is a simple circuit perform this one can solve using Kirchhoff law. As I say I like this naval equations because spice all most cases the relationship by nave equations, but you can always use meshes. If you feel comfortable using mesh, you can do mesh analysis. If you feel comfortable with node analysis, you do node analysis, this is why I do node analysis simply because spice does it. So, you can also do it.

Student: Sir long channel is (Refer Time: 20:48)

I agree with I want to hold C gd, C gs I have removed, but C gd I want to show that there is a feedback what is the issue on that. Typically C gs is higher compared to C gd. So, C gd is a very we say series, so anything is series troubles you most, we will come that that sort of miller theorem we will talk about that is anything in series feedback is an issue. Anything across many a times it can be neglected for the omega 1, just may be large enough forget about it, is that clear to you? This is not true for actual you may substitute and figure out keep everyone nah there is nothing that you have to remove or not to remove. You saw a full circuit terms will automatically get canceled if they are smaller you can add one in ten million. So, what do add there, so that term you can keep, so there is nothing wrong to solve simple I slightly took some exemptions.

So, if I solve this I start from S C gd into V n minus V o minus g m V in minus V 0 by R 0 these are all currents at this node I am talking I am talking here minus V by R 0 minus S C 0 V 0 is 0. Then I collect the terms of V in and V 0. So, V in S C gd minus g m minus V 0 S C gd 1 upon R 0 plus S C 0 equal to 0. So, you get an expression of gain which is V 0 by V in which is minus g m minus S C gd 1 upon R 0 plus S C gd plus C 0 is that simple second year nothing more and nothing less. So, are we doing it, we want to solve using there we know we gave a gave a already W values. Now, I want to figure out if given this data what w I can get.

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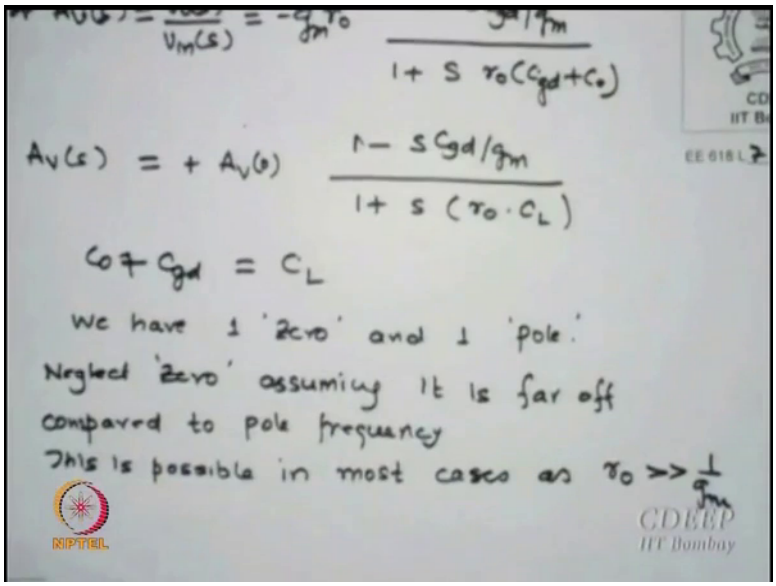

If you can now see for the final expression if I do this take g m R 0 out, what is g m R 0 minus g m R 0 is the dc gain, please remember in analog circuit the dc gain is not really dc input gain, it is a frequency independent gain is that word clear? It is called dc gain which means without frequency whatever is the value is called dc gain. In fact, there is essentially I am not saying any input signal of ac I am getting a dc output is not rate statement that, but it is called dc gain. DC gain means at frequency is close to zero whatever is the gain is called dc gain. It does not say input is dc, is that clear to you? So, please come and get to this. So, this is my dc gain into 1 minus S C gd upon this and I am this c now you can see C 0 per C gd is the total load capacitance at the output which is been given to us as how much 0.1 puff.

So, though C gd only could have been given C 0 only could have been given I just said that whatever this sum total this value is 0.1 puff. I am trying to reduce my calculations; in real life, you will have to use the actual values given to them at that point is that ok? This C 0 plus C L C gd I have to used away c I can say this is the value further solving purpose.

Now, assuming again to solve very simple case, I assume that the 0 S C gd by g m is given me 0 that zero frequency is far off away from the pole. So, I just now even do not bother of it maybe it is relevant in some values, but now I am saying the C gd what he was worried about it such that the at the 0 is some 100 megahertz or 50 megahertz. So, 2

megahertz is my bandwidth and my 0 is sitting at 100 megahertz by then the gain has gone down to some 200 d minus dv. So, I am damn caring about it ok.

So, I am not worried about then when it start rising by the time it will come to 0, it will be million years. So, I have done care if the 0 is far away and in design and that is the gain you will pay in design see to it that your 0 is far away from your any number of poles you are looking at. What is the advantage of that that because going to give you some plus phases and you are trying to adjust phase margins in actually amplifiers. This should not be the bothering point for you and that is once spec I use that the zero has to be at least ten times this and I use this value itself to calculate. So, zero is something which we do not want very much because zero gain is not file, so if that fact should occurred far away from us.

However, zero has an advantage what is advantage if the same position zero occurs at the pole then it will cancel. So, your gain will become flat anyway. So, zero is not that bad either, but right now let us see what is going to happen. So, this is possible in most cases as I say zero in this. This is possible most cases there is normally R 0s are much higher than g ms 1 upon g ms this value which I am saying this is a condition which is normally made. So, zero may come normally far away, but not necessarily because C g may decide where it will come. As I said this is a solution for the sake of design and these are not any specific technology rules.

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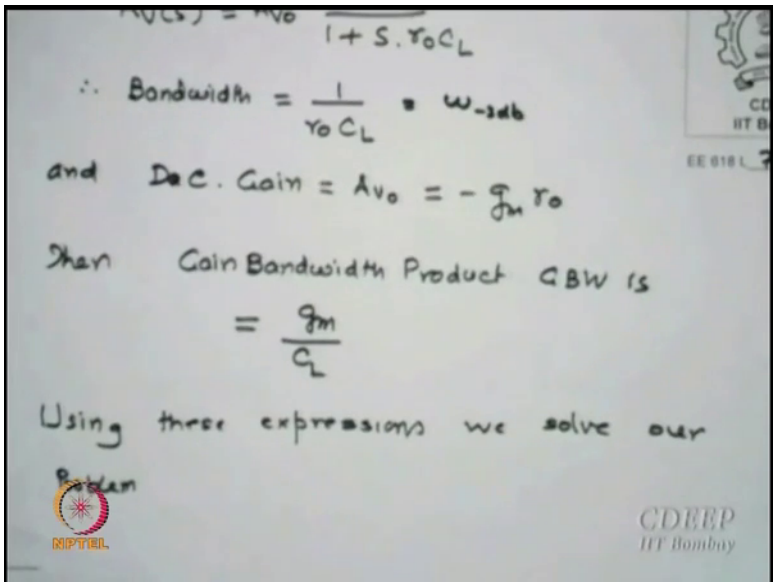

So, now I have some expression from this I have neglected zero. So, I got A Vs is A V 0 1 plus S r 0 C L. Now, what is the bandwidth from this expression 1 upon R 0 C L omega minus 3 dB as it is called if you wish the definition in bode diagram then this is one upon R 0 C L the dc gain is minus g m R 0 the gain bandwidth product is g m by C L. Now, these are the expressions which I can used in use in my design for evaluation of what the width, all that is width, my interest is in width.

Is that expression who wrote these are the expression I will use the bandwidth which is 1 upon R 0 C L the dc gain is minus g m R 0 and the bandwidth is gain bandwidth product is g m by C L. Now, using these expressions, we can now solve our problem what data I have given. I could have directly started on this, but I thought I will give you a expression first, and then show you where do I substitute, is that three expressions clear only three things I am talking about gain bandwidth and gain that is what it is.

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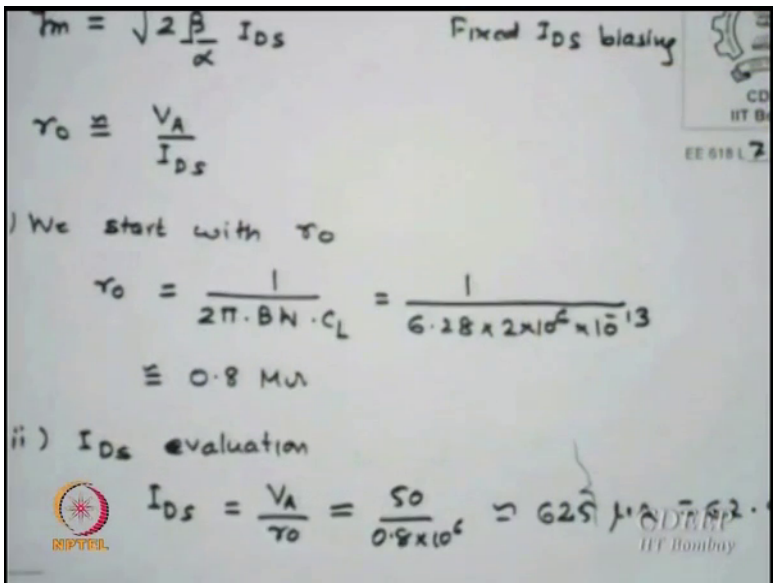

So, if I substitute noise is a constant current source as bias which expression I should use I am fixing I DS 2 beta I DS a under root of that is that see the chart in which I showed which one I am fixing correct, which the center one I am using. So, I am now using g m is that clear, that day I gave you table with for three fixing; in this case this is the minimum which I use in which I DS is getting fixed. So, g m is 2 upon 2 beta by alpha; if alpha is 1 you may not use it, but here I have given you. So, 2 beta by alpha I DS and we also know R 0 is early voltage divided by I DS.

So, these are additional expressions three first I said and these two more important expressions, I have to use in my design. Since, I have said the bandwidth is 1 upon R 0 C L what is the bandwidth 1 upon R 0 is the frequency which is 2 pi f is the angular frequency. So, actual frequency is 2 megahertz given to you. So, you say from that expression R 0 is 2 pi the bandwidth in to C L, I may bandwidth given to me is 2 megahertz and I am given the load capacitance of 0.1 puff. So, I substitute it everything here. So, I get a value of R 0. So, what is the value of R 0 I got, 0.8 mega ohms is that ok? This is two power bandwidth into nod that expression, we just wrote we are just substituting values now.

So, the first thing I figure it out that the output load form my case is 0.8 megahertz and then mega ohm coming from which parameter the bandwidth since we are given bandwidth I figure it out that it should have this much as R 0. Now, I want to evaluate I DS because I DS is going to decide g m. So, I must know my I DS, but I know I DS this I DS is nothing but early voltage by R 0 which is 50 by from where this expression is coming, the slope in terms this is the voltage. So, this is thus from the slope characteristics. So, I evaluate I DS equal to 62.5 microns as I said these numbers are not sine cosine, these are very arbitrarily chosen values. Please take it the real numbers may be very different it may be actually milliamps or tens, hundreds, eight hundred micro amps kind of things.

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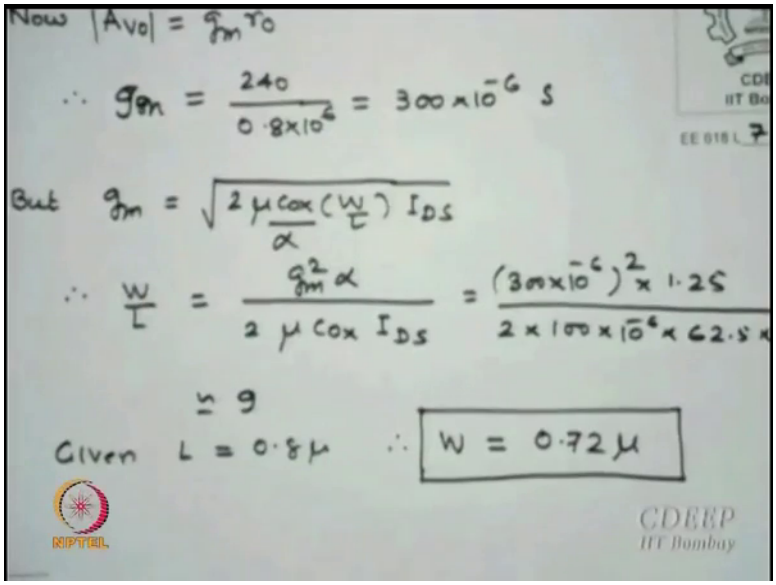

So, right now then go by this oh you said 60, 60 is some arbitrary number I also know my A V 0 which is g m R 0 as the magnitude, I just calculate g m which is gain divided by R 0. You have been told that ok, instead of 200 I will use higher you set. So, at this 240 only to divide by 8 nothing great you can use any other value. So, 240 by 0.8 10 power 6, this gives me g m of 300 micro Siemens is that ok? Please remember you said greater than 200, so 240 is greater than 200 it is not 300, so it is not too high also. Of course, you can use 200 value here and get what our value, but that is a minimum point you have done this is higher I used it.

So, if g m I already do not written an expression what is g m expression 2 mu cox by alpha into W by L into I DS is that correct, under root of course. So, from here I can figure it out what is the value of W by L. So, A W by L is g m square alpha 0.2 mu cox I DS is that ok, just manipulate. Substitute all values g m square 1.2 as alpha 2 into mu cox is 100 into 10 power of minus 6, and I DS is 62 micro amps. So, what is the final result coming out of this all calculations W by L is 9 roughly accurately you may find, but this is roughly I am very sorry. So, since the length is 0.8, check it whether that is 0.9 also I mean I just roughly did this and may be wrong also, but just. So, essentially W is now figured out for what are the values we met a bandwidth of 2 megahertz gain greater than 200 driving a load capacitance of 0.1 puff with a given technology of channel length of 0.8 with mu cox beta value given to us as this numbers.

So, I have been given a specification, and I have designed the amplifier value, this is how you design. So, it is a inverse process as I said start looking what is given, start looking expressions substitute properly and get the what is not known to you.

Student: Earlier because it was current source.

Yeah biased, strong fixed current source. I can put something to bias by V GS also. I put two resistor across the gate and can give a gate bias as such, I can do many way I can also push from the lower side resource current sync current which is through mirror. So, there are number of ways in which I can play this gain, but as of now I say this is the in this calculation you must have seen in real life if this resistance of the current source is not infinite where it will appear in this circuit this.

Student: (Refer Time: 34:31).

If that has some r o this.

Student: (Refer Time: 34:38).

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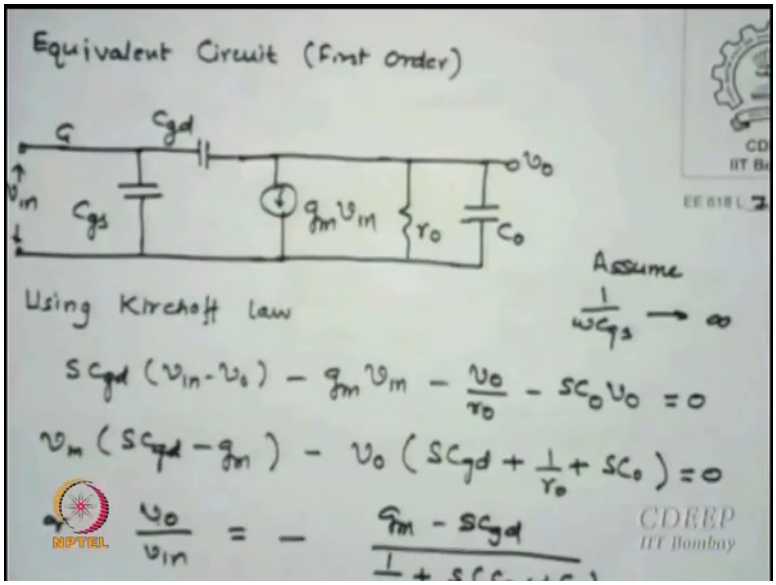

Another r o problem will come from the node side this has to be understood in this case constant current source with ideality is used as I said the either around 0.35 down you should use short channel effects. But people have used long channel devices models even at 0.25 also, but why we are not worried too much about because when you go on a spice for a given technology the models are available for that technology in the spice itself. So, I am not give me looking into what model L, but analytically up to where I should use expressions. So, I say in most cases up to 0.25, you can use these analytical expressions; at the end we are finally, going to simulate on spice and that for a given technology node will be able to take care of the actual models of that technology.

So, we are not too much worried about models, but since I give I want to know where do I start I must know reasonably good initial models, so that I can give you good initial guess is that clear to you? So, this issue are nothing to actual spice simulations because spice will take care of different models are different nodes. And I know it will use different analog models, it will use different r f models, it will use different digital models. So, it has all kinds of programs which it will take care. So, my opinion for this design the g m by I DS is 4.8 per volt.

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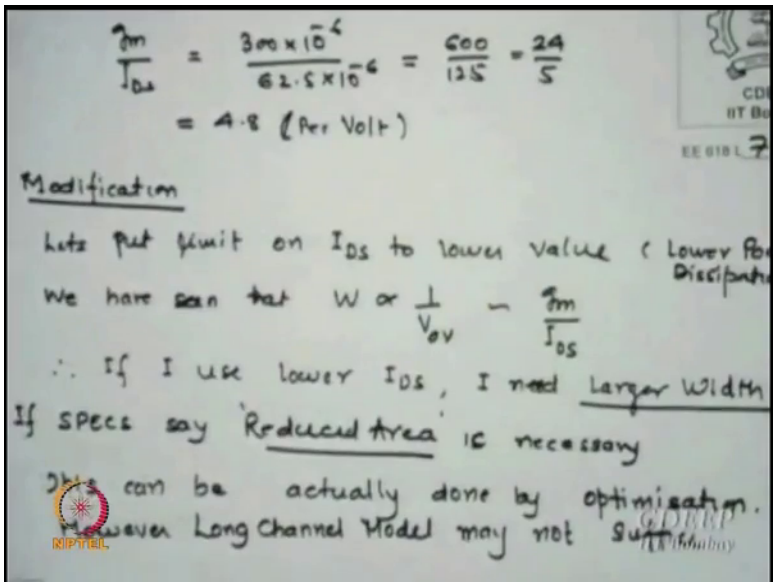

Now, let us say someone says that I want low power design for the same amplifier. So, what does that mean I want to reduce I DS is that clear? If someone says I want to design an amplifier for a low power comparatively right now what is the power this I DS into V DD, which I am not specified, but that is the power dissipation. So, I say I reduce power means I reduce the I DS value itself. Now, what will happen if we see an expression now the width is proportional to 1 upon V ov I have given those expression please way I have given enough expressions for W and everything and W is directly proportional to g m by I DS.

Now, this if I use lower I DS which is what low power people are asking me I will need from this expression width will be larger is that clear is the design issue clear? If someone says reduce I DS essentially I am saying increase widths is that ok. So, what is the penalty I am paying area, but that person may say no it should have a smaller area then I have an issue because you say I want a design which has low power and low area is that point you should clear? I reduce I DS w may increase, and I may need the spec, but now is a minimum I cannot give a area. So, what do I loose in case I do not want loose area either ok.

Student: So, if we increase W, the current decreases only.

If I reduce I DS, W is proportional g m by I DS and fix g m the g m has to they fixed the reason why I want to g m gain has something to do with that. So, I do not want to hit g

m; otherwise I DS is going to hit g m as well. You can see I DS is under a beta into I DS. So, if I release I DS we this will g m will go down, but I will adjust W by L to get that g m. So, I am fixing g m and they say I reduce I DS. So, that the power is only related to I DS. So, I say pull down that. As soon as I pull down that I will have to increase w because I am 2 beta I DS, if I DS reduce beta must improve; that means, width must increase is that ok?

Since width increases based area increase, but specs say reduced area. We understood the design part what I am going why I am showing you have this because as a designer of these are the issues which will come before you. This can be actually done by an optimization. You can keep changing to values till you get reasonable area and reasonable power. However, the models available to you are only long channel models and we say these are not the ideal models. So, how do I optimize that is the actual design is that point issue, but C L has nothing to do with W by L.

Student: (Refer Time: 39:32)

But that C gd is very small compared to the output load. The other load is driving something which I do not know I just put it 0.1 value. See the load is not the part of the circuit, load is from externally you are putting it can be any value in a driving you have to do, OPAMP may drive any load for example, just you write we change, but that is the way it is. I may design for worse driving situations, but load can be anything it is not its plus C gd I agree with you, but C gd is a function of W that I appreciate, but this others values of external loads you and I going to put can be any value. And to say myself I am saying even if that varies the C 0 stronger than the C gd increase.

Student: Suppose in the largest (Refer Time: 40:19) the load capacitance only.

Because the next W by L, I do not no know the next stage which I am driving I do not know what is it you say eighty two inverter input or a space which capacitor filter in I do not know what W by L, they are asking for their input side. So, I am only saying that whatever it is equivalent capacitors I had to drive is so much is that clear? I am not trying to say that this is the final answer if I am just trying to give an method of looking things is that correct as the designer how do we are looking to it. This can be actually done by optimization; however, long channel models may not then suffice that is our issue is that ok?

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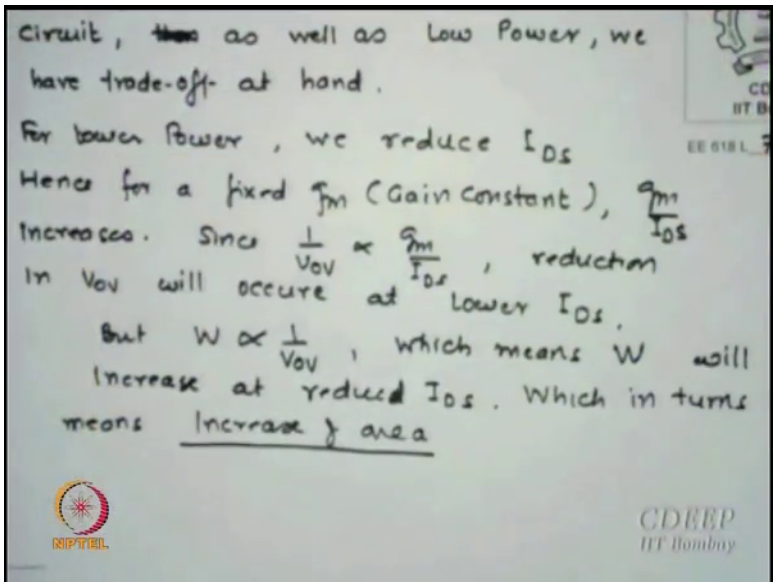

So, just now I said if you are have a design for a smaller area and smaller power, we have trade off situation available. For lower power we will reduce I DS as we say hence for a fixed g m that means, gain constant g m by I DS increases because if I DS reduces g m by I DS increases. Since V ov is 1 upon V ov is proposed for g m by I DS, V ov will occur reduction in V ov will occur at lower I DS, but W is inversely proportion to V ov, so W increases. So, increase of area is whatever you make you always see the w is increasing now how to get rid of such situation because this models are worry is this linearly going or is it some other like it is following if that is. So, done it will not proportionately increase is that clear?

So, I want to see is that model which I use for V ov is an ideal model though I may not have better model immediately, but at least can I do some mischief to actually get rid of this situation is that point, W I mean whatever you do w is increasing ok. So, this all that I stayed earlier is the statement written by here nothing more than that whatever I said earlier is the written part an actual language part are wrote here, so that at the end what I said is available for you to read. So, what is the actual value where what is the accuracy you should build to doing this is what my next is in design.

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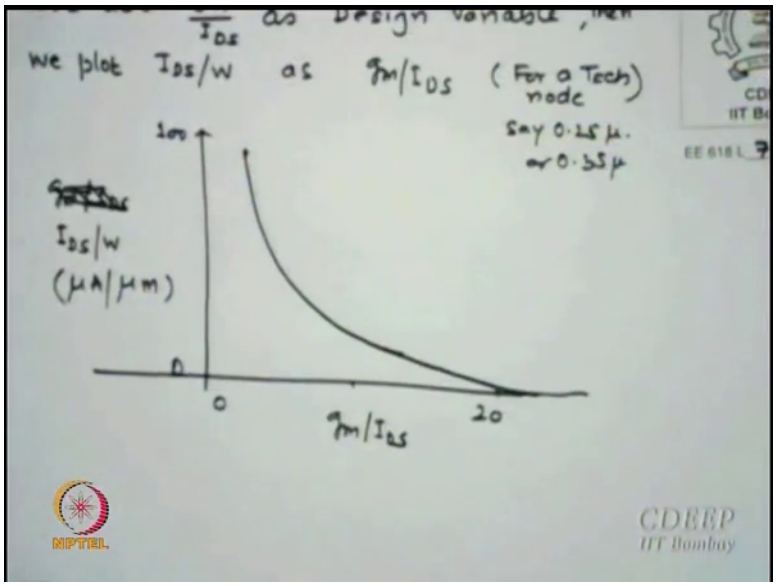

So, what do we do now? In real life do not use V ov as your design parameter use g m by I DS as your designs parameter this is slightly different from most books which they talk, I am not saying all books. Most books they always go by V ov times or we they are called V a x s some called V GS V T V GT books name different, but this is slightly different though please remember they are connected it is not that I am going physics out. So, I say I have from the expressions I have for a real device for a given technology nodes a 0.25, 0.35, 90 all are it is I actually do spice simulations for this different g m I DS I evaluate different I DS by W and plot it is that ok? This it can be done even experimentally by technologists and by simulation by designers. Sometimes this technology people will give you this graph.

What is that I am plotting I DS by w as a function of my design parameter noise g m by I DS is that clear to you? So, I some random members are not really only this is typical values for these technologies. So, 0 to 20 Siemons and I plot micron by micron, micron on this side. So, I say we made smaller the g m by I DS ids by w will smaller and larger this I get w is that clear to you? So, this figure I actually can either using spice or using technology data if provided to you evaluate this, this is a major start work before, once you use this also use it for different channel lengths. You create this graph for you is that clear, which is your base design this. You do not have do n times for a given this you do once; both for different channel lengths if you are going to use multiple channel length devices for each of them you create these graphs.

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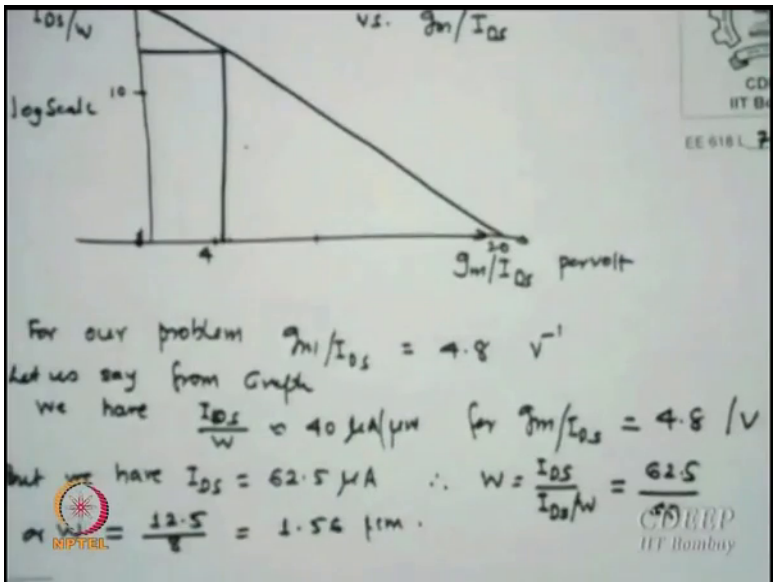

Instead of plotting this graph in that fashion, if I plot logarithmic 0, 10, 100 or 110 to power 1, 10, 100 on a log scale again g m I DS it may look more like linear graph. You know you must know how logarithm term B is not exactly linear, but close to linear. Now, for that earlier problem which I said I have solved that g m by I DS was 4.8 per volt. So, I go on this graph. For this g m by I DS, I actually figure out what is I DS by W, is that clear? So, for example, in this some number I choose which may not be accurate again. So, let say 4.8, this value is 40 micron per micron. This I do not say exactly I can some number, it can be only 45, it can be 38, it can be 30, but some number.

So, for g m I DS of this, I figured out I DS by w is this number, but I DS we are having under was 62.5 microamp from the design. So, I got to know it is only 1.56 microns. So, if you realize that the decision of getting actual W, if you are only use V ov expression, you have over designed the chip, W [FL], but [FL]. Of course, these are not as I say do not take it exact numbers this maybe not 1.8, it actually even maybe 4 microns, 3 microns is that clear to you this number which I am only putting from some, some graph, but this may certainly always be lesser than that earlier V ov model. So, the first time I told you that do not use V ov model, use g m I DS model. And if you use this, your widths will be much more controllable are much more named to you which may be having lower areas then what you thought, is that correct?

So, you have [FL] first time [FL] g m I DS [FL] actual design parameter [FL], it is not V ov. All these years I have been teaching your course is a V ov, V ov. So, this year either I will change my track and I say ok, do not use the V ov use g m ids, but now I figure have I do not I DS [FL]. And from that plot you can get your correct bids is that ok. So, this is a better way of looking a design then the V ov models.

Now, in this case I am not very much worried because spice will have models. So, these graphs can be more accurate to a given node then what the actual V ov models I have derived. So, in that sense I am more correctly doing things which probably will come into real life. So, either designers what is the best way of designing copy some ones, but that is plagiarism. So, do not do that. What does he can do, do this, is that ok?

So, this is I have keep telling you that once I said you that every year I change my track. So, this year I am changing my track to saying it is I DS g m by I DS as a parameter of design though please remember to 2 I DS by V ov gms. So, I am not really going out of physics, relationships are similar, but not the same as I just shown you. Is that clear? Because it now is taking care of the real life situations in the device that clear; that then you do not have to worry too much because this will take care of all such things which could probably occur is that clear.

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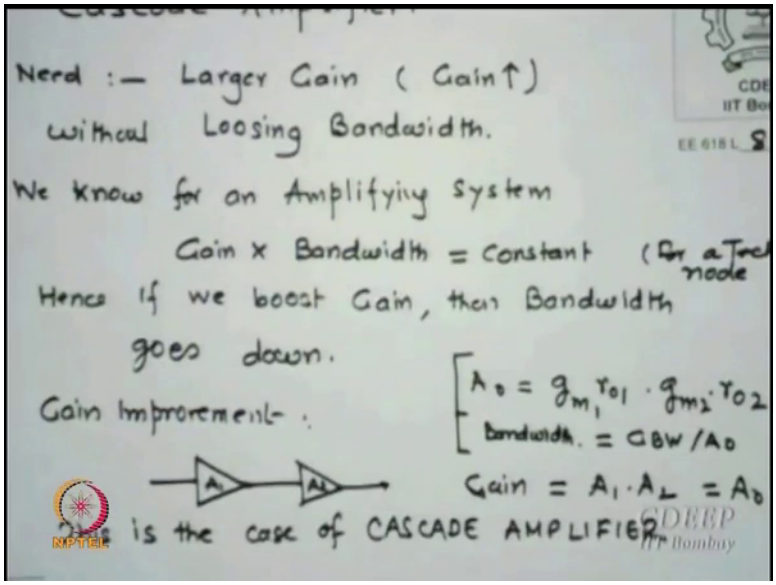

The second amplifier of my interest the first amplifier I said the gain is g m times R 0 and gain bandwidth g m term by c, is that correct. So, if I want to increase the what is G

B W - gain bandwidth product which is g m by c. So, if I now take a system in which I want a larger gain, one method is I can design a single amplifier with larger gain that is also possible. But the problem there is it will have to huge values or W L s, it is called the aspect ratio would be very bad for you would actual designs.

So, what is the most common practice of doing designs is to put cascode off two amplify you want 100 make 210 gain amplifiers and cascode them cascode means output of first is given to the input of the next. Let us say each has a gain of A 1, A 2 which is g m 1 ro 1, g m 2 ro 2. So, the gain is g m 1 g m 2 r o 1 r o 2 and if they are equal g m square r o square is the gain. However, the bandwidth is gain bandwidth divided by A 0. So, what does that mean if I increase the gain my bandwidth is going to be lower now.

So, cascode amplifier has yeah I do increase my gain, but I have a problem of using the bandwidth across, but that is what we do not need. In most design what will require a most system what will require, I do not want to lose my gain bandwidth, I want to keep my bandwidth same, but I want to boost the gain. This gain bandwidth product is called figure of merit. Why it is called way for a given this g m by C, for a given I DS given capacitance, say this is fixed is like an f T value equivalent of that. So, that is a figure of merit.

Now, this figure of merit is that means, sacrosanct technologic [FL] power supply [FL] fixed [FL], but designers cannot go by saying that I cannot increase gain without using bandwidth if they says so then there is no design left. So, [FL]. So, the alternative to this cascoding the word we use is amplifier we use is called cascade amplifier.

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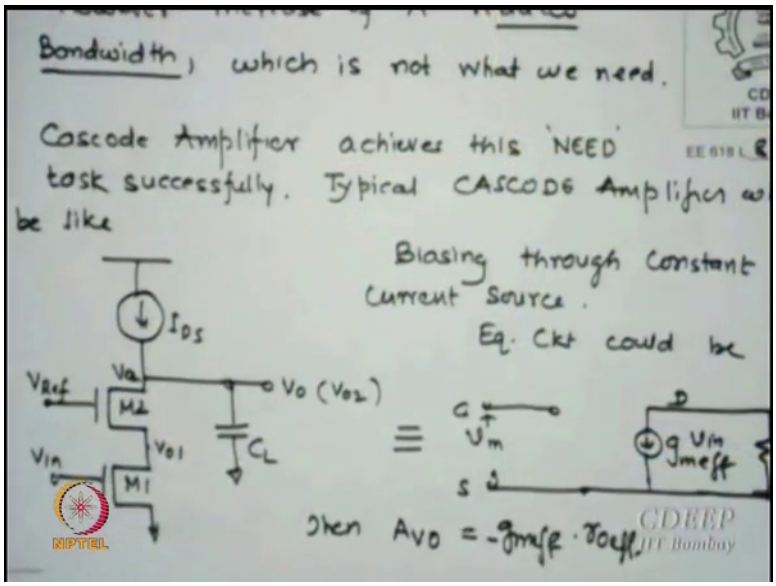

So, our need is not to reduce bandwidth, but to improve gain. Cascode does not, we figure out the another way of looking the same thing and we call that as if our cascode amplifier which allows us to retain bandwidths, but push the gains. What does that mean you have broken the technology figure of merit gain bandwidth product is constant you said now I am breaking that. You said all right the [FL], now I am trying to see I will boost the gain, but I will not lose my bandwidths, is that clear?

A typical cascode amplifier is shown here just forget about M 2 first. So, it will be a normal amplifier M 1 is the dire and I DS if the bias current source. Say, if I have M 1 this an a interprets a transistor M 2 in series, though cascode amplifiers have its their own problems which you shall see later, but there are folded cascode opams available opa is available. So, this process is very nice. What is this, what is source is grounded. So, which amplification it is doing common source. So, this M 2 I am giving a fixed dc bias. What I mean of fixed dc bias means for ac what is that terminal ground?

Student: (Refer Time: 53:49)

Fixed dc means ground. So, what is that amplifier is what kind, common gate amplifier. So, I have a common source amplifier get in a next stage is common gate in cascade, I have both common source. The first time we change from common source to next stage is common gate is that ok? What is the difference between the two, both stages in cascade was common source, here common source is followed by common gate, and that

helps to improve gain, but not lose that is exactly what cascode is alone. If this is what (Refer Time: 54:34) circuit is equivalently saying assuming right now Cs are internal Cs are not used equivalently saying I want a cascode amplifier which had a current source as g m effective V m shunted by r o effective and of course, the load capacitance, is that ok, this is what I am looking.

So, the A V 0 will be g m effective into ro effective. Now, if g m changes what will change the bandwidth will change gain bandwidth powerful vary on that. Where if g m does not change, but only r o improves then I have boosted the gain without getting out of bandwidth issue, I am getting out of bandwidth issue is that clear. So, I may like to do a design for this amplifier in which g m may remain almost constant, almost little bit this, but r o may boost by r ds as much as I want actually that is what the theory of cascode amplifier is.

To worry as a designer which will solve this problem soon is something like this. In analog circuit what is the guarantee of each transistor region all theory on divided on what basis the transistor is always in saturation is that clear to you? So, there will be a V DC at here or V D drop V DS drop here there will be a V DS drop here and if this current source is the plate by similar two p channel transistors there will be two vds drop ups upwards also. So, from the power supply to the ground how much voltage now I will have to drop 4 V DS. If I want little more I am put another series in that I may require 6 V DS; a minimum V DS we shall see later is close to V t to make transfer in saturation which essentially means that now you are closing V DD either you improve your V DD further. So, that I will be going to this or some transistor may come out of saturation.

So, cascode started fantastically in theory, but in real life or worry started as chain increase in series, this is like a NAND gate situation. If you are larger find in kind of NAND gates, the issues is too much capacitance comes and too much current drops have to be gain because that each you will have to be then turn on, speed any were go there. So, it reduces all your other hardware. So, the NAND gate function is similar to what here we are now saying that too many m series I please take it every time into I push it by gain a put another one I will put another gain on that. But if I put too many now worries are the transistor will not remaining saturation for a given V DD.

So, there will be some limitation of maximum g m R 0 which I can attain even in cascode for a given technology nodes. So, it is not that you can increase this to any number you have limited by. So, [FL] modifications [FL] folded cascode. So, we tricks, but it is a one V DS down there for other [FL], but still it is not small as much you put additional power supply voltage either is required or you can no more than this change is possible. So, there is a limited gain increase, but the gain a advantages your bandwidth gain bandwidth product is retained that is exactly what we are trying to do in cascade.

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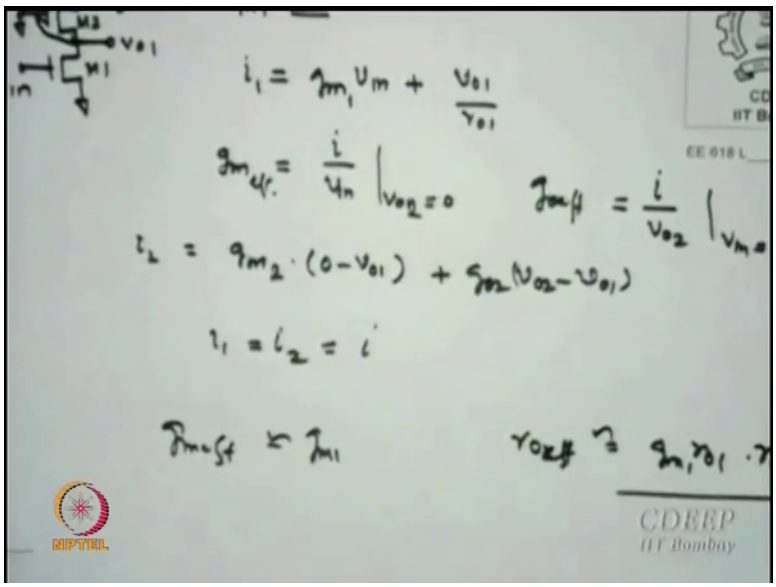

For in ac case, this is my V n, this is grounded. This is V o1, this is V o 2, this is equivalent of ac. Now, what we say let us say the current flowing through this small ac signal for a V in is small i. So, we say for this transistor M 1 and this transistor M 2. So, let us say for M 1 now i is equal to how what I should write, yes.

Student: (Refer Time: 59:20)

G m 1 V m plus V o 1 by r o 1 equivalent circuit, two current sources one g m other V by r. So, two current sources in parallel that the met current in the drain side is that clear? Now, what I do is I actually want to do something in which I will say if I say g m and I say I upon V in at V o 1 is 0, for the first case. But if I do for the other than let us say this is I 1, they I 1 into same, so g m 1. Similarly, I can write i 2 what is the i 2 g m 2 into how much mainly just think of it, how much is V GS there?

Student: Minus 0 1 minus 0 1 minus 0 1.

Minus V o 1 0 minus please remember the V GS for this is base. So, 0 minus V o 1 is the V GS for that. So, 0 minus V o 1 is that ok? What is the current in this plus g o 2 into V o 2 is that clear, is it ok? So, now I figure out.

Student: (Refer Time: 61:03) even the minus minus p 1.

Ah.

Student: (Refer Time: 61:04).

Oh sorry sorry your right you are perfectly right V DS, I am very sorry you are perfectly right. R os is g o, 1 upon R os g o. So, now, what I say if I had this expressions and I can now say for any amplifier g m is defined as if I ground V o 2, then what will happen ground means for ac. So, the current is only proportional to V in which means g m is o by V in. Please remember current in a circuit is still same is that clear ok, current in a circuit cannot be 2. So, we say i is constant which is flowing through both M 1 and M 2. So, now, g m is only gain that sorry V o 2 if I say g m effective l I say I should not say is g m effective; g m effective is i by V in when V 0 is short it. By similar argument what is g o effective will be, yes i by V o 2 1 V m is grounded. When input is shorted impedance c at the output node is the output impedance is that correct?

So, I might have now I have figure out a relationship between i 1 and i 2 from this such that I can derive g m effective and g o effective. And once I get what is the thing I am getting g m r 0 is the net cascode gain is that clear to you? And that I will g m by c if g m effective comes to be same as g m 1 let us say then my gain bandwidth is not changing because g m by c is that clear, but the same time gain is boosted because gain will become.

So, I will tell you r o 2 or r o effective will be g m 1 r o 1 times r o roughly. What is this what is g m r o 1 the gain of the m one multiplied by the output resistance of the second will be the r o it will derive this is I am just giving you hints on that because this time is running out. So, I just does not want to derive it. So, the gain in cascode is that I somehow want to push r o higher by retail g m as what it was. So, I will beat that

technological strength and I will say other, but you are really looking for in theory what we are doing is the following.

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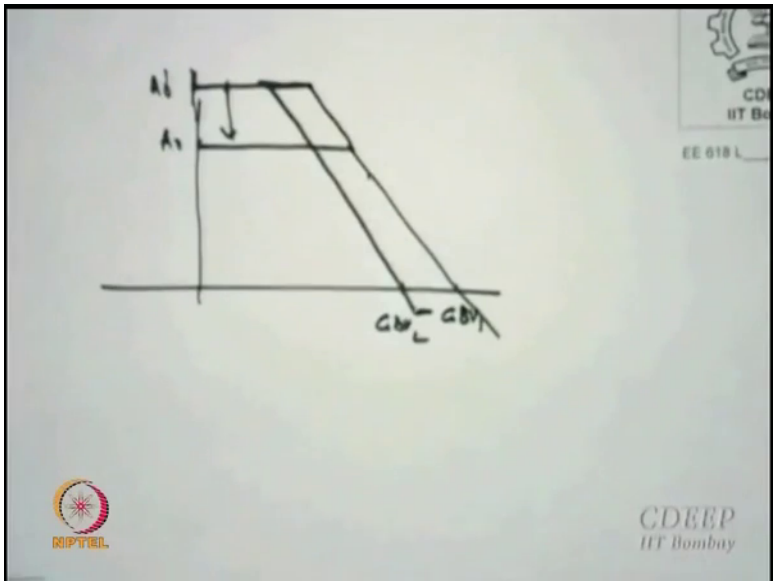

Normally what will do is if this is your amplifier, this is your gain bandwidth product, if I increase the gain really, I will get this curve. If I boost the gain A 0 to A 0 dash more this point g gain the one mainly to gain bandwidth two which is smaller. This is what will happen in cascades. So, what should I, what should I what do I now really looking for I may do this, I am trying to do this, I still reach the same point, I improve the to some extent the bandwidth and I also improve my gain this is what cascode does. This is what cascade is trying to do, is that clear? That is why cascade amplifiers are ideally suited for analog applications, but what is the catch in cascode as I will said we will discuss in next more detail that the V DS adjustments becomes very, very crucial.

Typically V T is not now equal to 5 times V DS is not 5 times V T I made these to have 1 volt, V T 5 volt V DD; now 0.4 word V T and 1 volt V DD. So, only two and half times. So, 5 on 4 V T drops it is 1.6 volts supplying required, where I have only 1 volt or 1.2 volt supply. So, now, I am constrained that I cannot use cascode at random because my V DS situation may be not very conducive to me is that clear to you, otherwise theory wise it seems to me I should just forget cascading and use everywhere cascades.

See you on next time.