CMOS Analog VLSI Design
Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture – 06
Basic of MOS Amplifier (part-2)

We are continuing with our small signal model before we start amplifier. Typically, as we have so far solved equations, the equivalent circuit of a mos transistor is shown here. This is your gate, this is your drain, this is for common source.

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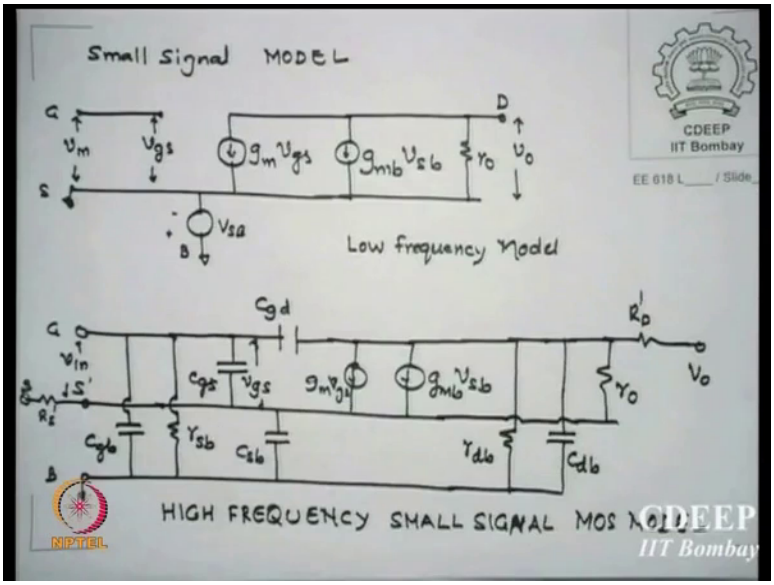

This is your source, which may or may not be grounded in some cases it may be. And then there is a bulk. And we believe, that all capacitances are right now not relevant in the low frequency range. Essentially, it means 1 upon omega c, if such that it open circuits everywhere.

So, assuming that you can see there is a input voltage of V GS which is equal to input voltage of V in and since gate has no connection resistively to the source, this is a open and therefore, V in is equal to V GS. At the output side and the drain side, you have the current source which is gm times V GS or gm times vin plus, and there is another current source which is due to the V sb substrate bias; which will give me a gmb V sb term, shunted by r 0 as the output resistance.

Now, if this is the low frequency model, and in many cases since we are interested in the MOSFET's or mos circuits bandwidth which is the frequency at which gain is at least reasonably constant. For those frequencies will require capacitances, and this is an equivalent circuit which is call high frequency small signal models, this is most important all this analysis always has been done for small signals. And the issue we shall raise little later, if there is not enough small signal word satisfied, what do we do. That is one of the major issues right now in most new devices and circuits. You can see from here source has small resistance rs dash; which is the source region resistance n plus region resistance rs dash.

Similarly, there is a drain region resistance which is re dash. The rest part is similar; this then there is a capacitance across the C gs gate to source capacitance, which we declared as V GS. And there is a capacitance between drain and gate which we call C gd, then at the output side there is a gm V GS as the one current source gmb vbs be are the another current same as this plus, and they r 0. So, they are same.

Now, what is difference is; there is a capacitance between gate and bulk. Sometime in gets screen sometimes may not gets screen, but we should show it in case it is screened we just remove that. And there is a resistance which is associated for substrate. That is call rsb, and there is a resistor capacitance between source and bulk, C sb. Then there is a capacitance between drain and bulk C db, and there is a resistance of the drain side which is R Db.

Now, these are essentially equivalent of a diode you know, r into parallel c is what the rc combination. So, these are those resistances in are normally they are very high. So, open circuited, but as a logic we must put them, and then say they are large small and when we remove them out. But this is total small signal high frequency equivalent model of an mos transistor, and in case you want to solve this, the easiest ways to figure out the values of each of them. And there are number of loops or number of nodes whichever way you want to solve Kirchhoff's law. You will be able to solve V 0 versus V in relation. That is what we are looking for at then gain V 0 by V in.

Since I have enough nodes are enough loops, I can solve as many unknowns has been in notes or has been on has been meshes. And therefore, you can always solve this circuit, will give a small example to show how do we solve that. In all analysis please take from

me that this may be a very good base, at the end of the day we will not solve actually all the circuit by hand. But to start something on cad we need some hand calculations.

So, in that hand calculations all model can be simplified. Because you are only trying to get the first guess in that case all this. Detail values may not be required in many hand calculations. Though there can be some error in hand calculation, I will list them out what happens, if you do not take care enough in case of designs; however, this is the model which we will be using for a mos transistor, and this is shown common source, but it does not matter. You can tilt any angle to get it common train or common gate, whichever the way the circuit remains or the equivalent circuit remains same.

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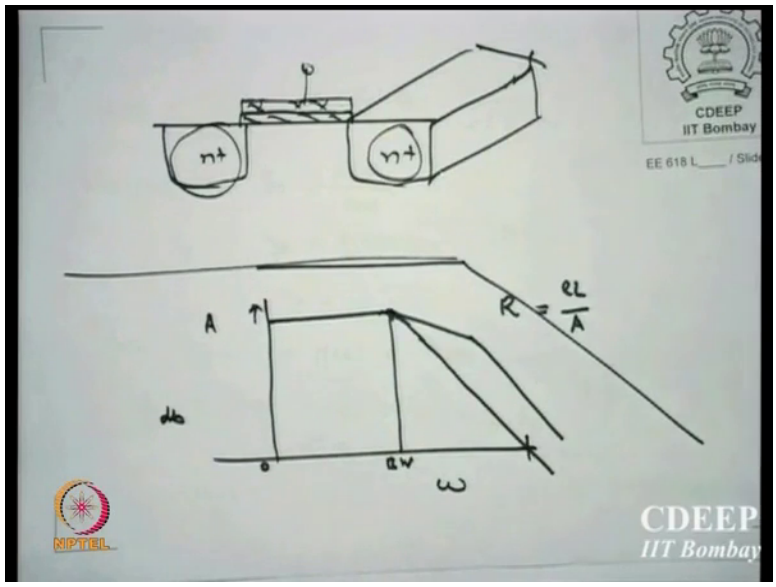

Let us say it is n channel, all this device unless had otherwise devices are n channels, if there is a cmos part, there we will explain that cmos again. There is a resistance associated with this region, and there is a resistance associated with this region. After all there is a semiconductor regions, and they may have heavily dope. So, the resistance may be very small less than 5 Ohms or 3 Ohms sometimes, depends on the area.

Now, that is where the problem started. Why we started looking into it? If you see a rho L by A as the R, you may actually reduce rho, because of doping higher dopings. But this area also is going down, because you are scaling. So, if you scale down, this is area may not be as what it was earlier it maybe 100 time thousand times lower.

So, essentially r may not be as small compared to what we thought in the long channel devices. So, please take it that why this new models are added this terms, because they may be dominant terms not nominal, but they may actually change the pole positions or 0 positions. And therefore, one must take care in solving any Kirchhoff's law on the any circuits, is that clear? In normal case we neglect them, we say it is few Ohms the others are kilo ohms. So, forget it if they are in series. But if they are in shunting then they will be the one who will matter who most of it times.

So, one has to take care of all this in writing as circuit requires comes will remove the terms which are not relevant in evaluations. Is that n plus? This is like a 3-dimensional device a 3-dimensional register. So, this is a bar of semiconductor which will have some resistance rho L by. So, this is what we keep saying you that this is needed because in case you are using accuracy than you may need them also.

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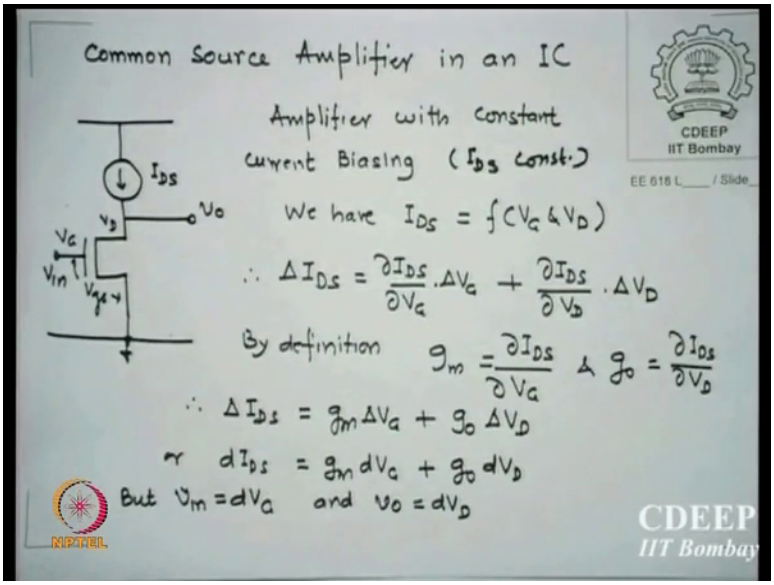

So, another method of following the same amplifiers which I will earlier did; this is my method which I always say that you know you can look at the solving any equations, or solving any circuit, by very different small signal analysis. Not really very different, but interesting way. So, I just always want to show you how to I can solve other ways. Let us say this is a common source amplifier, which is bias by a constant current biasing; which is constant current biasing is I DS is constant fixed current source. Right now, I also assume it is a good ideal current source, what does that mean? The output resistance of

that current source is infinite. In real life if I replace this by p channel device as a current source, it is R D r 0 will actually come into picture. Is that right? Now it is assumed constant current source ideal, in reality they may have to be modified for the real r 0 comes there.

So, this analysis is I just this is a technique, and this is nothing great about these solutions which otherwise you will get. We know this current I DS flowing in this transistor is a function of V G and function of V d which is a standard mos transistor theory. I can use my partial you have partial differential kind of partial differentials of this to equate sometimes. I say change in I DS must be equal to red I mean delta I DS by V G into delta V G step.

Similarly, for the V d delta I DS by delta V d into capital delta which is a step function. We know by definition change in drain current with gate voltage is essentially gm. Change in drain current with V d drain voltage is essentially g 0. So, we rewrite delta I DS with gm delta V G plus g 0 delta V G, if I convert into differential forms it is delta dids is gm dV g plus g 0 dV D. In our case change in V G is essentially the input signal AC signals.

So, ga vm is dV g V 0 is dV D, which is the output AC signal which is nothing but change in the drain voltage is because of the small AC signal which is applied at the input. Is that okay? This is as I say many people believe that you know this is better way of explaining that 2 port parameters which you have must have learner you must be learning now somewhere s parameter A V parameter h parameter. How do we get parameters from any transfer functions? This is how we get it. So, that is the technique I am showing you how do I get 2 port network solutions this is how one can try any 2 puts or any inputs in fact, longer difficulties in solving.

So now I have equation delta I DS is del gm del V n plus g 0 dV D. So, here is that expression, which it will appear and I put it now.

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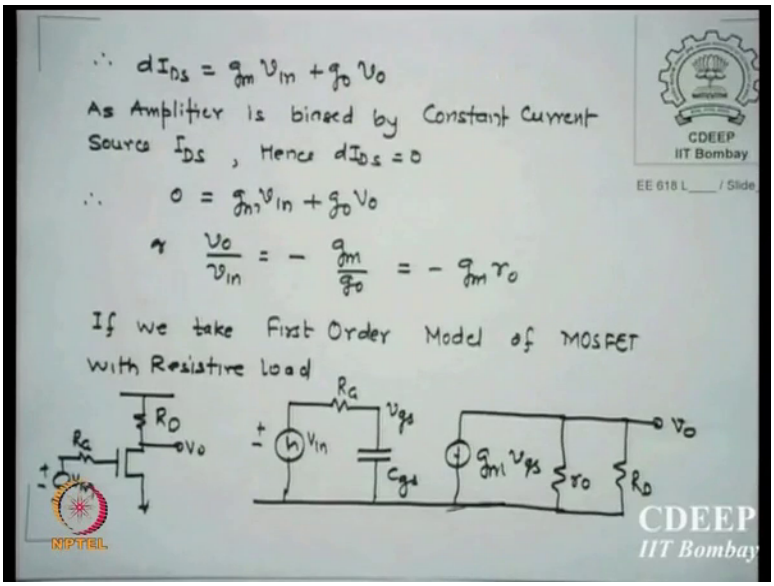

So, I get delta I DS is gm V in plus g 0 V 0; as amplifier is bias in constant current source, there is no change in current. So, g delta I DS is 0 which is equal to gm V in plus g 0 V 0 if I take a ratio of V 0 by V in, it is minus gm by g 0, g 0 is the output conductance which is 1 upon r 0.

So, it is minus gmr; that is the expression we derived. This is called intrinsic gain of a mos amplifier. Why it is a intrinsic? No load resistance was used, instead of load we have constant current source, with infinite output resistance for that, is that clear? So, this is gm times r 0. Now if we take the first order model using an R D now instead of constant current source, the and let say there is a series resistance with the source, and then and let us say some capacitance C gs is taken care. And right now, assume that C gd is open circuiting at a frequency of my interest; then I say V in is R G equivalent. So, there is a C gs which is holding the V GS voltage. Then it is gm times V GS r 0 shunted by R D.

So, this is as I in all these cases V sb is taken 0, that is source and bulk are grounded. Unless specified do not use those terms. If I specify something or indirectly specifying it, look for that value and substitute in gm be V sb terms and solve for it. What is that you have to do is just add many times 0.6 1.1 plus points it is gm is going up as the gmv equivalence of that.

So, you can need not solve many times, just add instead of one put one 0.6, and you can get rid of much of the solving. This is for hand calculations. So, this much assumptions

may not be very absurd, but in real life you may have to calculate actual values given doping given everything, and then figure out what is the gmv values you get.

So, if this is my equivalent circuit. Why I am doing it? I want to give some numbers, which is very interesting in designs, and that is why I am trying to look for them. Is it okay? This is in equivalent circuit there is nothing great all that I put 2 terms here, and additional term R D here. So, this is still low frequency that C gd is open circuiting, when upon omega C gd is still infinite, infinite enough to neglect open it.

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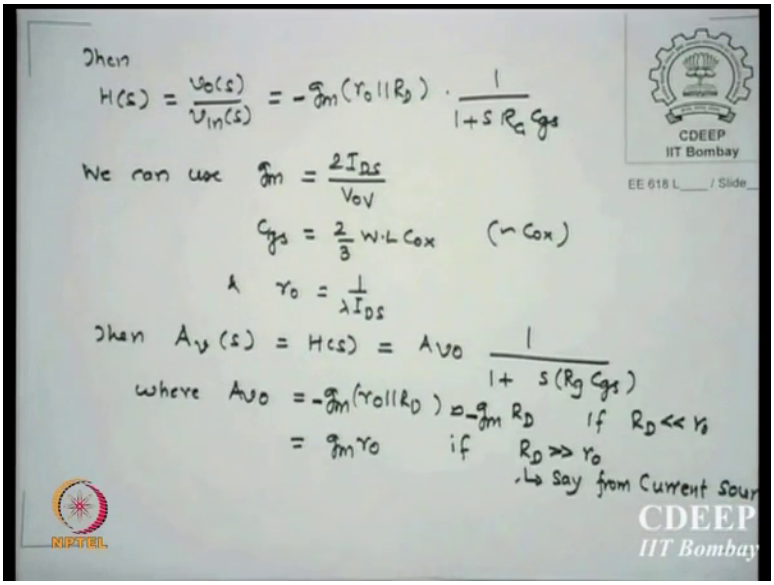

So, the transfer function from output to input, which is the gain function A V S, which then can be written as gm r 0 parallel R D, I should have put a minus sign here, because if face opposite. Now we can use some derived values for gm C gs r 0 which we already derived in our device theory. And earlier we said gm is 2 I DS by V ov which is V GS minus V T the excess voltage.

So, those who all taken a course of my analog like service there, and many others there is the difference in approach when I come to design a course. The basic I cannot change I mean analog amplifier will give me gains, but how do I derive and how do I am actually get design for it is what I am now showing. So, it is nothing extraordinarily different from what we learned in second year, but even then, it is we are looking at it. The C gs value we calculated are the rate is 2 third w by cox in saturation. If you wish you can use

one (Refer Time: 14:59) cox term as well 2 third can be made one, but if you want to keep and I do keep some times.

So, I am keeping it, but as I say if someone puts it this is nothing very absurd will happen. R 0 is 1 upon lambda I DS which is the current. Then A V S and A V 0 is defined as sorry it is minus everywhere is gm parallel r 0 R D. You can see from here sorry, I will just put it and come back. The current in this parallel resistance of r 0 R D is what gm V GS current is flowing through. So, minus gm V GS into r 0 parallel R D is my V 0. So, that is what exactly is gm r 0 R D is my DC gain. And if you say R D is much smaller than r 0 it is minus gm R D. If r 0 is much smaller than R D, it is gm ro. Which case this will occur will take a first one is normal resistive loads. The second is the case when.

Student: (Refer Time: 16:04).

The biasing is constant current source, in that case r 0 will be R D will be much larger compared to this. And in that case probably this term can be that is why it is a intrinsic, intrinsic case. So, once we do this. So, what is the trick I am trying to show you? I am trying to derive some expressions for gm I DS and gmc gm by C gs. And these are the 2 expressions I am going to use in my designs. So, I want to get those expressions from what I am writing. I normally use a term which I will show you later. Ro parallel R D is small rod which is ro parallel R D, and then you can replace it by either ro or R D depends on the values. All you do not you solve it and you automatically one of the term may go if it is much smaller or much higher. Is it ok?

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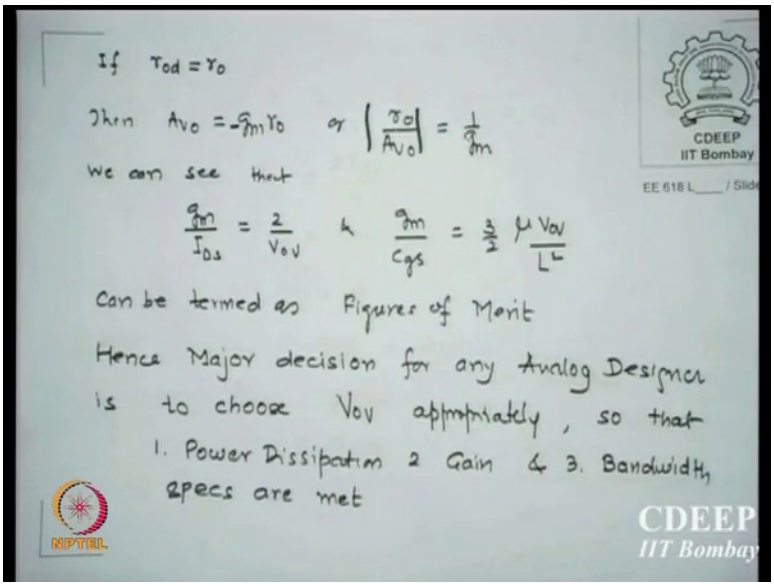

So, having done this if rod is r 0 as I said in that case A V 0 is minus gm ro, then I can write r 0 by A V 0 is 1 upon gm. And this expression 1 upon gm magnitude do wise. Then I say gm by I DS, I know is 2 by V ov, I know gm by C gs is to 3 by 2 I had derived last time mu V by l square. Then these 2 terms I will call them as figure of merit figure of merit for analog designers. I repeat which are the 2 terms I am going to design for; gm by I DS and gm by C gs. Please take it this gm by C gs is essentially ft and will see what that term is. That is why it is called figure of merit. Gm I DS is a figure of merit because it decides what? It decides some way the power it decides the bandwidth. And therefore, the gain is well. So, that is the figure of merit.

So, what is gm by I DS, and what is gm by C gs will decide every aspect of an amplifier. So, these 2 terms I call it as figure of merit. So, what is the major decision for any analog designer; is to choose proper V ov. You can see expression everywhere you are only seeing V ov. So, if you can choose proper V ov. So, that the power dissipation, the gain, and the bandwidth specs are met. Is that correct? So, what is the designer spec V ov. Is that clear? V GS minus V T; how much excess voltage you want to keep for the bias requirements? In all that matters in decision of making power, dissipations, gain, as well as the bandwidth, is that correct?

Somehow though I am keep telling you all this and then I say I do not like this V ov term very much, and I will revert back to saying I will not use this. But initially I we say V ov

is a great term which allows me to design every spec which I am really looking for. The choice of V ov typically what do you expect the value of V ov should be in a smaller technologies now anywhere, any idea? Let us say I am working on one-volt supply, what should be typical V GS minus V T will be?

Student: (Refer Time: 19:34).

Point 2 volts. So, typically it will be around 200 millivolts is kind of V ov values, you will have to choose. So, one technique is fix V ov do something. Or fix something else and let vary V ov. So, we are we are trying to design based on these features. So, is that clear? So, V ov in my opinion is one of the major factor which designs the circuit performance. What are the 3 parameters? I am looking for an amplifier. Again, a power dissipation, and the bandwidth. One term which I have not said maybe I will have separate chapter to that, and accept it talk lot many on that, which is the noise part. We are assuming as if everything is nice for us. In reality the killing part will come from the noise part, and also temperature part which we assume as if everything is fine. All models are fitting into all our requirements, which may not be really true.

So, the whole why spice or why everything is; because all such variations analytically solving for all of them simultaneously becomes very clumsy not that impossible. But very clumsy, it is much easier to go on a cad tool to solve that. So, if we see this expression which I wrote here A V 0 1 plus s R G cg same expression which now H S is one of gm r 0 R D 1 plus this. So, if I now substitute gain function as A V 0 1 plus s R G C gs. R G C gs has a some kind of a trance time constant means is a pole sitting right there.

Now, please remember if we has done our second-year course well which we I hope. So, all of you have done. So, if I plot frequency versus gain, then I figure out for certain frequency till certain frequency gain is constant, and then of course, it goes down and goes down like this. Of course, this is a 3 db point where the gain was 5.7, but as a bodes plot we can actually connect to slopes, and this frequency from where the gain starts falling is our bandwidth up to which gain is constant.

Now, few things I must know. I want to increase this A. And that means, I am really looking for something like this. In real life I want larger gain, larger bandwidth. And also in turn power should not go up. That is what I am asking myself, and then I will say, then

I will say what I can actually work with so that the third parameter may help me to get what I want.

So, 2 I can get maybe third I will have to give up. So, within a given range, if I can fit that then I say I had design an amplifier, is that so my worries are bandwidth gain what is this? Term essentially if I plot in db, then this is 0 db.

Student: Unity gain.

Unity gain. So, this is the point gb gain into bandwidth, is that correct? And this point actually we may like you can do like this. You have many ways of moving this point. So, we will see how can you play games; that means, how many capacitors are around and where they sit, where this poles positions can be changed to suit your requirements. Sometimes you additionally put capacitance, some time you see to it the capacitance are not really strong there. Which are where we can adjust will see to it, what can be done is that.

So, design means given a spec how do you play with. So, we have already said; that the gain bandwidth this R G C gs is related to bandwidth, now because that is the only pole available to you.

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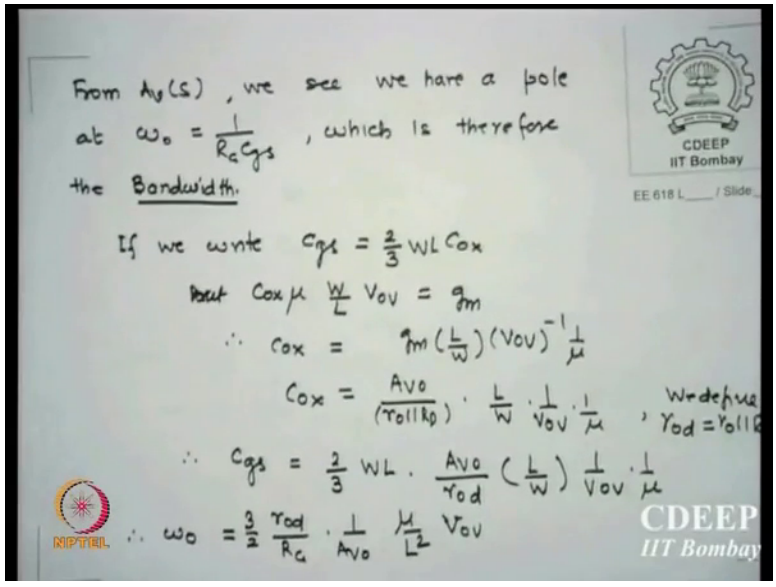

So, we therefore, say in the case of circuit shown by me no C gd and no output capacitance. The dominant pole or the only pole available to you is 1 upon R G cs. And

that is the one which will decide the bandwidth. If we right now C gs as 2 third W L into cox, we can write also we know gm is mu cox W by L into to V ov. We have derived this expression earlier. From here I would get I find out cox from here, and substitute in C gs. What do? I do from this gm expression, I get cox value, and then I substitute in C gs value. Is that point what clear? I use the second equation gm is cox mu V ov. Evaluate a cox something like this, gm l by w V ov to the power minus 1 1 upon mu. And then I play little game. I say if you see carefully gm r 0 or rod whichever you say is the gain gm ro is the gain.

So, gain by ro is gm. So, I replace gm by A V 0 by ro parallel R D or you can keep one of them also. Into are l by w which is the aspect ratio 1 upon V ov into 1 upon mu. If I see very carefully now, this w 0 if I substitute back here; now C gs I have calculated this long expression, I substitute with in my bandwidth terms. 3 by 2 rod by R G 1 upon A V 0 mu upon l square into V ov. This is the expression I get for my bandwidth. Why I did all this calculations?

Student: (Refer Time: 25:40).

I am looking for gain into bandwidth, and I am also looking which term will actually vary for what I am looking for. There are 3 terms there I will show you. I will right down I will show you this; if you finish it this I will show you what I meant. I repeat, my worries are power, gain, bandwidth. So, I am trying to see expressions in a different form.

So, that I will see which term likes a power; which of the terms in power expressions which will actually enhance the power. Or which will reduce and reduce the power. But if I reduce this I will come back to the other expression see if that term varies here, what will happen to the second expression which I used w for example. So, I keep writing expression for each which are of relevant for me, and I keep playing games to see which term is dominating for me, and when I can control. Is that design issue clear? So, it will be is that now you understood why second year to 4 4th year there is a issue? Or rather fifth year sometimes.

So, the issues are that is the design part. So, please remember what why we have a separate course on analog design a VLSI design, because there we only solve something. We say it is fine, it comes like this. Now we are where it given something how do I

match it. So, this inverse process needs much thinking than, because there are many possibilities which may do that. Which one is better? But if you choose one than the other may hurt. So, where done we get hurt which terms are important is designing.

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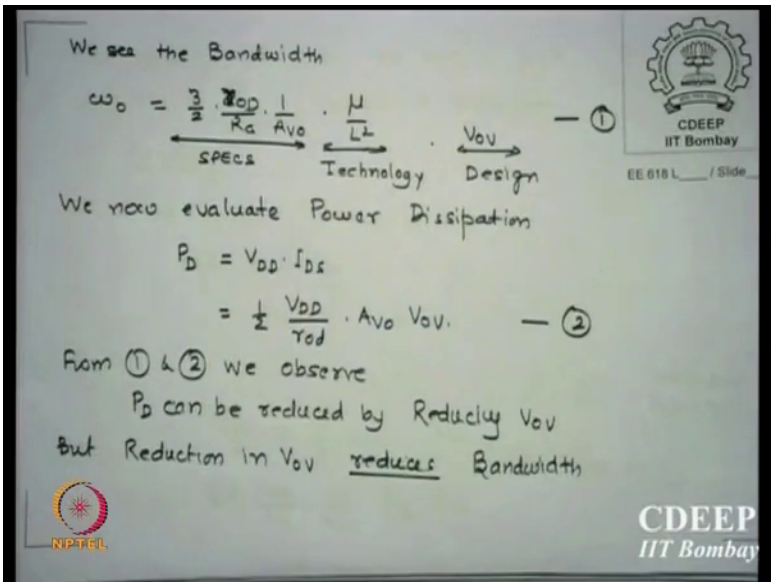

So, is that omega 0 term is clear. So, I write now same expression. If I put it here you can see now w 0 is 3 by 2 rod by R G into 1 upon A V. Normally these are specifications for the amplifiers. Gains are functions, R G is externals resistance of the source which is generally 50 ohm to 600 Ohms depends on the source. You use rod is normally R D if you are putting a resistor there, that is something which you have fixed. If you have put is a channel length somewhere you are fixing ro.

So, this we say is essentially specs related. First few terms 3 by 2 rod by R G into 1 upon A V 0 is this specs related. The second term there is mu by l square. This is not in my hand it is a technology people will say this is the best mobility I can give. And this is the length of the technology note I have use 0.18-micron, 0.13-micron, 90 nanometer. Whichever technology L in mu is decided them. We have no control what isoever on them.

So, this is whatever technology gives that is a spec for, I mean you can not change. Let us look at the power; dissipation is I DS is the current power supplies V DD. So, the DC power dissipation is V DD times I DS. If I substitute that I DS expression from the this I can rewrite, please check it A V 0 related to gm please, what is gain? Gm times rod. Is

that correct? Gm can be written in terms of what is that? I DS by 2 ideas by V ov, manipulate expression. That is what I am keep telling I will just manipulate few things. So, I get half V DD by rod A V 0. And now we observe if I want to reduce power dissipation, what should I do? This is all fixed; We.