CMOS Analog VLSI Design
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Lecture - 04
MOS Fundamentals

My interest of course is in gain, and if I see a equivalent circuit of a normal amplifier using a mos transistor very, very low frequency circuit. Nothing very great happens.

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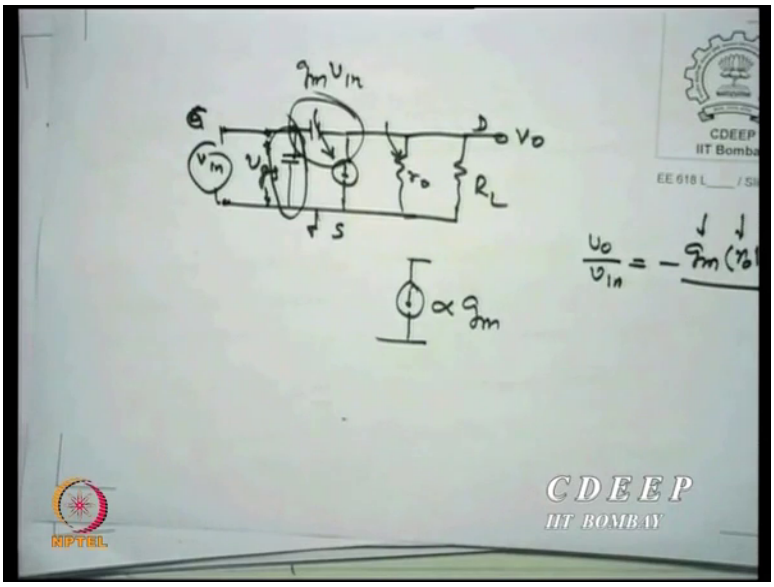

And it is let us say it is a common source, and I figure it out, that this is what is going to be seen by me. And this current source and this are 0, somewhere related to the device. This is a small signal low frequency equivalent circuit of an amplifier, common source we will come back to it again, I am just trying to say you.

So, my worry is if in a circuit, if I have a current source, which essentially, I am showing you something like this. Now this current source is a function of gm. Essentially, means it has something to do with the device, as well as the amount of biasing I am going to do with it. And since gm is what is most worrying me, I would like to have a model of a transistor which will replace or which will give me equivalent of gm expression. Because at the end of the day I can only solve something numerical.

So, I must create a equivalent circuit for a current source in terms of device parameters. And once I know what those device parameters are to govern which will control my gm, and similarly r 0, then I will say I had design an amplifier for a gain of V 0 by V in which you can see the very clearly is that if the gain is simple like this, it is minus gm r 0 parallel rl divided by there is no input impedance right now. So, it is infinite there. So, 1 upon infinite. So, 0 there is nothing 1 will be appeared 1 plus that.

So obviously, if I want to control gains, I must control gm and r 0. If rl is very, very small compared to r 0, I am not very keen about r 0 either, but in normal case I may be interested to know what are the values of r 0, and what are the values of gm so that I can control V 0 by V in, that is my ultimate aim. Of course, this is a simple circuit will actually modify the circuit more complex way. And we will see whether we can have some equivalent model of a transistor, which represents equivalently of this circuit.

Because at the end of the day when I design a chip, I have processes and I have sizes. We are done a mos transistor theory earlier. So, we know we can only control sizes w by ls, we can control partially mobility which is not very much in my hand. Which is technology dependent. So, all that I will control is threshold and w by l. And of course, power supply is also not in my hands by technology node someone say 1.2 volts supply that is the end of it.

But some extend therefore, control is only on the sizes, and also on the adjust. So, I want to create a model for gm r 0 many other things so that I will be able to control gm and r 0 so that I can attain a gain of my choice, that the design if I analyze analysis is so straightforward. But I want to know I want a gain of 10004, 10000 and above above means I do not mean how much, but 10000 minimum I want. So, what should I choose the values in a device so that when I interconnect on the chip that all circuit, it will give me a gain at least thousand 10000 or may be lower, lower or higher which are value we choose.

That is the difference between I keep saying between analysis and design. I am now want to know this value. Now I figure it out that that is not so straightforward, if I control something, I will figure out something I may lose. So, how to get optimal use or optimal parameters so that I get whatever everyone is asking. I can attain to a great extent that values, and that is what the design is all about.

So, if I had to create a equivalent circuit, or equivalent model for this, I must do something we are done in second year, but I will do little more detail here. That time you know you probably were not very deceptive, at least many of you I should I know about.

So now at least have word again. So, that you know that why these values are relevant for. For example, threshold they how do we control a threshold. Sometime that threshold control is beyond you, sometimes it is will well within you. The same technique which I am using for analog threshold control can be used even in the case of digital circuit, where will may probably do what called power low power circuits.

So, threshold control is a major area, where we actually look for design. At times technology forces you to do only this much. Then circuit wise what do I do if everything is fixed by technology then what do I design. So, there must be some circuit way of fooling a device or vice versa some may say so that we still have some leeway to design.

So, that is the aim of this course. We were looking for mos transistors. Already if a this is all n channel device. And we said that if V GS is positive and substantially higher, one can see from here it is going to say let us say, V DS is 0 and source is also grounded substrate is also grounded.

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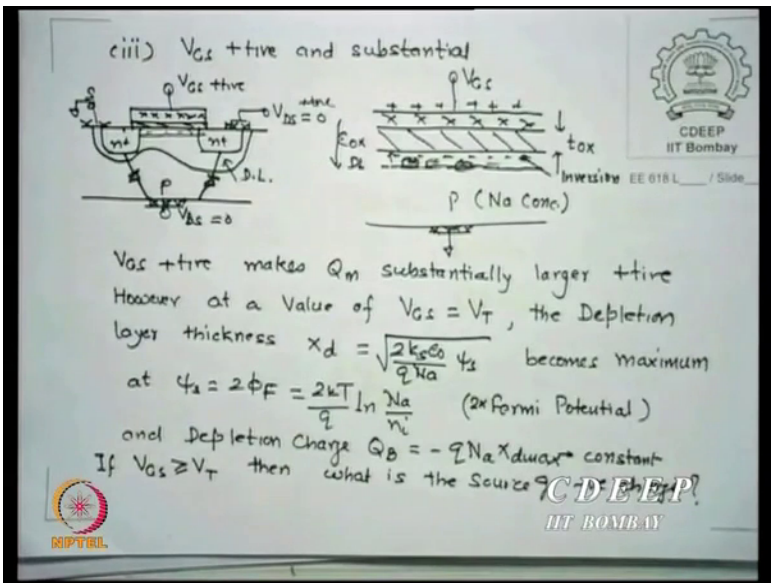

It is like a mos capacitor, which has the oxide thickness of t ox, which has a dielectric or permittivity of that dielectric is epsilon ox. And because we are applying V GS as we did

last time, initially there will be a depletion charge. Because we want to balance charge put on the metal plate, or gate plate. And this is positive gate voltage is applied you need negative charges to appears. So, first thing the holes move away, and you create a depletion there (Refer Time: 06:55) and I said last time; that this can continue infinitum, because that depletion thickness can keep on increasing.

But it does not occur because one figures out; that at certain value of threshold V GS equal to V T, the electric field in the depletion layer is large enough so that the whole electrons which are constantly generated everywhere including depletion layer, they get separated in the depletion layer. Because there is a electric field please remember poissons equation says D by dx is rho by epsilon. If there is no rho. So, there is no p is equal to n means no rho. So, r is constant of 0. Most cases the neutral regions are electric field assume 0. Whereas, in the depletion layer you have an electric field, and that can separate electrons and holes. At the point where it occurs, we say it is V GS is actually defined a threshold.

Now, this is what we said last time, and we say depletion layer width is proportional to the surface potential that is drop in the semiconductor surface. And one can see it is inversely proportional is the doping in the substrate. Where a size itself is a function of any size which is called fermi potential a surface potential, twice of fermi potentially given this expression.

So, we say if I had 2 phi F I already terminini, in xd I have another terminini. So, there are there is a transcendental equation. So, for a given any you can get a good charge equivalent of this you have to solve a quadratic sci kind of non-linear terms.

Now, we defined further, I mean this is what we said last time. If we continue to increase V GS, further above V T. Or we need more minus negative charges in the semiconductors, and now we say that depletion layer has already reached this maximum. And we said this of course, because now free electrons can be created, holes will still move down, but electrons can come to the surface which is called the inversion layer, because it is opposite of the substrate which we started with. Not going to too details of mos transistor mos capacitor theory, one can say V GS which is now equal to V T when threshold starts, the turn on thought it is 2 phi F which is the maximum surface potential

which we reach, which is twice the fermi level minus fermi energy 2 phi minus Q s which is semiconductor charge divided by C ox.

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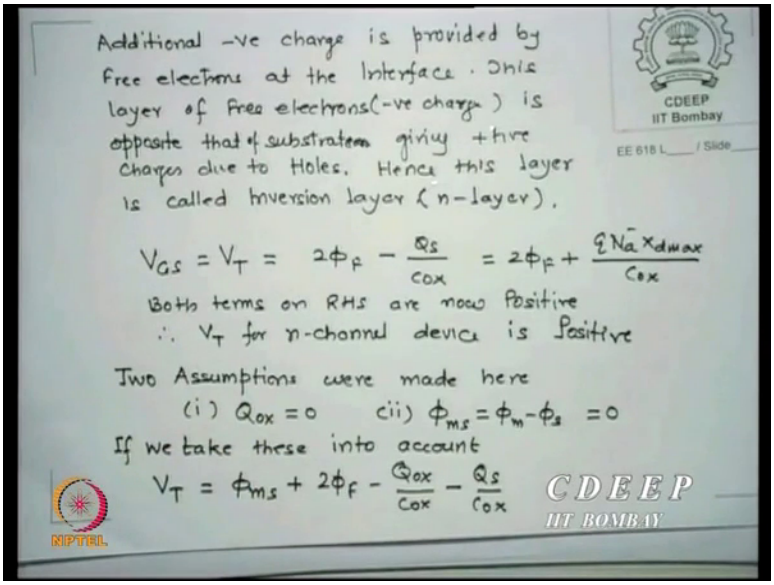

And this as I said it is same from the very simple relationship if you wish.

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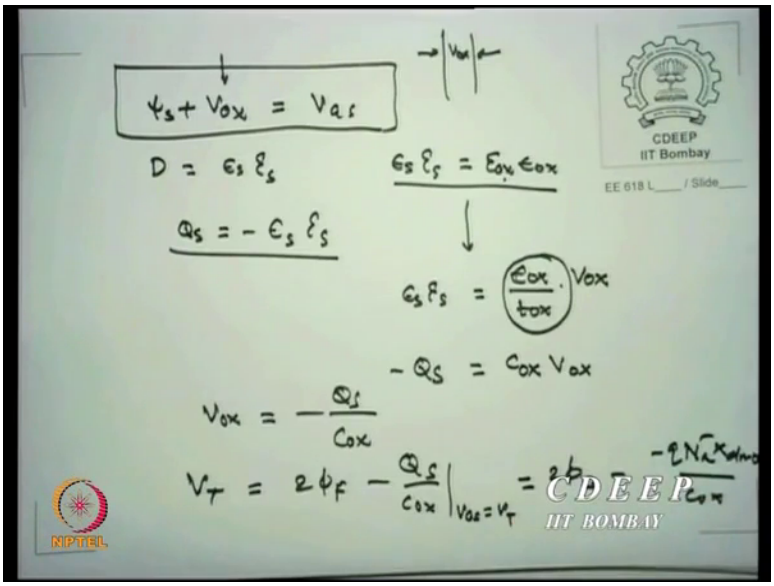

One can derive very fast not very accurately, but phi s plus V ox is equal to V GS.

Now, we know D is epsilon s Es these assuming the electric vector and we assume right now which is not very bad assumption, across the insulator and silicon D is continuous.

This is slightly vary some, essentially, I am saying epsilon E s is epsilon ox E ox the. EE for both is same that is the continuity of D vector along the semiconductor to oxide.

Once we assume this, we also know the charge in the semiconductor can be written as epsilon s capital E is the field and small E is the dielectric permittivity. So, the charge is minus epsilon s Es D is continuous over a one relation here and another relation here. Now I can say oh I can now start playing games. I say we from here this expression you can choose from here. I can write epsilon as s is equal to epsilon ox by t ox. Now this term from t ox is coming from here, because this E ox oxide voltage whatever you are seeing, the field across this is nothing but voltage divided by the thickness. So, this V ox by t ox is epsilon ox not epsilon E ox.

Now, this epsilon ox by t ox by capacitor theory is the oxide capacitance per unit area. So, this C ox is defined as oxide capacitance per unit area. So, C ox into V ox is minus Q s is that clear? Q s is by gauss's law is minus epsilon is s. So, I just substitute here. So, from here I get V ox is equal to minus Q s by cox.

So, what did I do that, this expression in which I know at threshold how much is psi s 2 phi f, and that I know because it is only function of na by na by n temperature. Na by ni ln of na by ni and to kt by Q twice of that it is twice kt by q. So, I know psi s. I know now via because if I know Q s which is the charge in the semiconductor charge density. Please remember this is all density per unit area. That is why this is per unit area this is per unit area. So, it is the voltage.

So, if I now have a term which is I know Q s directly otherwise. I know C ox anyway, because the oxide thickness I started with t ox. I know how much oxide thickness I have and therefore, I know the oxide capacitance. Is that clear? So, I know my V ox. Once I know my V ox, at V t one can therefore, say psi s is 2 phi F minus Q s by C ox at V GS equal to V T. This Q s at that time. So, at how much is Q s at the V and the inversion starts? Q na xd max is that correct? Q na with the minus sign because the negative charge.

So, we see this. So, at threshold voltage therefore, I have a 2 phi F term which is known to me I can calculate. And this is minus for n channel minus qna xd max by C ox. So, one can see from here every term is known from the device. Doping concentration is known from where you can calculate phi F I know phi f. So, I can calculate xd max because it is

a function of any na psi 2 phi f. So, I can calculate the Q s by C ox term, I know 2 phi f. So, I know my threshold. So, am I threshold, that is how I know threshold.

So, in this quantity is minus, and the sign here is minus, and 2 phi F as I say band bending down phi is positive. So, both terms are positive adding to each other. Which means threshold for n channel device is always positive; however, this statement is can be modified little later, but that is what we want threshold of an n channel device should be always positive. If it is 0 or negative, what does that mean? That the inversion has certain even at 0 bias. Because where threshold is lower. So, by the time you reach 0 world already in version has is already available. And that was one of the major worries in earlier technologies. We started with as I said earlier, we started with p circuit p device circuit for simple reason, because gating the other 2 terms which I will show you now we are. So, strongly to get you that the V T is to become net negative. And once that becomes then; that means, device is always on. In tain terms of device called depletion mode is already in the depleted situation.

Which means always on. So, you have to go minus higher voltage to switch it off. In a circuit we never wanted that to occur. We want on off particularly for digital for example. So, 0 to something is switch on, now that was not possible. So, we said look for p channels, in p channel this is negative. This value will become plus Q nd xd max. So, this will minus and will hold this will be minus, the other 2 terms are always minus. So, all the terms which you will get is minus V T. But p channel I want a minus V T. So, if there were situation those 2 terms which are minus only may add to minus value more. So, to turn on a device will require much higher minus voltage so that it crosses V T. That most possible because it is a 3 volt I may put 5-volt supply if 5 we done I will put 10-volt supply minus of that.

However, if I if I have a minus V T of for a p n channel, then I have a problem that I cannot done turn it on it normal ba biases, and that is why I say we started with. So, what are those 2 terms which caused so much worry for most of us. There are 2 assumptions we made so far, one is we said the are there are no charges in the oxide, which reality they are. There are charges very close to the interface. They are normally always positive. Normally, I am not I will not I am not go too detail on that. They are called fixed charges. And normally within 100 Armstrong from the interface. They are situated.

Now, take a situation in which you have a charge at the interface. What was the problem with us?

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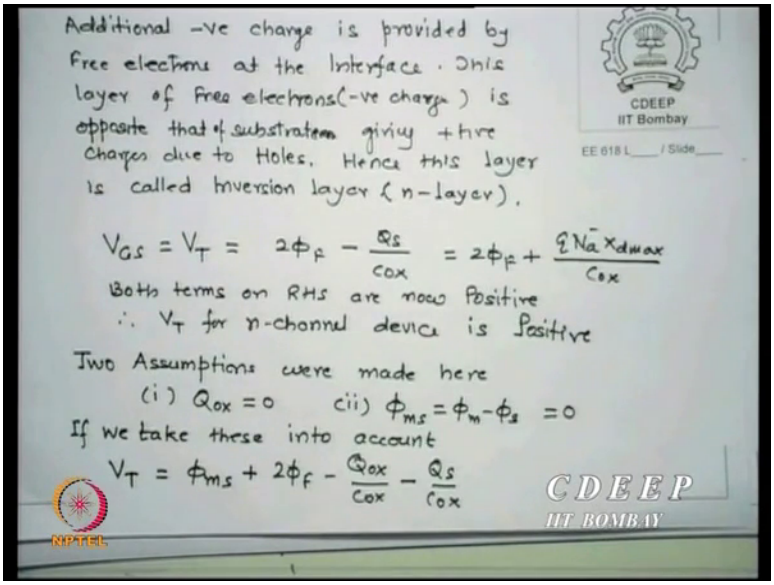

If I have a device, and this is my oxide and this is my semiconductor. Let us say positive charge occurs very close to the; this is oxide and this is semiconductor. What it will do? I have not applied bias, but this positive charges itself will now expect negative charges to appear in semiconductor to balance the charge neutrality; that means, anywhere by V GS what we are going to create? Negative charge. So, even without V GS I have some charge already available. Is that clear to you? Already there are charges available to you.

Similar thing happened if you have a metal. This is your metal; our assumption is between metal and silicon the work functions are same. Work functions means the energy taken for electron to leave the material is called it is work function. We assume initially phi m is same as phi s, but in reality, the material will have different phi ms. For example, if you put aluminum as the gate, aluminum has a 4.2 electron volts as phi m; where semiconductor is typically 5.2 minus phi s phi F values will just around phi E B for example.

So, this means phi ms phi m minus phi s it is negative quantity for aluminum. Even with the silicon gate which we use poly gates as we say, the polarity of poly and the dope substrate will be opposite. So, there will be again difference between phi m and phi s which essentially means it is normally and normally depends on the metal use there

something you use, phi ms is always negative; that means, if phi ms is negative it also want something additional already available to you, semiconductor is already having some negative charges already sitting there, we also have positive charge which also is already created this.

So, normally how do we measure? Equivalent level. So, we say apply additional as if this voltage, so that the equilibrium is that in fermi level on both side seats are equal. This is called flood band. And from there we now say in inversion can be sitting, but that is this additional voltage was already, already charges were available, that much you would not need now actually. This is already present with you without worry.

Now, the problem is this is giving you negative, both values on negative charges, and you are going to create some negative charges due to V GS, but these charges may be sufficient for the inversion to be there, which essentially means that the device is pre-at 0 itself at it is inversion. This essentially is the worry which means the V T of n channel transfer could be fully negative 2 terms were positive, but these 2 next 2 terms which I will now show you, may be strongly negative compared to these 2 positive terms. And here is that expression I am talking about, this is my 2 phi F Q s cox is what normal V T would have been, but 2 assumption I made Q ox is 0 which is not 0. And phi ms is 0 which is also non-0. So, if I add these 2 terms without going to details of band diagrams. Because some other days specific someone wants come to me, I will explain you mos theory even much more in detail.

So, why we say they, because that is our braided mos transistor we have been working for 25 years or 30 years or maybe more 35 years. So, I have for us it is very trivial to understand what is going on. But for you it may be interesting some of you not all of you. V T is equal to phi ms plus 2 phi F minus Q ox by C ox, this relation comes from the fact or you can see from here why did does it; total charge initially was 0, but if there are oxide charges, this is the new equation charge neutrality.

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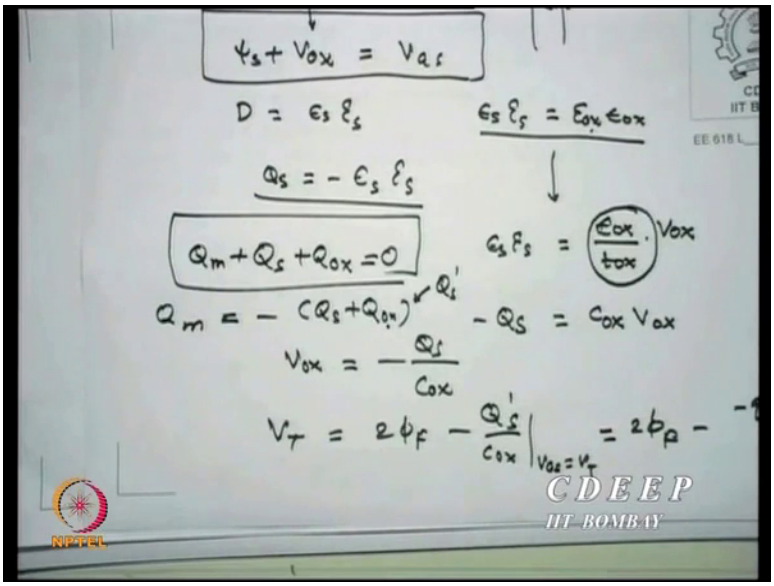

If that occurs, we can say Q m is minus Q s plus Q ox. And this I call say this is fixed I call it Q s dash. And then I substitute here Q s dash, because that is a constant value. Q ox is always fixed from the technology. Positive always known to me how much.

If that is so, I will get additional term of minus Q ox by cox here. Now this is negative, please remember in the expression this term is coming negative. This is positive, this is negative. This is positive because, minus Q na. So, this is, but these 2 term may offset these 2 positive terms. This has happened because initially when technology started in 16th's the Q ox was extremely high in the process we made. It was of the order of what we say 10 to power 12 per centimeter square as the density multiplied by charge it will eluvium per centimeter square. So, it was a very, very high charge density was available in the interface. So, whatever we do for n channel, it will always be on irrespect to what we do.

Now, we figured out in 20 years 50 years down then, that I can control Q ox by technology details. I can do something which will reduce my Q ox. Now I can do a Q ox of 10 to power 10 per centimeter square into Q of course. Which means this term will very small, and in which case this may not be strongly negative. Of course, this I cannot play much, this is a inbuilt gate whatever I create. But this stronger term may become smaller and then the net value may become positive.

Now, one catch from all this, if I want to increase V T with a given Q ox and phi ms, what is the term I should improve on so that the V T goes higher? That is the circuit requirement. From here expression can you chick check what should I increase in a the doping in the substrate if I enhance, I will be able to enhance the threshold voltage. That is the control that word which I say control, I can do some technology control now and say boost the na. It may have something else a problem. So, I will selectively boost the na wherever I want, that is in the channel only I have higher doping substrate I do not have; which I can selectively dope the device.

So, the way thresholds could be adjusted, also you can have very interesting thing you can have 2 areas or 2 separate transistor may have a different dopings, and we have a multiple V ts on the circuit itself. So, tomorrow you design a good analog block or a digital block, and you expect variable V ts technologically it is called additional mask, extra one mask is typically cost around one million dollars on process.

So, you say one mask one million dollar. Another V T is 30 one another mask for just for that another million dollars. Typically, 24 masks are required for making a good chip at cmos chip or an equivalent of the chip. Now you add this as now I saw new technologies are coming and many controls are being given, you may require 34 masks. So now, remember how much money per mask you are adding that as to the chip cost.

So, what intel pentium 4 initially was sold maybe one forty dollars, or now they may sell it 200 dollar, because now I have improved something which is multiple something I am giving you which can control your power requirements. So, all technologies costumes of course, if you make millions and trillions that cost may actually go down, that is what the whole game in the circuits are.

So, is that clear? So, the basic idea of a mos transistor V T control is to control alternatively, you can also control it from C ox or t ox, but t ox is not very much in mind it is a technology dependence. When you I say 90 nanometer should have so much thickness of oxide point to phi should have so much; I mean that is it (Refer Time: 25:20). So, I am not very much within my this. But if I see C there is a absolvent term going on. So, I can need not were consider silicon dioxide, I may look for other dielectric with higher episolons. And in that case high k dielectrics actually came up.

So, they are their own problems. So, in general, a typical capacitance voltage characteristics of a mos t capacitor look something like this. This is for n channel device. What does please remember p substrate always gives you n channel device. N substrate will give you p channel device. So, this is n channel device means p substrate device.

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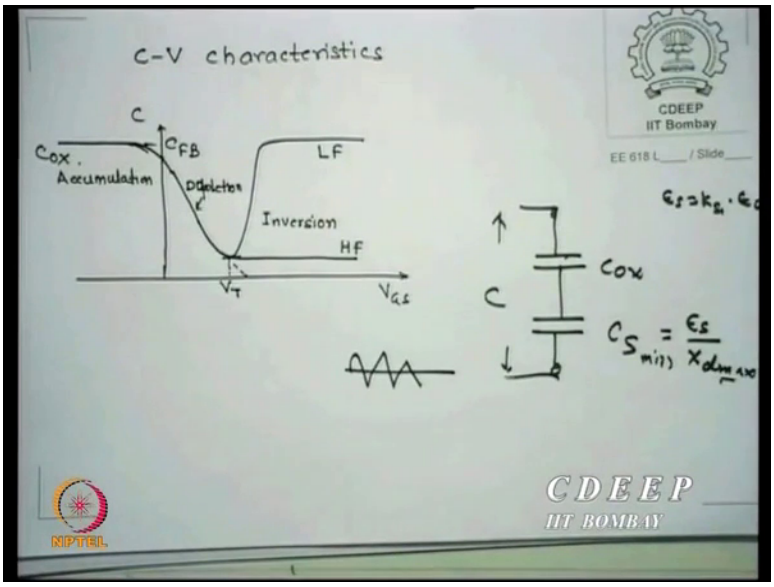

So, we apply what is the threshold for p channel n channel device, positive. We assume right now that Q ox and these are small enough. So, they still shown V T. So, if I have a V GS negative, since there is a accumulation you can see in accumulation, there are plus charges and there is a metal charge plus. So, it is a good m I m capacitor metal insulator larger charges means equivalent metal. So, you have a metal insulator metal.

So, fantastic capacitance scheme. So, you say C ox is the only capacitance available when you are in accumulation; however, a phi star increasing V GS towards positive. Somewhere down I said as you cross 0, V GS becomes positive depletion starts the depletion layer starts, and you start getting negative charges due to depletion.

Now, what can you see, you have already seen that figure which is a capacitive figure, you can see from here, this is metal. This is silicon sorry, this is metal this is oxide. This is the inversion layer, and also there are acceptors here is. Now this has 2 capacitance now. One due to the oxide, and one due to the semiconductor, semiconductor charge means it is equivalent of a capacitance there. And you see they are in cs. So, what we say therefore, it is like saying you have a C ox in series with s, which is semiconductor

capacitance. So, after V GS becomes positive, there is a semiconductor capacitance which is essentially how much? Epsilon x by x t. This is k s epsilon naught; k s is the dielectric constant, epsilon 0 is free space permittivity. So, this is that. Please remember epsilon is k silicon and to epsilon 0 silicon dielectric constant of silicon dioxide is 3.9. So, epsilon s is known to me. Because this is 8.85 for 10 to power minus 14 (Refer Time: 28:14) per centimeter.

So, I know now this is series in compared to C ox. What will happen if you have a series capacitance? The net capacitance seen between these 2 node will what will be it will decrease you are in series. As you increase V GS xd increases Cs decreases. So, what will happen to the net series? C further goes down, C further goes down, because Cs is started going towards smaller value. As this reaches maximum to a reach Cs minimum now you cannot have further depletion layers, xd max has reached.

Now, the net capacitance is C ox in series with Cs minimum. Where this will occur this xd max when the threshold occurs. So, if I keep increasing V GS, somewhere at V GS is equal to V T I reach Cs minimum. So, the net capacitance then becomes constant. Now this is slightly catch I showed you 2 curves, one shows constant. The other shows, it goes back to higher value of it is original C ox. This is essentially because of the frequency of measure; how do I measure a capacitance? I apply a current source or a voltage source through a resistor, and pass current through a capacitor. So, what is the current through a capacitor? C dV by dt is the current rj omega C times V is the current in the capacitance. If I know my omega, and I measure the impedance on a impedance bridge, and I know what currents I am voltage or current, I am pushing then I will be able to evaluate the capacitance. Assuming rs are practically 0.

Once I know 0, but then that omega term appeared there; that means, the frequency at which I am monitoring, will give me the impedance. If omega is very small 2 phi F, then I am in the low frequency zone, if I omega is megahertz tens of megahertz or 100 and above I say I am in high frequency reach.

Now, why this at high frequency what happens, when I apply higher frequency, basically what I am doing I have a DC over which I am superposing

Student: AC.

AC, if the frequency of AC is this; whatever this capacitor here I was monitoring, I must say that the depletion charge must vary with the frequency because you are going to plus minus. At much higher frequency depletion charge cannot follow that. Is that clear to you?

Student: No

So, it shows constant value.

Student: (Refer Time: 31:03)

But at where very low frequencies, it has time constants available enough that it also modifies. So, the average value of capacitors now starts increasing I, I increase V GS, and it is maximum V GS, it shows as if it can follow anything like one herd if I do it will go back to it is original value, more details other books.

So, the idea is I can measure for a given technology a mos capacitance at high frequencies or low frequency, together is individually otherwise that is what all that all that my other colleagues in the so-called device area only thing of course, should not say only major thing they measure is a cv measurement, and keep telling we did great assist. This is all that we do keep measuring CVS.

At the end for the circuit, what I am really looking for equivalent circuit. I am not interested as I say yeah, I this theory I did find I, why it satisfied my ego oh I understood. But for a circuit how does it matter it only wants equivalent put it what you want to equivalent of that. So, we figured out in a mos transistor shown here, just for the sake of forget about this figure right now. You can write down this expression.

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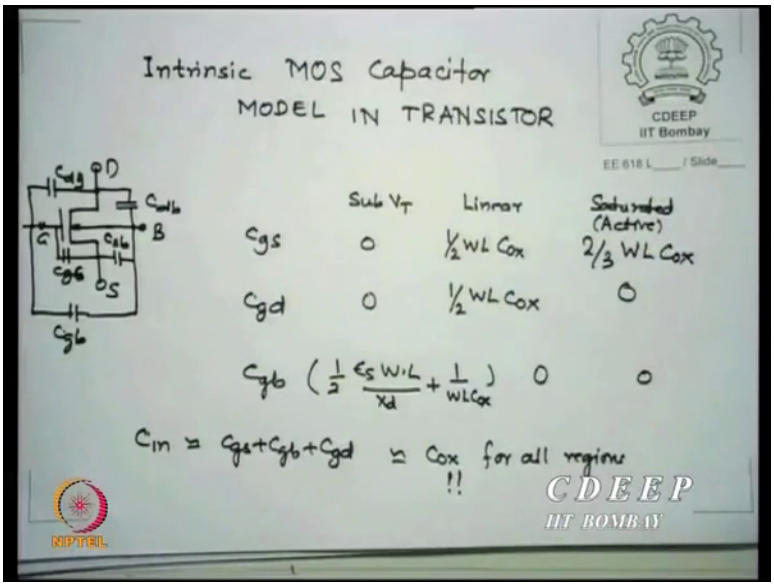


There are 3 capacitances of interest at the input side, which are the 3? One is gate to the bulk, which is called C gb, gate to the bulk, but means substrate. There is a capacitance between gate to the source. So, we call that is C gs.

Now, you say from where this is coming, if you see the expressions, this mos transistor just a minute before I will come back; you can see from here there is a depletion layer here. So, there is a diode sitting here. There is a diode sitting here. Diode has a capacitance, and the reverse by both are reverse bias anyway. So, diodes have capacitances source to bulk.

Which side is a higher capacitance?

Student: (Refer Time: 33:10)

No drain side has a larger depletion layer. So, smaller capacitor. But smaller capacitance have more difficulty then they have larger capacitance, if they come in parallel or in series depends how do they come.

Now, there is the capacitance of from the gate to the bulk, but if there is a channel bulk is screen because then they are only small r in series to that, is that correct? So, the C gb is 0 if there is a channel existing. Once channel exists, the bulk is screen; that means, there is no connection with the capacitance. Is that clear? So, these otherwise if there is a short channel here there will be a capacitance here, oxide capacitance and also bulk capacitor.

So, these are the capacitances associated with. Now what we do here? Which is what the trick we are saying, in a mos transistor in fact, if you see all positions have different capacitances. We will see later. The channel does not have same thicknesses. So, the voltages across every point is different. So, essentially, we saying we are n capacitance going from source to drain or in parallel.

So, what is the model we can do for a circuit? We say lump it out. Half this side, half this side. And remove there distributed something solving is a difficult task it is like a transmission line theory rc rc network solving here I say use lumped models. So, there is the catch word I am using. Analog circuit design essentially users lumped models, is that clear? As all the word derivations which we will do later are essentially assuming that lumped models are valid. Once you say lumped models are not valid, we said this is the highest frequency you can use. Because for the design you can only do this much. That frequency we want to know up to where my circuit will function. You know, I then I have to find out my analog circuit will function at one megahertz 100 megahertz gigahertz, where is that cutoff which I have?

Now, that frequency is essentially decided about up to which frequency by the device you can have lump model model equivalently fitting the experiments. This is the basic understanding we use. So, beyond that not that one cannot solve, but we will have to do something transmission line theories like we do in microwaves, and probably one can solve a more microwave involved problem the using fields, but field theory is not. So, trivial third year people who have heard it must be doing about it. It is not very easy to pick up the fundas unless you know very well what is divergence and curl in a better fashion. And to get that field has to be there. So, a we will say we will use only up to lumped circuits, and we will be safe in all our analysis, is that clear to you? Is that point clear? How do we increase that frequency, maybe we will see we can I increase this cutoff to a higher level higher low how much higher I can go can I go to 100 gigahertz possibly yes possibility no. So, you will see that.

So, my issue is that I must know my capacitances, because if you see my earlier circuit; which is that equivalent circuit I drew for you first day first point. Where is that? Maybe, if I have now a capacitor here, a capacitor here and many other capacitances, then I have a problem because circuit has a feedback. Circuit is connect some input cannot be going beyond certain impedance as shown here; that means, the limitation of the frequency will

appear as soon as I get actual capacitance in the circuit. And that is what I want to know, how much is the maximum frequency I can have so that I can operate my amplifier oscillator, whatever circuit I want at those frequency.

Now, this capacitances is what we are trying to figure it out how much are they of course, what I am showing here can be useful for even the digital course who have taking really say design course there this is same. It does not matter here or there. So, we are 3 possibilities C gs C gd and C gb. Now C gs which is gate to source capacitance, there are 3 regions of operation. What is sub V T?

Student: (Refer Time: 37:49)

It is phi F is still there, but not 0. But assuming right now that inversion is so small practically we are not assuming as if there. So, we say sub V T capacitance is 0. Which capacitance will if there is no channel? What is the capacitance say between gate and the bulk? So, C gb exists, but C gs and C gd does not exist because there is no inversion at the either ends. So, we say C gs is 0 C gd is 0, this additional term which I shown here is it that partial depletion layer which was coming there, even at 0 bias is taken care and this is our oxide capacitance, is that correct?

Now, if you see the linear. What does that linear? We are not desktop, but in which that V GS minus V T is less than V ds assume right now, that is called linear mood, in which case we can now lump it half C g half oxide capacitance to the source, and half to the drain. And then we say there is no C gb because channel exists both. So, screened out.

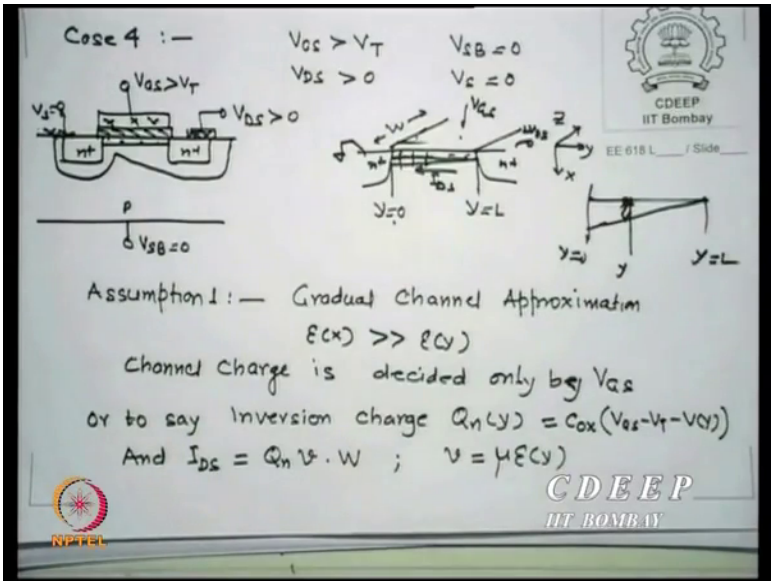
However, when the device is active mode or what we are interested in all those theory which we call saturated mode, they are just we will come to it soon. Now at that time it is a trapezoid of the channel and therefore, we say it is 2 third area into oxide capacitance. Since the channel is cor up to corner to this, the bulk is screen drain there is no charge left there. So, this is also screened. So, only capacitance available is c.

So, in general what we do is for a general purpose, irrespective where the device is operating. We add all these capacitors at the in a DC case. If that occurs, you can see if you add any term which is very close to C ox. This is 2 third. So, maybe one third plus. And so, C ox is upper value of that. This also will give upper sorry, this is I think minus sign you just check.

So, essentially if I use only C ox, I may not be over I may be over estimating; that means, my frequency actually will go down than what I expected really may happen, but I am safe so many a times. The first design goes with C ox said fine, thank you very much. Otherwise if you are solving on a computer, how does it matter if the circuit is given all the specifications and all the values. So, it will calculate and substitute every voltage whatever is happening, and use that capacitance at that point.

So, in numerical analysis I do not do any assumptions. I said this is the solution, you solve, in the case of analytical I have worry because every time then I will have to remember or add correctly. So, I want to make some simpler assumptions. Not that I may use this also, but I am just trying to so many books will say they are using everywhere C ox. The reason why they are using is because of the assumption is that little over estimation, but fair enough.

(Refer Slide Time: 41:07)



Student: Sir (Refer Time: 41:06).

Let us quickly finish up the device part so that we will actually go on the major issue of our interest, but as I say why I am showing a device, because I want to show you those parameters, which process and design is required I mean which design parameters. From where they can be controlled, because that is why I know want to know the theory. Otherwise for me expression is good enough spice maybe there are versions we will only

give you the first version. Why we are doing that? Because they are the problems which we may give, will be only simulation problems and you must run spice.

Essentially spice solves a small network. What is it solves? I is equal to g times, we were all 3 are matrix. Is that correct? That is all that it does. Now this gs could be voltage dependent current dependent. So, that non-linearity certainly comes. Larger the parameter matrix may become bigger larger circuit may have of so many nodes to solve. So, the complexity of matrix solving may increase because of the non-linearity terms, and because of the larger sizes, is that clear? But basic idea is Kirchhoff's law g in to V is I, is that clear? So that is what spice does.

Now, what is g? You must know device parameters, you must give so that it can calculate dependent sources for the; So, it means data from the device it means data from the connectivity from which node to what node what component you are putting. Once it knows the circuit, it just does g is equal to V. And you can calculate V or I any position, any mesh, that is essentially spice. What is spice stand for? Spice.

Student: (Refer Time: 43:02) word.

Simulate.

Student: (Refer Time: 43:07)

Simulation program, s spice, I c integrated circuit, E emphasis. This program was written by Barkley group headed by brussels newton. Unfortunately, he is no more.

Student: (Refer Time: 43:25)

He was the provost of not provost, he was the president of Berkeley some time. And his group has written this programs spice, now all industries actually working on spice, but they are modified model they are modified few things and then keep telling oh this is our mind; thus, I am mentor graphic as his own spice some other specter basic spice.

Reason is in if I have a what we used to call a small routine, I am a block that routine for anyone else. So, I am a still none spice there, for outsider you say I do not know. What is program? I run there you know, I just call from somewhere run that. So, everyone is using spice is one way or the other, h spice you know just came with some other name,

because they say it is it takes care of both high power and highest frequencies s spice. Some better models they put, but basic idea is g V is equal to I and nothing more than that. Is that clear? So, do not get too much worried, and it is best thing to happen because then you can listen music, and you can talk people things you will be done by someone else for you. So, it is good.

Quickly we find out the current, because at the end of the day for a circuit person, I want to know given a voltage on the device, what is the current I am going to get. Because that is what my model is asking what is g? So, I say I must find the relationship between currents and voltages. If I get that expression some way I will convert into equivalent source, and if I do that I my job is over.

So, I figure out what is the mos transistor doing, if phi gs is greater than V T on n channel device, V SB 0 source is 0, and I am applying positive V DS, and applying positive V GS greater than threshold. Now there can be 2 possibilities, of course, but first we say V GS is large enough. V GS is large enough, and V DS is relatively smaller. Please remember, once V GS is greater than a channel may exist in the substance. As soon as channel exists, the one shown here this is source this is drain. How it does it look? This is an n plus area this is n plus area, this I am applying plus V DS small enough, but and this I am grounding. What does it look like? A semiconductor bar with voltage V DS on one side and ground with the other. So, it is like a resistor a small resistor.

Since it is like a resistor which law I am following.

Student: Ohms law.

Ohms law or drift current only flows j sigma E is the equation of drift currents. Sigma essentially is conductivity, which is related to resistance. Since ohms law has to be followed, now I must know what is r, because if V I know and I want to know I. So, I must know V by r, r is what I calculate for this device. This is what all that we do when we solve it.

So, the first assumption we make there are 3 electric fields or other 2 strongly feel electric fields, let us say this direction downward is x across the channel is y, and along the third-dimension plan dimension it is a z. This is the axis I used. So, you can see from

here, if this is x there is a electric field downwards positive V GS, which is I called is E x across off side.

Because there is a current in the channel, there is a voltage means there is a electric field this be divided by lengths equivalently not (Refer Time: 47:11). So, there is a E y and there is E x. So, the first assumption I make, E x is much greater than E y, which is called gradual channel approximation. We can remove that. What is essentially telling that the electrons available in the channel are essentially governed by the gate, and no one. Is that clear? Control nowhere else. So, gate is controlling the charge, is that clear? So, this essentially says E x is stronger than this. So, this control the charge. That is what gradual channel approximation is all about.

Or to see the inversion charge is; what is it charge densities capacitance per unit area into voltage. So, if you see it what is the capacitance here? C ox. Just as (Refer Time: 48:04) what is the voltage you can see from any point here? I applied a V GS here. Current is flowing in this electrons are going in this. So, current is going in this direction. R ds into source. Since this is a resistor, what does that mean? At every point of the channel that is from y is equal to 0 y is equal up to y is equal to l. There is a voltage drop, what is the net voltage drop at L V DS which I applied? But at the source 0 from 0 to V DS there is a voltage drop everywhere, is that correct?

So, if I take a channel, let us say this is my channel. And at any point here y, this is my y is equal to 0, and this is my y is equal to L at any point on the channel, I use an element of the channel B x as such, and then I say if I can calculate the resistance here. By rho L by a expression, and then integrate it out across the channel length, across the x both side. I take a piece and I actually integrate on x side and integrate on y side, to get the net equivalent average resistance, and I is equal to V by r, that is what I am doing.

So, I figured out the charge density is V GS if I apply V GS, minus V T because that is required for inversion. Minus V y because at every point now substrate is equivalently saying at py. In normal case of capacitance substrate was grounded. Now at the lower side of the voltage is potential there. So, what is the voltage across the oxide now, V GS minus V T minus V y multiplied by capacitance per unit area will give me the charge density available if electrons in the channel below, is that clear?

Now, this is an approximation. More accurate expressions can be done, but we just see. We also know from the very simple electrostatic law electro metallic electrostatic laws.

Student: (Refer Time: 50:18)

The current in a resistor essentially is 2 times velocity times the width. But the width come because, as if you are a number of such channels and you have to add all of them. So, multiplied by w assuming that is constant; that means, this w is uniform throughout. So, if I do that I have a Q v w is the this is charge per unit area, please remember. What is the velocity there? Mobility times the electric field, is that correct? I have a drain current which is charge density electron charge density into velocity and velocity is essentially mu E y into width of the channel. Better expressions can be derived, but just to take from this.

So, if you now know I DS if I know my Q n which is here, I assume now mu is constant. But in reality mu is also non-constant. So, we have to take care of mu variations. E y how much is E y? 0 to L it go from 0 to V ds, how much is the voltage across channel?

Student: (Refer Time: 51:26)

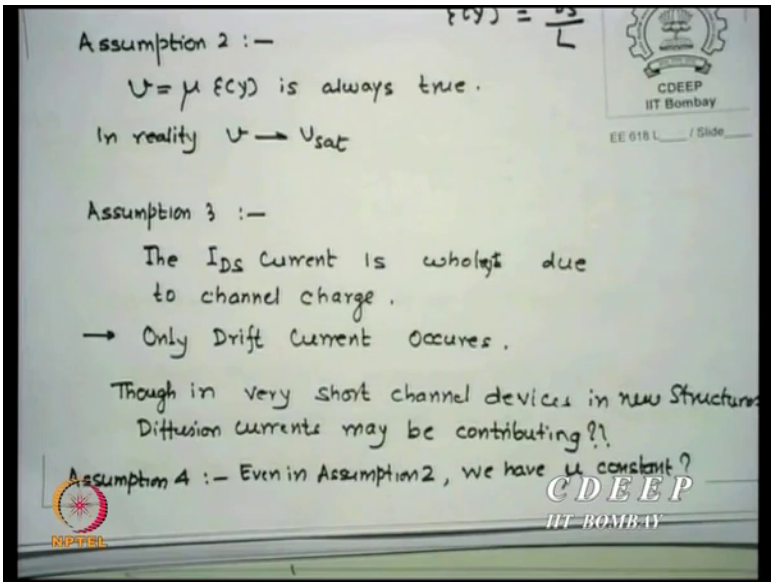
As the length goes from 0 to L, voltage goes from 0 to

Student: (Refer Time: 51:30)

V dd V DS, is that correct? So, if I integrate these 2 terms which I am going to, then I will get net average I is equal to I DS equal to average resistance multiplied equal to voltage across that. This is what I will do.

The second assumption which I made which I said V is equal to mu is constan[t] is always available, but that is not true. Because if E increases too much the velocity starts becoming constant. So, right now my assumption is V is not reaching vz which means actually. So, there is another assumption I made, first assumption what did I made, E x is much stronger than E y, second, I made assumption velocity is still not saturated. Which what does when this can occur, what is the electric field?

(Refer Slide Time: 52:24)



Student: (Refer Time: 52:23).

Is V DS divided by length. So, when E y will be smaller? Either the V DS is smaller or

Student: L.

L is larger. Larger channel channeling devices called long channel devices. So, in a long channel devices this assumption is good enough we say velocity does not saturate. What is the new problem will now come? As you go for smaller and smaller dimensions, the velocity will become saturated day one. And that is our worrisome part as you come to the models.

Third assumption I made which is also an assumption. That net current in the channel is essentially drift current; that means, that is the only current I have. Which is the other possible current in a semiconductor.

Student: Diffusion.

Diffusion current, but I say there is no diffusion current. There is no gradient though there is, but that current is say million times smaller than other I say there is nothing there. So, the third assumption only drift current occurs. This is also an assumption in real devices if you are doing a device simulation projects or something you can get rid of

all such assumptions and get exact values. But to a great surprise you will find, it does not give the exact experimental result in spite of great modeling.

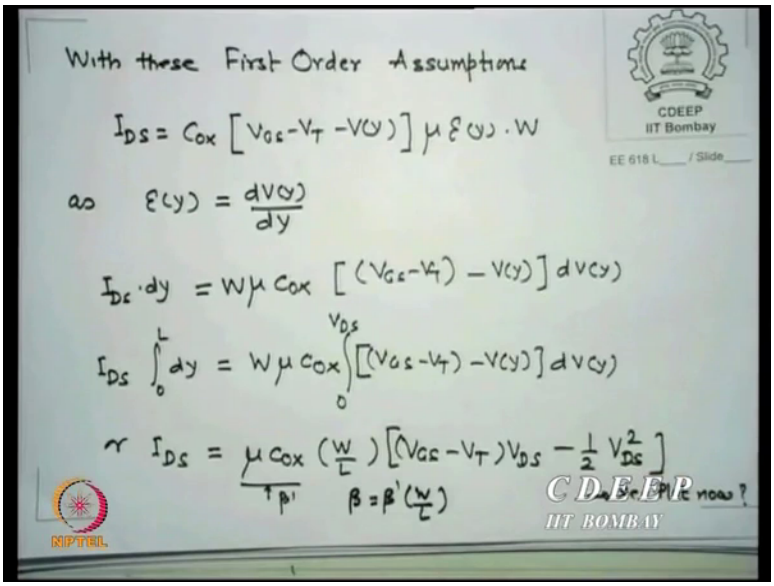
Then finally, what to do you try to fit some parameters which fits into experiment. Once you start fitting then hole physics is lost. So, physics and fitting do not go together, but what do I do it? I still want to retain my physics. So, I add constants to it may be less than one my or exponential some term, which is say constant you see. So, it is called fit constant fit functions.

So, keep physics with some fit functions, weightage. And then you say oh it fitted my physics also it is good, my you are just trying to fool yourself by why choose the same physics? You could I written alpha 0 plus alpha 1 x plus alpha 2 x, polynomial 100 k by fit, alpha adjust. Constant spice what does it is do? The model as you scale down technologies it changes it is constants. Fitting functions, because experimental given technology is known to you. So, you try to come closer to it and you say look, I have got exact physics exact fits. This is game all device simulation people including deeply.

As I say I already said new structures, and new smaller devices diffusion current may not be as small. Though we do tricks so that it becomes smaller. There are other assumption, I mean we assume as I said mu is constant when in real life mobility varies with electric fields. So, even mobility is not very much constant function of y it is a function of x also.

X it comes from what we call the interface state density right now we will not going to. So, mu is not even a constant, but all these assumptions when you make and get I DS V DS characters what do we call? Textbook model, which probably and then the actual model, what will be give fit k 1 k 2 something so that it fits to the reality. So, as I look this expression I am still using nah that is the game all spice models people do including us.

(Refer Slide Time: 55:55)



So, if I have now substitute using first our assumptions I write E y is dV by dy electric field is slope of voltage V y I substitute in this expression which I wrote. I write I DS dys w mu C ox V GS minus V T minus V y dV by y changes from wall where 0 to L V y varies from at; so, 0 voltage a drain V DS I integrate from 0 to L to 0 to V DS, and I get this expression. I DS is mu C ox w by L bracketed V GS minus V T V DS minus half V DS square. This is the simple integral of this.

What is it trying to say? These constant that is why it has come out before integral. I also assume as I say V T constant, which may not be V T is a constant value. So, I just in differential integral I did not use that I said V T is known in really even that may not be constant.

Now, this in my analysis, analytical nc, I use mu cox term I call it beta dash is that correct and this beta dash, into w by L. I call beta. Which is like telling I know bipolar transistor used to have a gain factor. So, this is equivalent of a gain factor. So, I may use in my final expressions betas, beta dash is mu cox and beta is beta dash into w by L. This is my writing, it is not necessary you can keep writing mu cox w by L everywhere and fair enough. This is just to reduce the size of the expressions, I write is that I repeat how did I do it? I wrote Q vw as my grunt. I know V is mu v. So, an E I had substituted dV by dy, then I figure it out I can integrate this from 0 to length, because that is what the

resistance blocks are. So, I just submit them all, and once I sum them all I get this relationship.

Now, the trick worrisome part is now after you write down this expression, you will find if I really plot this I DS versus V DS characteristics, and I am some funny characteristics I suddenly see. Now the fun starts here, if I plot this expression I DS, this expression for all values of V DS. I figure out initially you can see from here if V DS is smaller initially, this term is small and I DS is proportional to V DS. If V DS is smaller please remember, half V DS squared term is smaller neglected. So, I DS is beta times V GS minus V t. And if V GS is fixed by me I DS is proportional to V DS. That is why it is called linear mode. I DS is proportional to V DS. What is the condition? V GS minus V T is much larger compared to V DS and therefore, this term is neglected.

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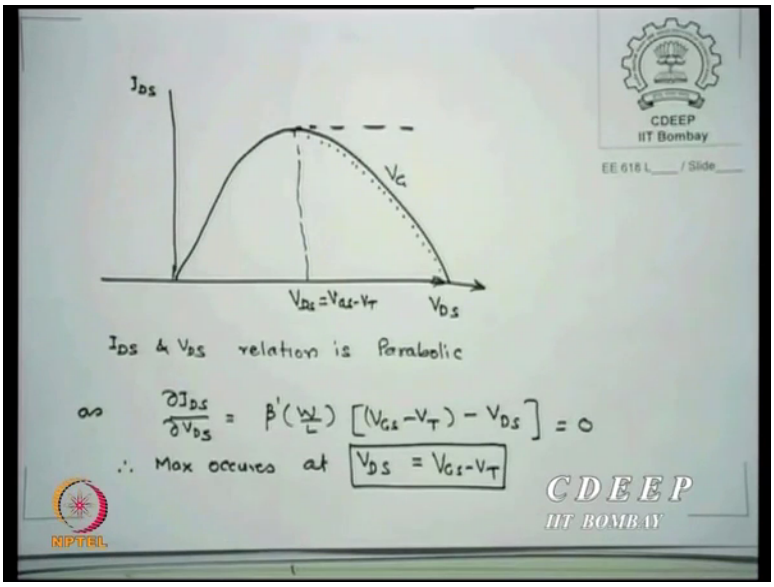

However, this assumption does not go. And I keep increasing V DS, that expression now says as V DS starts increasing, the currents are decreasing, because minus half V DS square term start increasing, is that correct? And at some this V DS actually I DS is 0. It is going down. So, it looked parabola because that expression is half square, I mean parabolic. So, it shows a parabola.

But in real life no one has seen that beyond certain voltage current suddenly dropping down; that means, current remains constant people have seen that expressions characteristic. So, what has happened? So, we say in real life, if there is something has to

happen like this; the this point I must know, where this can start. So, I said what is the maximum value up to which current is still one directional. So, I differentiate this equated to 0, and I get V DS equal to V GS minus V T at the point, beyond which the current will fall.

So, there must be something related to this point V GS minus V T equal to V DS is the issue, at this point onwards something else is happening. Certainly, linearity is not there, and no other term going higher negative so that current goes down.

Now, what is beyond then this value? Beyond this V GS minus V T first further increase V ds, I do not get this. So, the theory is something which is what device is very interesting part is that (Refer Time: 60:55) clear? In reality I had never see going down, but the expression shows it should go down. It does not. So, what could I happen at this voltage beyond?

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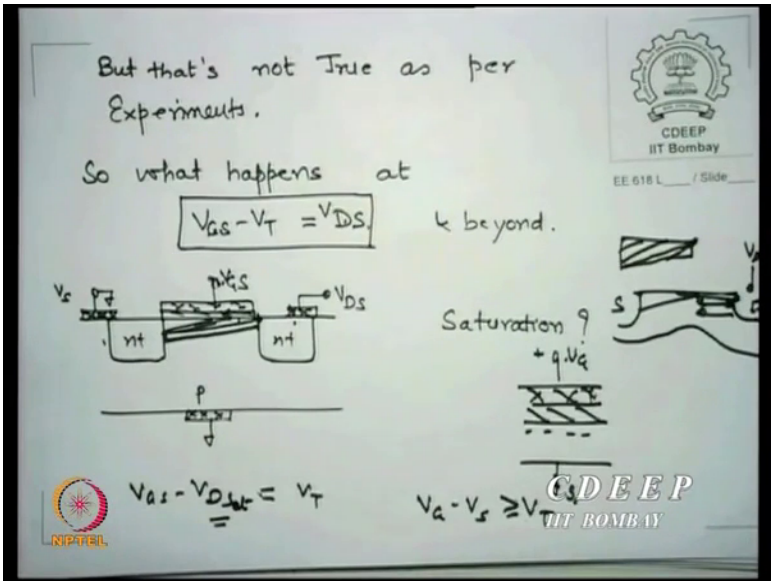

Now, this voltage is very crucial as if you see when the threshold occurs in a capacitor if you see a you have a capacitor. This is your metal. This is your substrate. What is happening? V G minus V s is the voltage across oxide. This should be greater than V T to have inversion or for plus or minus, whatever if it is plus and I want inversion to occur here, is that clear? This is always defined it.

Essentially now saying if V G minus V s is less than V T, there is no channel. Is that correct? That is what capacitor theory says. So, look at this transistor. If you increase V DS beyond V GS minus V T or at that point when V GS minus V T is equal to V DS, what does this value essentially saying? This is V GS, this is V DS. Is that correct? This is 0. So, all voltages are measured from 0 V GS as well as V DS. So, V G minus V D is nothing but V GS minus V DS, is that correct? Because sources down there. V G minus V D is same as V GS minus V DS. So, if I use this expression V GS minus V DS, this is at this point is occurring, is that correct? If now V DS increases beyond this point, what will happen? This quantity will become minus. So, there is no inversion possible. So, just beyond this point V GS minus V T is equal to V D, V DS beyond this value V DS increase there is no inversion at that end.

So, you what you see here, there is no inversion when V DS which s V GS minus V T value. Please remember source is grounded, is that clear? Gate voltage you are in fixed very high, but higher than V T. So, at the source there always will be channel. Because V GS is always greater than V T that is we started with. So, source will have a channel all through, but at the drain end at the point when V DS becomes V GS minus V T, channel is not existing at that point is called pinch off. So, channel is pinched off.

But since V y is varying along this point. So, V GS minus V y is decreasing along this line; which means the number of electron density available in the channel will keep on changing as you move from source to drain. Larger here because the maximum potential is given by you V G minus 0, is that clear? In between smaller smaller at the end it may become 0, which essentially means the channel thickness will be maximum at the source and will keep on decreasing towards drain end.

Normal in case of channel existing throughout, even then it will be something called trapezoidal sorry it is a trapezoid, but if you further increase it may actually pinch at the other end, and it may become triangular. So, initial trapezoidal channel will become then triangular, is that correct? This point we call device now enters saturation. At this point; that means, V DS greater than V GS minus V T device is entering saturation.

So, what does that means? In the case of bipolar I do not know how many are still recollect, when I say a I C V c characteristics and I say devices in saturation mode, what does there means? Actually, V c is very small in a saturation. The reason we say both

junctions are forward biased, I C become maximum. So, we say this is the saturation. In MOSFET that is called linear region, the current when it becomes constant saturated we say you are in saturation. That is the name changed from there.

So now, if you declare this that pinch occur here, I further increase V DS what will happen? Current is increasing. So, this point may actually shift from the drain into this, because now V GS minus V y itself may be small enough to pinch that channel that point. Which what does that mean you may have this pinch of point shifting from drain towards source as I increase V DS beyond this value, is that correct?

Now, the question in physics was; that if you have a channel, which is pinched here this is my source this is my drain. And I am applying a V DS, which is greater than V GS minus V T, electrons were moving in the resistor. But what is here? The depletion layer. There is no free carriers there. So, why carriers should go? There is no current. Current should have gone down 0 immediately is still didn't go. This is essentially saying, this is the depletion layer something like this, it is a large depletion there. There is in this depletion there you have a large electric field; the direction is positive to negative.

This large electric field whichever carriers are coming from here are sucked by this electric field, and brought down to the drain side. This is essentially how bipolar transistor works. As the carriers these base collector junction, the electric field there is so high, it collects, same procedure. Is that clear? Otherwise the current should have gone to 0, suddenly it did not, it actually sucked out.

So, larger the field here because what, but how much is the current whatever this resistor can give you only that much carriers can be picked up. That is decided by your V GS V DS values you already decide. But once it reaches there, at that point whatever carriers are available to me, I just be pull it up, is that point clear? This is the reverse bias pn junction theory, whatever is available will fall down. How much I am not sure. Whatever you say I will because that is slope. So, high electric field is high it will fall down. This is the theory behind the pinch of ahead.

If I do this and if I substitute those V GS minus V T, I call this value

Student: (Refer Time: 68:14).

Saturation, at which at a given V G value V GS minus V T reaches V DS. That value is called V D sat, it saturates. Now why currents become constant? They are still not answered bias. The current is becoming constant because, as you increase V DS the net this triangular part whatever it is the charge density is only governed by V GS. So, that is not changing, is that correct? So, the available carriers are not really changing for you. Because as I said gradual channel which essentially current cannot now change. Because whatever has happened has remained there. So, current becomes constant or saturated. So, it is essentially now trying to tell the following. It is telling me if I plot a I DS versus V GS character what is this curve called? I DS is the output current V GS is the input voltage.

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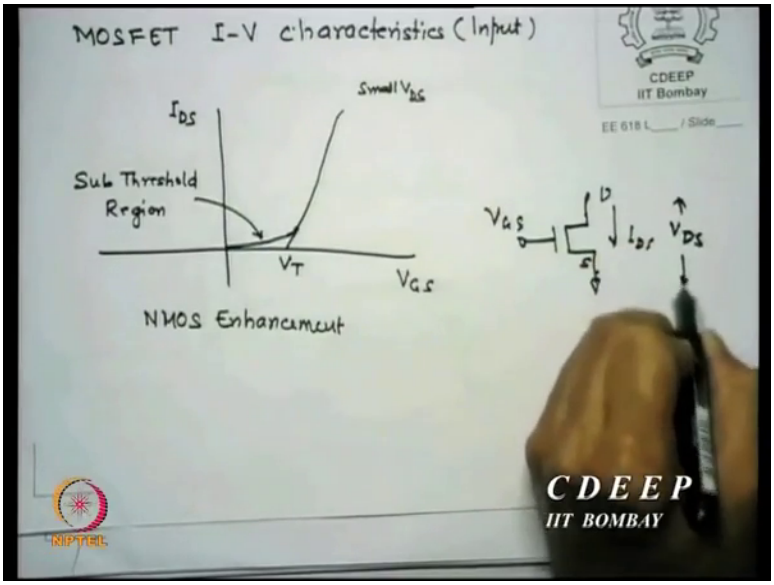

Student: Transfer (Refer Time: 69:31).

Transfer characteristics. This is drain, this is this, for n channel this will direction. So, input the output relationship is called transfer. So, I figure out as long as V GS is small less than V T. How much is the current? It is not 0 I said at V GS equal to 0 is 0 because there are there is nothing there. But as soon as you go beyond 0, then V T or what is the situation? We are still in inversion, but small inversion, is that correct? V T was defined as 2 phi F value because it started at phi F itself. This region is called sub threshold region. There is a current going on, there is a current going on and it is exponential we will see later.

But at V T which is what you say current, then start very heavily. And as it starts V GS start, increasing V GS minus V T takes over. In this case V DS is required y though V GS minus V T should be much larger than V DS, V DS is still require there are current cannot go. So, V DS is step kept in millivolts 10 sub millivolt to 100 sub millivolt. And V GS varies from 0 to V Dd. So, if you see the current starts shooting heavily prep V GS minus V T times.

Now, this is the call transfer characteristics. If I do the output characteristics. So, what do the output characteristics? Since it is called I DS against V DS, please take it sorry, I just draw I will show you the potential between this is V DS which is essentially for output in most cases.

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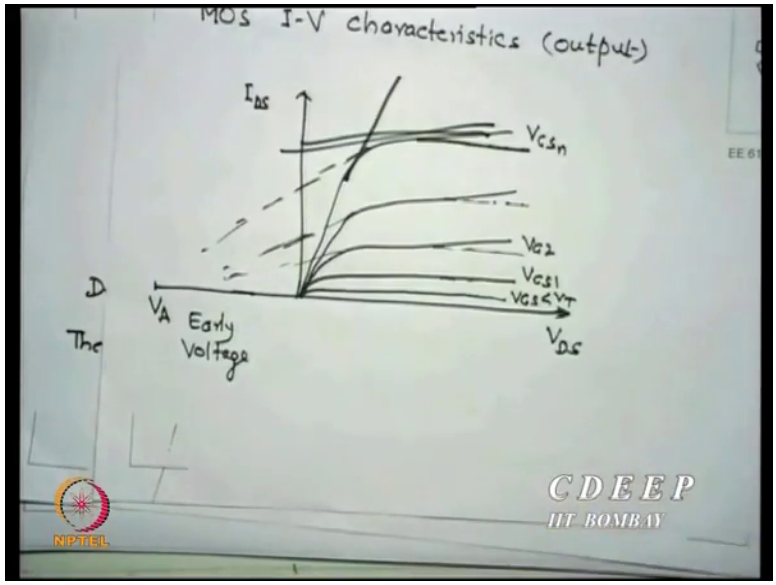


So, if I plot I DS versus V DS at different V GS values, I get for a smaller V GS which is less than V T a very little I DS which is this current essentially flowing. 2 currents it is flowing which are the 2 currents I have flowing here one is sub threshold, what is the other current in the transistor can flow?

Student: (Refer Time: 72:03).

Reverse saturation current of the 2 diodes, whichever is smaller one of them will flow, is that correct? That reverse saturation current plus sub threshold current is essentially small current, this small world is not really small, because in newer technologies that is

my issue. I said you in a one someday that 32 nanometer down, the off current maybe put in the on current. That is why I use mobile from constantly nah, so that power drain come how.

So, that is exactly the reason. So, off current shown here is very small. So, analog people are therefore, not very happy to go to 32 nanometers or some 0 nanometers kind. We are worried actually. Beyond this value initially current rises linearly, and for given V GS minus V T equal to V DS you know smaller V GS this point will be faster; V GS minus equal to V T V GS small. So, V GS minus V T small. So, V smaller V DS it becomes saturated. Larger the V GS saturation points goes above and above and different characteristics are seen.

The only problem which I see here is something worrisome, and that is may be interesting. As well I just now made a theory which is said current becomes constant, independent of V DS. That is what I say whatever available I push.

But in real life I monitor, I see on all such characteristic there is a slope, what does that mean? I DS is earlier I said in saturation it is independent of V DS, but it seems it is not independent of V DS. Marginally varying, but varying. And another feature which we will see later of course, not shown properly curves, if these slopes I actually extended in the minus V DS time, they all curves meet at one voltage. And that voltage we call is early voltage; which is taken from early effect in bjts. There is no early effect here, but the voltage is still given the name early voltage. There I C V c characteristics, a different iv if you extend down at one value of all of them meet which we call as where the base gates punched. So, we say that is early voltage.

Now, here also that effect is there. Now that early voltages are some interesting value, because then I can calculate my r 0 if I give I am given a early voltage. So that is the why I said early voltage. Now I want to know

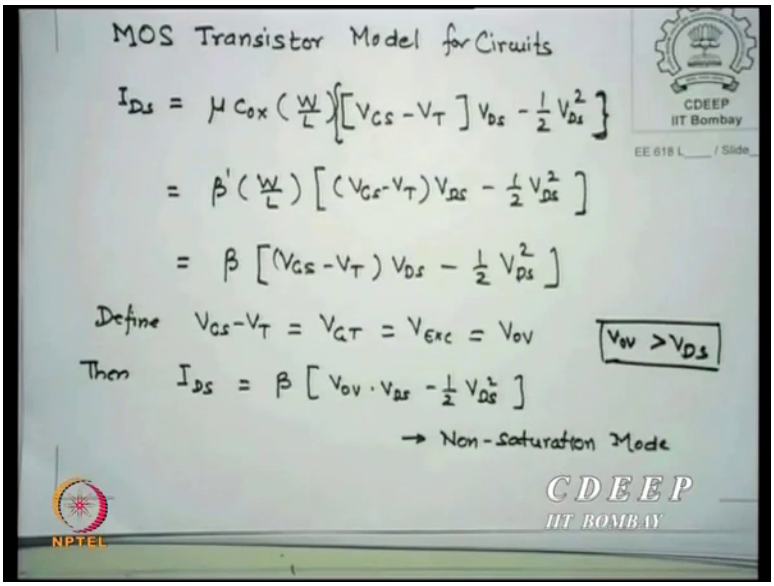
Student: (Refer Time: 74:47).

If I have to represent this few minutes, these characteristics as an expression first and then once I know expression I can calculate from expression what, if I know I DS function of V GS and V DS, I can in differentiate with respect to V GS. So, I get gm I

differentiate with V DS. So, I get my r 0. So, I must get a relationship first between I DS and which I first derived. But now let us see what can happen.

Student: (Refer Time: 75:18).

(Refer Slide Time: 75:25)



If V GS minus V T which I defined as please take it V GS minus V T I defined as some books defined as V Gt, some books like boyers and lakers book g laker boyers and least book define access. And I define over voltage, my definition. Why? So many years I am talking. So, I do. Why I said over over and above weekly, how much (Refer Time: 75:49) which makes transistor though of course, this is something taken from one of my old colleague from Stanford. So, I just use his this view.

So, in a book if you are having a different look, same names will be I am using V ov they may use vx or they may use V Gt whichever name they are giving, please remember they are saying what is it V GS minus V T. Is that correct? Now we say if V ov is larger than condition is V DS, that is V DS is small; that means, channel exists throughout, devices in non-saturation, it is not saturated. Is that correct? Device is a non-saturation the current can be given as beta which is mu cox w by L. V ov times V DS minus half V DS square. Is that correct? V GS minus V T is replaced by V ov. This is what more, when the channel exists throughout, and that condition can only occur when V GS minus V T is larger than V DS. Once V GS minus V T reaches V DS we know it enters saturation. So, prior to this; that means, channel exists throughout is that okay?

So, in a non-saturated mode the current is; and why I say it was linear because if V DS is smaller I DS shows linear relationship with. So, for a smaller V DS you are more linear. As you reach towards saturation V DS is not very small. So, you see curve slope changing. You can see from here as you reach here, the slope changes. And that is the reason it changes.

So, what is the model I am really doing? It is called 2 region model. One I will say like this, the other is sorry, like this. Whenever there is an issue 2 models at that point must have same values. Because that is the fixed value. So, at the new point both model should give me same values. This is the new value. I will say if that I get it, I say fine 2 regions it fits now that word is fit it fits, and then I use 2 expressions independently as if they I do not know what the other as doing. That is all modeling people do. Device people do not do it they do not like that.

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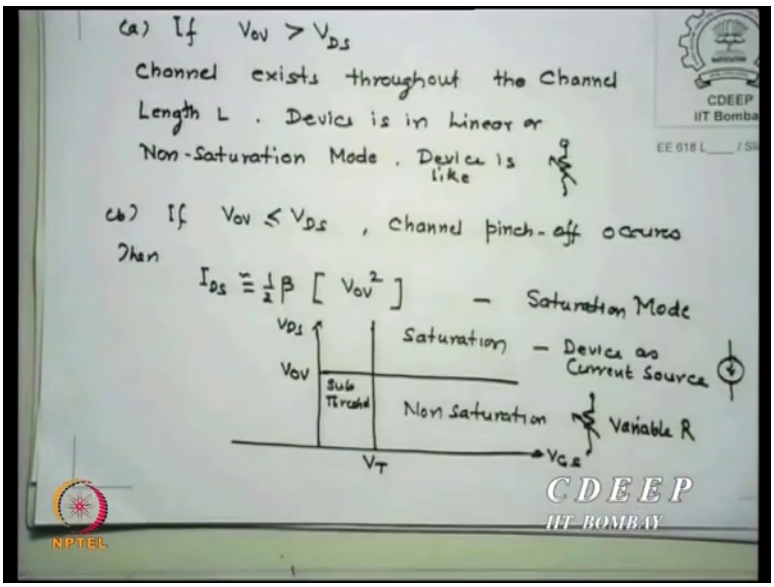

If now you say V ov is larger than V DS and I DS is proportional to V DS, what is it looks like? You can see from this curve again.

Student: (Refer Time: 78:46).

On this region, you know slopes are different, is that clear? A different V GS slopes are different.

Student: (Refer Time: 78:52).

That means, it is equivalently saying it is a variable resistor. As long as you are non-saturated at any V GS, you have a different resistors, is that correct? Linear is with a different art. So, device acts like a variable resistors in non-saturation, as straight as that.

However, if I now increase V DS further, I say pinch off may occur at V ov equal to V DS, or V ov is become smaller it may further get saturated heavily, then one can see from here that expression, which I will just show you. Now I will just repeat again.

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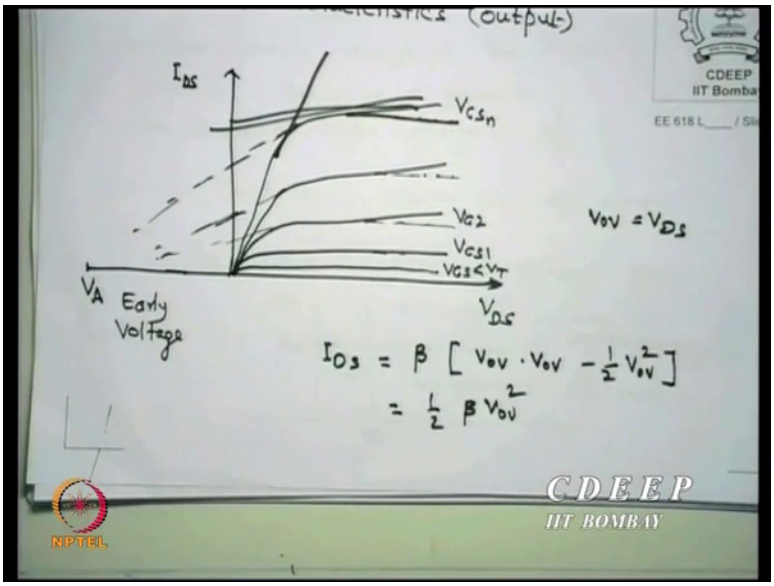

If V ov is equal to V DS, my expression rights I DS is equal to beta V ov into V ov minus half V ov square.

Student: (Refer Time: 80:01).

At this point, this is the expression. Which is half beta V ov square, is that correct? Half beta V ov square. So, what does this? Does it have any relationship with V DS? No as of now it increase that. So, what is it acting like? I DS is independent of V G V DS, what is it looks like?

Student: (Refer Time: 80:29).

Output current source. So, a transistor in saturation acts like a

Student: (Refer Time: 80:35).

Which current source?

Student: (Refer Time: 80:38).

Voltage control current source V ccs it acts like a V ccs.

So, the graphical graph, V DS versus V GS I am shown here. If V GS is less than V T, and it is V ov you are less than V DS is less than V ov this region is sub threshold. Anything below V ov V GS minus V T is greater than V DS V DS is smaller than V GS minus V T, you are in non-saturation, which means you have a variable resistor. And V ov is smaller than V DS, and V GS is whatever it is for this value you are in saturation. Which acts like a current source, is that clear to you? This is what equivalent of mos (Refer Time: 81:36)

So now I know, if I see a mos transistor, depending on the voltages I am using, in my circuit I can replace the device by equivalent current source or equivalent resistor depending on the way I am working at. If I force the device to always remain in saturation, then what will happen? The mos transistor will always behave like a current source. That is exactly analog region. When the device vo vi characteristics shows slopes, both devices of p channel n channel are in saturation. Therefore, we said mos transistor analog is always like a current source, but the at the edges it does not. So, signal if goes beyond so-called nonlinearities may settle.

Finally, last expression for the day and we will stop here. In saturation in real life I say there are slopes I DS beyond saturation point also keep increasing very literally. I mean the slope is very low there.

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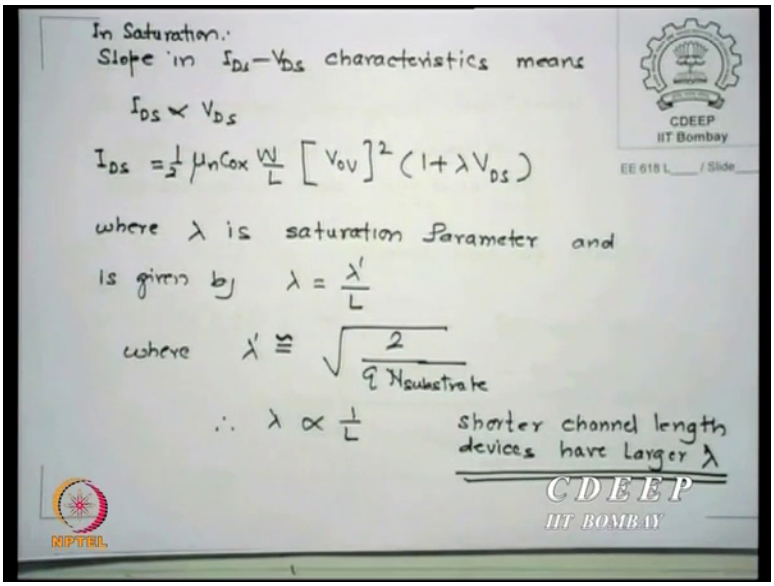

Now, if I see it is a very slow low, I can fit in this. I fit the curve and I figured out this is my normal saturation current, I multiplied by lambda V DS, 1 plus lambda V DS where lambda is called saturation parameter, which we can derive of course, is equal to what we call lambda dash by L; where lambda dash is equal to 2 upon Q substrate under root we can derive all the theory of that.

When the device is having a flats this from this characteristic can you say if it is very flat, what does that mean? Lambda is 0, 0 flat as lambda increases 1 plus lambda V DS factor will start increasing, the slope will start building, is that clear to you?

So, in a technology is small you can see it is substrate dependent. It also is depending inversely proportional to length. So, if I wants smaller lambda, what should I do? You can see I want smaller lambda. So, I should have larger substrate concentration, but what does it will do increase V T. So, if I increase V T what will happen? My net currents will go down. And I is I let us say 2 gm will go down; however, the other possibilities are use longer length devices. So, is that now clear? That in normal good device I want saturation to be very good. So, what should I use device lengths?

Student: (Refer Time: 84:28).

Larger than normal technology node. For example, you are working on 90 nanometers. You should not use channel length everywhere 90 nanometers. Use it one 80 270

something 2 times 3 times. So, the analog functions will be better because of lambda will become smaller, is that clear to you? This is the crux of all analog design. How much channel length you should use. Longer channel devices therefore, will give you better analog performance any day is that clear to you? That is why 0.25, 0.35-micron technologies will give you better analog performance. And 65 nanometer 45 nanometer then it start killing you. How do I get rid of both? That is the design part.