CMOS Analog VLSI Design
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Lecture – 03
MOS Fundamentals

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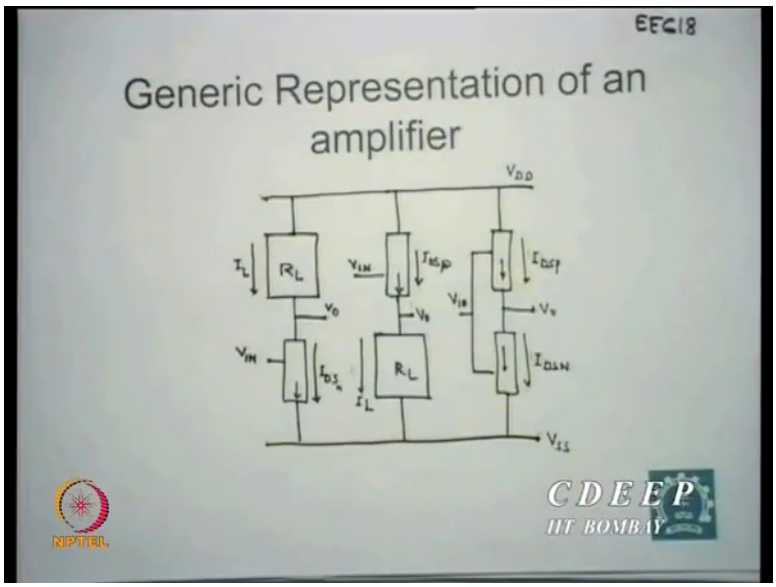

As I said you one of the major criteria of any design in analog is to get the circuit working which has gain that is our most important thing amplification that is what we do in analog circuit. So, we want to amplify an input signal which may be very very small in many cases like in mobile and there is the antenna gives a very very small signals and we want to amplify that. So, our major activity in any analog design is amplifications. So, all our effort initially will be how to do a good amplifier now what is this word good, good means what good.

So, we will like to see how do you design desired amplifier characteristics instead of saying good, there are yes.

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I agree with you filters for example. But if you see a active filters there will be some unity gain amplifiers, gain does not mean essentially even the attenuators as a minus db gains. So, in some sense amplification is the conversion of some input to the output in

some you have a right valid issue. However, here the circuits which I am showing probably have gains there are three kinds of amplifiers shown into shown by me one is the standard amplifier which all of us know. So, these are three amplifiers shown here the first one which you are seeing here is essentially an amplifier in which there is a some kind of an active device in general it may be n channel device for a MOSFET which has an input and it allows you know some kind of trans conductance through this at the output.

So, it converts this voltage into some current and through this load current flows in this please remember in a circuit in arm only one current can flow. So, if this is my output arm only one current can flow. So, whatever is current coming from power supply must go through the driver either. So, this two currents must be balancing every now and then, the driver current must be equal to the load current because there cannot be two currents in the same army.

So, this device which is shown here shows that I L is equal to I DS n and whatever I am showing here the lower part of this device in case of n channel it is source is grounded to V SS. Now, this word V SS will qualify little later we do not say its ground always what I mean why we says because we may not say it is ground always, but in right now let us say its ground and the load is connected to V DD. So obviously, this is the standard amplifier this device can could be bipolar transistor it could be a MOS transistor and in any case ir drop here will actually provide you the output voltage, very simple amplifier.

The other version could be you may have a p channel device or PNP transistor and since you want to keep that power supply same positive V DD. So, this is than become source than becomes drain for p channel device and the load is downwards and same method one can say the output is now. The reason is that I am always saying current can always flow from power supply to the ground irrespective of carriers is that clear whether it is the electrons are holes though they do move opposite they do move opposite, but then net current electrical current external to that is always in unidirectional from positive potential to ground or negative potential that cannot be change this is Kirchhoff's law and nothing much can be done on it still stands perfect.

So, this is a p channel device, same technique. So, one can have an n channel device or can have a p channel device both for amplifiers and if we make a combination of the two

which is the p channel device and n channel device connected to the gates we call it complementary MOS or CMOS amplifier. So, this is essentially to some extent we are now saying that each transistor behaves as load for some time is that correct initially may be this is driver this may be acting like a load after some time this may act like a driver and this may or you may say superposition, you have n channel amplifier superposed on p channel amplifier each acting load for the other one is that clear.

So, this is a possibility which we can use and the advantage we shall see soon why CMOS because you already seen CMOS is one technology which digital has adopted till as I said technology node right now is 16 nanometers. So, since every circuit is digital which is marketed in heavily at least there is a 20 percent is analog; that means, 80 percent is digital so; obviously, we someone who has majority or power will govern. So, digital people govern and because of that CMOS is the standard technology do what we. We may change materials for some reasons for some device or some circuit requirements that may be are silicon carbide, silicon germanium, silicon germanium carbide, gallium, arsenide, indium arsenide, indium arsenide, gallium arsenide, mixtures many things can be done. But CMOS may still may and as I said many years for last so many years 2030 CMOS is going to stick.

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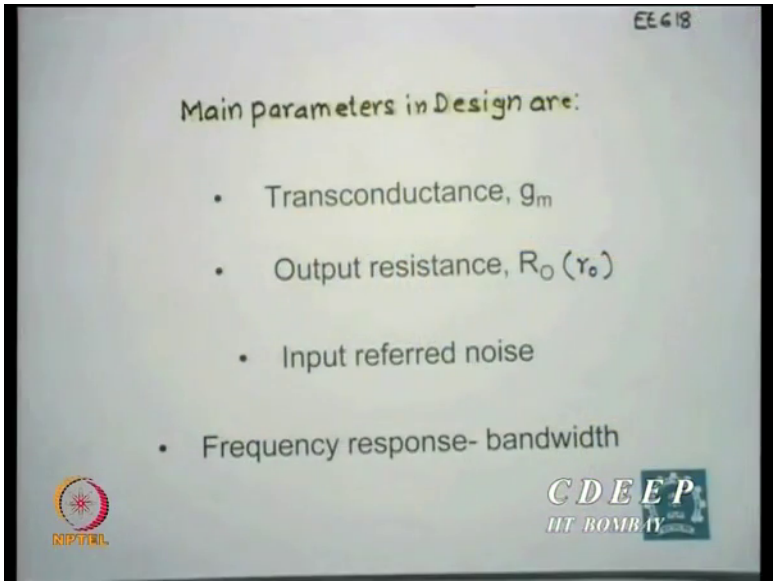

In any analog design we find there are few parameters of relevance, three of course are most common some others will add later. The first of course, is transconductance what

does; that means, from the input voltage how much is the output current gets modified by the input signal essentially called trans conduction, from voltage to current converters are essentially trans conducting. So, the first and most important parameter for an amplifier is the g m transconductanc. We will see what values we get in real life.

Then the next very very important characteristics of a amplifier is the output resistance. In the case of normal amplifiers which we are seen just now for example, this you know this load of this, this may be a resistor, but in n CMOS there is no real register there. However, you can connect a load afterwards. So, you can have something like this as external load, but the way circuit operates generally in integrated circuit there is no real resistance put anytime whatever is the output resistance of this is useful for the next stage connections. So, what the next stage input resistance is the output resistance of the last stage and that we call as R 0.

So, in an integrated circuit not that R L will never be used, but in general connections are not through load actually load is output resistance itself is acting like a load. So, having said so, the second parameter of interest for me is the output resistance for the transistor or the amplifier which is R 0. And the third and the most important for analog is the noise this and the word I am keep using this were very important when we come to noise we shall talk about is input referred noise. The noise can be at the any node, but we call it input referred noise and that is very major criteria of design how much is the tolerable input referred noise, how many DBMS or DBS corresponding given signal, how much essentially it converts into what value we are more popularly known signal to noise ratio, how much is this noise at input to noise that output ratio we can get is very crucial for any amplifier.

So, this input refer noise is essentially is a basic noise available without external anything and say if that is what is going to change or increase and your purpose of amplification may not be as good. And the most important other than the gain factor which is the first three essentially a first two essentially gives the gain, second one is the noise were worrisome and the third which is the most equivalently most important from digital there is a speed how fast the circuit is working 6 gigahertz, 4 gigahertz, 5 gigahertz here is what we say equivalently bandwidths; how much is the bandwidth, that means, up to which frequency gain is constant or reasonably if we say its bandwidth.

So, for an amplifier we are always designing for a gain, noise and bandwidth is that a three parameters which we wish to control. If we are able to control these three parameters strictly then I have designed done for my requirement is that if I cannot control all its so happens trying to control one, I lose something else then I save ever that is with this technology with this, this is possible no more that is we say figure of merit end of it.

Before that how much play we can have as in the case of digital I think you are already learning and you know much about this we can trade off power and speed increase power; that means, increase currents the capacitor charges faster or discharges faster so speed is higher. You reduce the power reduce the currents slows down; however, we can meet both slightly by adjusting area this is the game which will play in digital. Here we have to play game for gain and frequency. And third which is not visible immediately is the noise which may actually control both. And therefore, these three are very crucial parameters in our analog designs.

Here is another slide we are still generic will come to it today MOS transistor little bit so that you know what exactly I am talking about.

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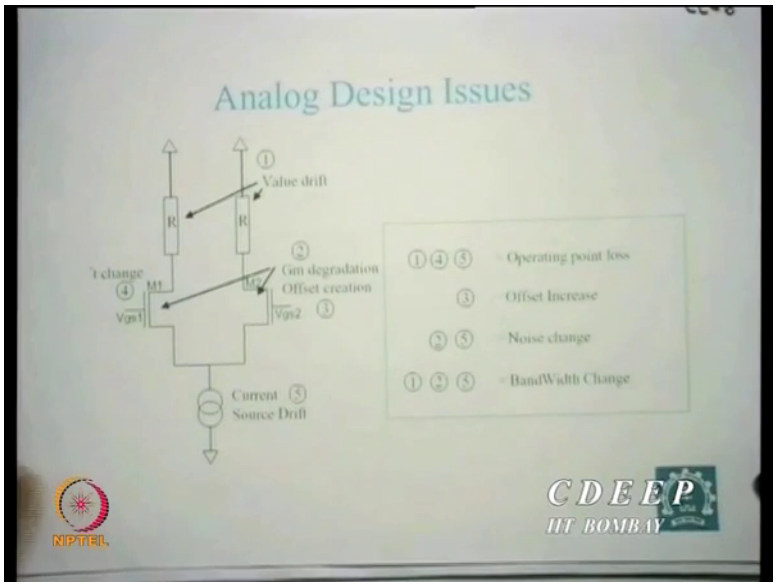

Here is the differential amplifier shown to you wills you actually design and defend this semester. There are two n channel devices with two loads and this is the biasing current which is called current source and I we are just name them 1 2 3 4 areas. So, for

example, there is R when we said constant there is nothing called constant in circuits are devices or in integrate circuits R me drift change. So, one possibility is there is a variation in R.

We also said the transistors are identical for define this is only statement will be in reality M 1 M 2 may not be identical in many ways. Its threshold may not be same its size may not be same W bias may not be same and therefore, they are not identical. So, there is some kind of offset relationship, g m it will be related to them, so g ms may not be same for either M 1 and M 2. So, that is another issue which may have to create. And of course, this so called constant current source may not be constant and if that change is the bias point is changing. So, if the g m and everything else we change.

So, if you look at these variations 1 4 and 5 that is V t change drift in this and R values it may change the operating position of the amplifier. If you look at the 3 that is essentially the offset because of the non W by l equivalence then it may increase this change may increase actually two devices may be offset by some value. We believe that they are same, but we are not actually.

However do not worry in real life offset can be canceled some way or the other. It is not that there is no way we cannot get rid of offsets. What is the price will pay? As I increase any high, as I improve anything I will have to pay for it and that payment may be in the external extra hardware which I may have to put or extra power I may have to pump to get rid of some of these, but that is not that we cannot do that and will see some of the offset techniques will use that. 2 and 5 which is essentially again threshold variation as well as offsets in g m particularly in g m variation causing because in M 1 M 2 same way the change in current in the biasing currents may actually lead to change in noise and noise is a very crucial factor as I said to you.

If you look at the last this one, we say one change in R 2 changing g ms and 5 changing current biasing current all of them can change the bandwidths. So, the is that point clear why design is an issue because in design I will be given a specification, but please take from me if anyone gives you say that I want a gain of 100 you say I cannot design for you, you say what is the maximum minimum in between the gain you can expect. You say in a range of 80 to 100 I am fine with it, so I can design a circuit which may gay give a gain 80 to 100, but it may not be always 100 or always 80.

So, anytime aspects is given to you give designed this it is not doable. So, one respect must come from your customer which is doable and that is once a range must be specified. So, I will say the minimum gain I expect is 100, so if a 120 I do not mind, but 100 is minimum bandwidth I wanted so many mega Hertz yeah that is the minimum I expect, but you do not say no it is 2.73 mega Hertz or 2.73 I cannot do this any design there is no way I can control specific values. If I try one and then I other I may not be able to control. So, I always will say you give me some margins in designs. So, this is the major difference in analysis which we do and the design we do.

But to do a design we must know analysis other how will a design, but the focus should be this that we have to attain specs within a given range that is the trick of the design issue. If you look at the other part which I said gain and bandwidth I just said it, but they will come back later also.

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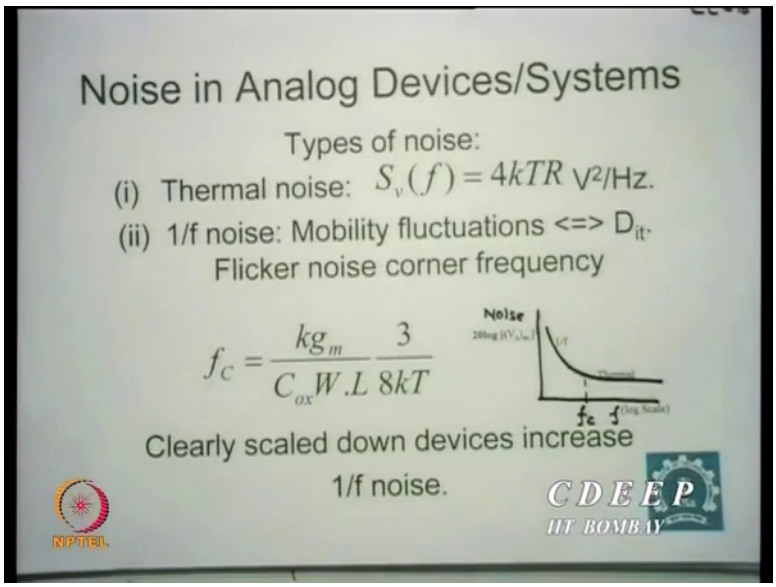

I will not going to very strong detail just I will show you there are two kinds of noise. In fact, three kinds of noise, but at least shown here one is called thermal noise which is always present because of the incessant motion of carriers which is called the thermal noise and there are other names also in thermal noise related names short noise and other (Refer Time: 16:05), but I take it thermal as a common name. And the way we will define when I talk about thermal noise it can be given by as we called 4 kTR whole square by Hertz and this is the function S V f is a noise function will define it little later.

The other noise which is very dominant at low frequencies it is called flicker noise or one upon f noise. The word one upon f came because the noise essentially decreases with frequency linear. There are noises now available which decreases by 1 upon f square first of is noise as they called will see that and the tongue comes, but see simple first models are there frequent as the frequency increases the noise linearly falls this noise area or this noise is called flicker noise.

There is a point at which this flicker noise is exactly equal to the thermal noise and that is called corner frequency, we can define this latter you can see the figure has been shown here this is the noise versus frequency initially there is a one upon f noise at low frequencies and somewhere beyond fc thermal noise takes over because this term here volt square per Hertz will actually start dominating over because 1 upon f may go down further and the thermal noise will take over.

So, we say at the point where thermal noise takes over from 1 upon f we say corner frequency for noise and that is given by some kind of this function and will see to it how do you control these values. Noise is some way connected to g m you can see clearly it has a term oxide capacitance per unit area the width and the length of the transistor and of course, the temperature at which you are working of course, all noises are generally temperature dependent. So, if you are working on a circuit which is at higher temperature 55 degree centigrade or 80 degree centigrade which is a military standard requirement may be 125 degree centigrade and that case your noise will be higher definitely higher nothing much can be done because kT dependent.

So, noise is their temperature dependent and therefore, in normal circuit what will you do to reduce noise, cool it if possible as much as possible or remove the heat from the circuit as fast as possible. If you can do this keep sinking then you can operate the device at relatively lower than. So, where it will be the lowest in their life, if I put a liquid helium jacket everywhere 4 degree Kelvin then yeah my all noise, but then suddenly you figure out g m once will not be there. So, then the amplifier may not be available, but as such noise can be minimized by reducing the temperature or what we call ambient temperature. Do not look at too much into expression which will anyway derive later.

Here is a small amplifier shown here the idea why I wrote those expression is to explain this figure.

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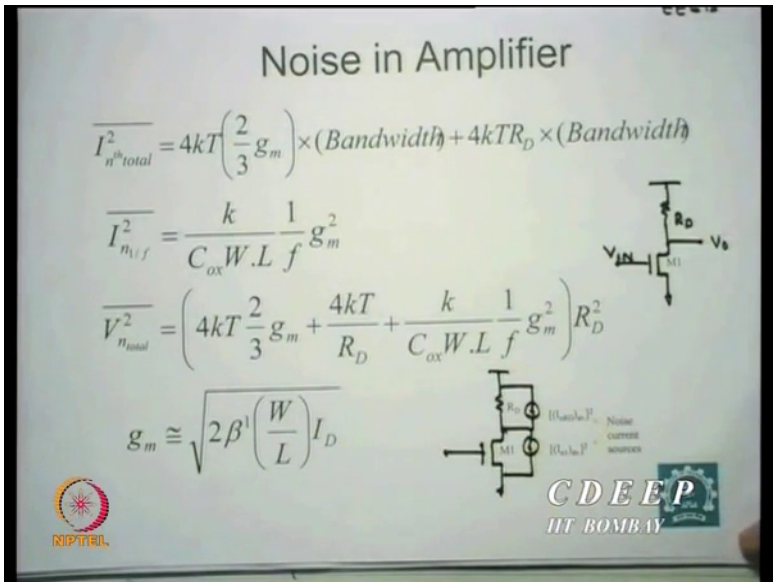

What we say that each resistor or a device which also in a way is resistor contributes to the noise and it gives equivalent current sources across each of them. So, you R D there will be a ion R D average square current shown here and this is ion device every square each two currents sources are available with each device and the resistant. So, as many devices or resistors you have that many current sources noise current sources are available and noise currents, currents multiplied by registers variable will give you noise outputs.

So, larger the iron squares are equivalently V ns then you will have larger noise outputs is that clear. And when can see somewhere they are strongly related to g m is that correct and therefore, as you look for the gains as you look for the bandwidths keep mind that your noise is also getting affected simultaneously. Then many designs this criteria of noise little higher and therefore, we do not pay so much attention as normal case, but in real IC designs now probably you may have to actually start looking first noise and then see now what can I do. So, these issues are very relevant and therefore, should be appreciated this beta of course, except means W by related will see that the device parameters essentially decides the noise factors. We will come to noise again because that is a very relevant area of analog designs little more in detail.

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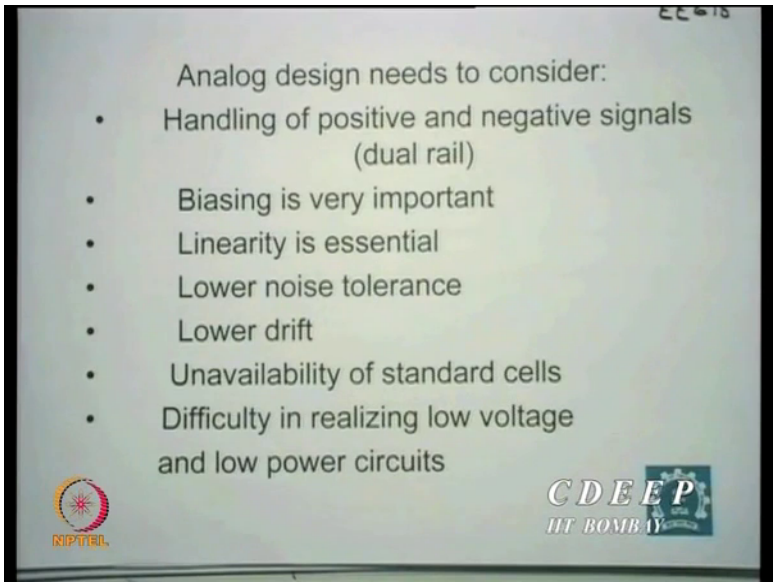

So, if you are a analog designer what are you looking at how much things he should consider say few things not necessarily it is all of it, but most of it I have written.

Most analog circuit if you see they have signals alternating AC signal signals are not necessarily you need you need direct DC they may be waving, but not DC they are not only plus, but they are also minus like an ac signal running on 0 voltage. That means, signals can be positive or negative. So, is power supply can be positive or negative in our designs, V DD and that V SS word can be done minus V DD also or my we call it minus value of power supply or any other value need not be same I this is called dual rail, 1 rail plus 1 rail minus. Compared to digital design all analog circuits always have dual rail designs because many a time minus V SS or minus value at the lower end may help.

In the case of analog I already shown you I V characteristics earlier, but maybe will show you again. The biasing point where you buyers decide the d V 0 by d V that is the gain, where do you bias is very crucial because that will decide the g n that will decide R 0 that will decide everything for you. So, bias point control is very very crucial and analog times. So, as I say if that drifts everything drifts. So, one is to worry about bias points operating. In our second year course we always thought [FL] fixed bias [FL]. So, you have to do some tricks to keep that constant.

Also for normal amplifiers we do not want gain to very because otherwise you know for some signals it is something some you want gain to be constant or to say V o being

characteristics in the region of interest should be linear d V 0 by d vn should be constant linear. So, that is one important thing and therefore, these circuits are many times called linear circuits because there we assume gains are constant d V 0 by deviant relationship is linear and therefore, the circuit themselves are called linear circuits. It does not mean that in real life there will be everything linear in fact, the whole life of every one of us or every fee creature of this world is extremely non-linear. How much non-linearity you can control or how much idiosyncrasies you control that is what your outputs are nature would be every one of us have different idiosyncrasies you have very non-linear in nature same inputs does not evoke same response.

Some may be right now feeling why is teaching, but still sitting here, some may has each giving to trivials everyone has that same thing I am saying, but you may have different perspectives that is what I say non-linear issues. So, reality is non-linear, how do we control non-linear systems. It is for that I said already you said all analog circuit are extremely noisy. So, they should be somehow may noise tolerant, but they are very low noise tolerant small change will immediately shown at the output do not do anything it will come out. So, that is the one worrier for a designer. We must see to it that the drifts are smaller I just shown you earlier figures the drifts can cause what everything can be changed. So, drift have to be minimize is one consideration in every design.

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Anything which changes is the drift; this value drift it can be plus or minus drift can be either. Standard cells are essentially block design a priori design fab tested and then their square block is shown to you AND gate. So, inputs one output this currents the speed and internally what is not to do this is a standard cell from. There is no real problem with digital circuit even if I reduce the power supply we are going to 0.6 as I say maybe 0.4 someday because we are we are happy that 1 0 still can be reachable.

So, in analog if you reduce the voltage the current reduces and g m is nowhere then g m is the essentially proportional twice what formula it will root or a square or half whatever you see later, but it is function of ideas. Now, if you change this the current goes your gain goes bandwidth goes, everything goes and then now as I say in the new technologies when you are asking us to work on a very low biased circuits we insist that

at least do not tell us that you will work on 0.44 we will have our own power supply and we will work on our own circuit part.

So, there is a power management unit on every mixed signal because analog cannot function at point 4 it say it say no, you are closer so much to the noise that I will only c noise. So, I will not like to work at very low by says though it is fantastic because it will give low powers. So, designing a low power analog is itself a big challenge. So, that is the game one has to play because overall chip cannot be you know one part is heated for so much and the other is not so much then there is another issue will come in this temperature gradient it will set and it will start wearing that digital far faster. So, there are issues in placement of analog blocks also where do you keep them.

So, there are many issues when you put analog with digital because as I say low power is the game everyone wants low power which is true means low power is the game this days, rather I always like to call that low energy systems. We are not very keen about voltages is a powers we should be worried about energy. Essentially I am saying you can have large currants with lower voltage or lower larger voltage lower currents still energy and for a shorter time. So, as long as you manage that you are still in a low energy systems and that is more important.

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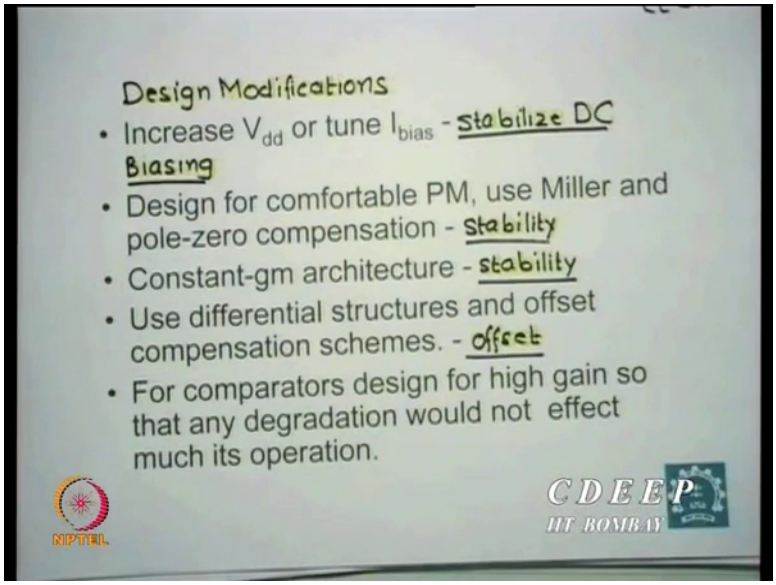

So, to summarize what I said in key to stabilize the DC biasing you may have to either increase the power supply or tune the bias currents variate some way you will see current

meters do that. The word pm is very important you will see come to it later phase margin one of the major worry in analog circuit is phase can relationship between outputs and inputs. If you are seeing a transfer function in a control theory we keep talking of margins sometimes in time scale we say jitters, all of us are jittery when something does not go well that we want in circuits when the jitter it gives noise mob; phase noise. So, what we do is that may change the stability of the system. So, you may have to do some kind of pole compensation pole 0 compensations or some way you must split the poles or whatever technique feedback systems are therefore, necessary and you must get the stable circuit.

We must work on architectures which are constant m because if g m changes as I say everything changes. So, any design you do see to it your block has constant here that should not be I may change the value of a g m at my will, but once fixed it should not change that is what design is all about constant g m which also is required for good stability. Now, we know this offset part which I said if the two arm of the circuit has equal upset or equal change in a differential mode something which is common may get cancelled and that is what the different theories are about and therefore, offset can be minimized if not making 0 at least by using difference and will see that is why all differential amplifiers are so common in analog designs.

For comparator designs you need very high gains so that any degradation would not affect much its operation because comparator shifts a to d converts. So, the gain of any comparator should be very high so that any marginal change should not reflect 1 0 it should give immediately and such degradation effect should be minimized. So, when I say gain I am certainly looking at g m and when I say look g m I go upward and see everyone is hurted by heard by change in g m. So, the issues are essentially device related and circuit related in their interactions.

So, when I design you must remember that design is not just analysis is right I think I made other day.

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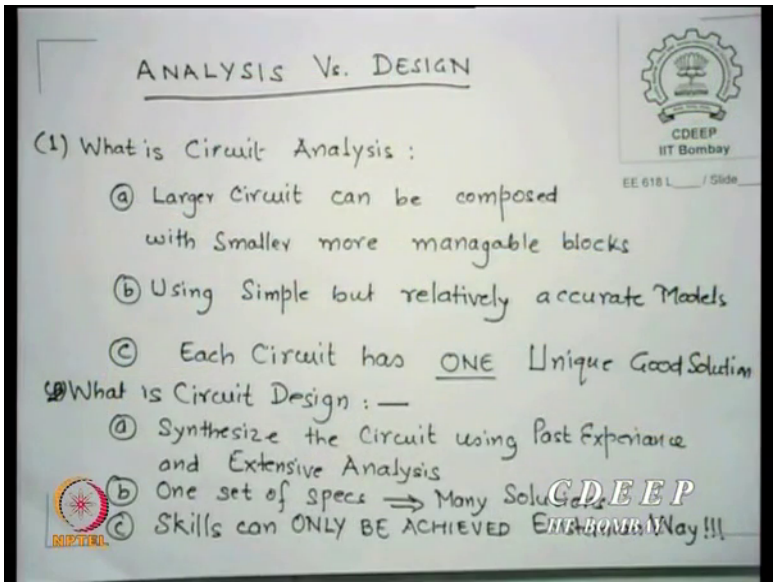

What a circuit analysis in my opinion someone asked me well, we can have a larger circuit which can be decomposed as reduced into smaller blocks and each block is manageable in designs that is analysis how we do it we do not solve simultaneously huge network you can solve on a spice or a simulator, but normally when I analyze I do not have such large papers to write so big expressions.

So, what I keep doing is use blocks see to it that it is input output always matches that is the trick we use and always reduce into blocks and design it and these blocks should be designed with very simple models for transistors or any other device we use. If they are too complicated you cannot do a circuit analysis easily. So, you need to have very simple models, but relatively accurate because otherwise why I calculate gain 100 and it founds to be 10,000 then I am nowhere. So, it has to be delightedly accurate, but much simpler to handle.

So, why do you really need then the in so called simple models yeah they do give some values which can then act as a first assumption values for large signal or large value analysis, where to start that is the issue. Each circuit has one unique solution this design this analysis if you show me this is input this is output this is alternates unique solutions. Now, if I do a design how it differs. In most cases you synthesize the design by your past experience that is why to protect this, this word IP has appeared if I design its mine and you cannot take (Refer Time: 32:31) and take it.

So, this is from the past experience and since if than does not know exact solution you do a lot of iterative solution. So, you actually have to do extensive analysis to really design a circuit when you say extensive which means by manually it is very difficult how many times I have do 100 times same thing just tweaking things. So, it will be very difficult. So, I need some support from other than me. So, I will see what it is. Given aspects there can be many solutions whereas, in the case of given a circuit solution aspects in this case there is a requirement and I may get through anyways and that is the designers issue.

Now, one interesting feature which I wish to tell you all as an engineer if you want to become good. All engineers require skills engineering is not only analysis engineering designers, engineers should be good designers and they require skill. Now, how they can be achieved the word I used is Einstein in bei. What is Einstein in bei? Einstein once asked that when he was doing problems in general relativity one of his person student in his class or rather his colleague that time, he asked him how do you really solve such a intricate complicated problems or how do you approach that.

He says just by doing it. So, to attempt anything just do it that is the only way you can do some things and long as you do not do it you do not know what to do it and therefore, you must do it that is the Einstein. So, please follow your failures are good enough they will teach you many more things and next time you will be more accurate or more correct.

So, this is my suggestion to all those who wish to remain in even in finance value this may be equally true. Some of the building blocks which I am going to design in this course I am a design current sources current mirrors, single stage amplifier, differential amplifiers, operational amplifiers, variety of operational amplifiers there may be a cost code amplify, Op amps, there may be what is OTA means.

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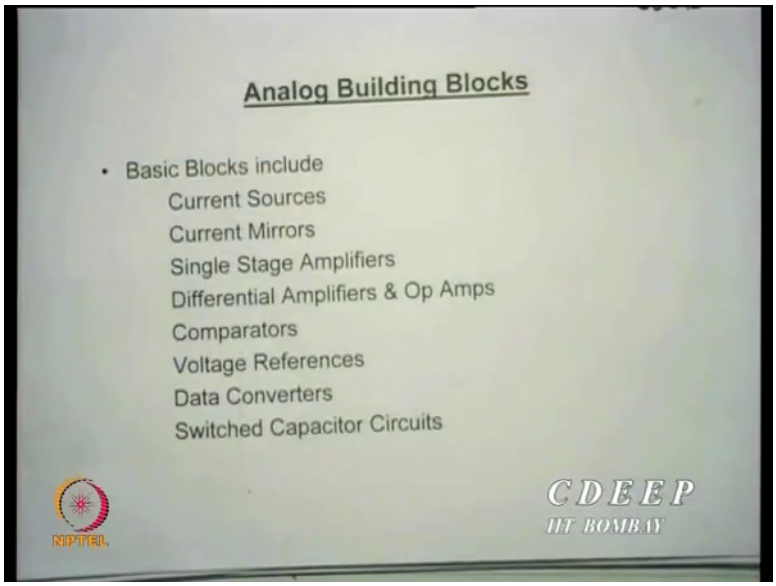

Operational Trans conductance Amplifier g m related, so OTAs then I may designed comparators voltage references. I did not specifically said the lower one my said unsure data converters this part though is required since there is a mixed signal course going on I will not talk about adc and dac in this course. I may instead talk about oscillators and frequency synthesizers, plls maybe I will talk more.

And then the switch capacitor circuit these are essentially also part of mix signal, but since they are filter realizations we will talk about some simple filters if not very complicated filters active filters as I say using switch capacitors which is what technology will appreciate. So, this is something blocks will this course will address to. Hopefully by the end of the course you learn enough that all of this you yourself can design to given spec.

So, please remember we start always with trivials and then build on this, this is how designers to do small [FL] another small [FL] keep doing till you reach your ultimate aims. Many of you have already done this and hopefully should have done in your second year course at least. So, this much so far is more generalities we say this is what analog design is all about and as I say our course name itself is CMOS; that means, there is a MOS transistor setting somewhere, though I know again radius to [FL] I have taught them devices. So, they cannot say MOS device was not taught other scan. So, [FL] others may be here I may start with a little bit of basics and MOS transistor because I keep

saying you analog design is more between interaction of device and a circuit. So, not knowing devices will not help you in a good analog design is that clear to you where are they in digital you do not need to know device technology or anything. In fact, nothing you should know you can still design; the best designers who do not know anything, so they design better.

The problem with the designers is essentially I said it is iterate you are to longer process to do please take from me in analog design what is the problem. There is a very famous story of a famous statements made in many books many journals many years ago that if you put n number of monkey say 100 and give them paint pencil paper and ask them to sketch anything what they do even then they cannot write it legible book irrespective they say they are our ancestors, but even then they can even with 100s of them. Same way if you ask a monkey who is relate why a monkey is used because they are next to us. So, if we can do probably they also can is the; if you ask a monkey and give him a spice tool and say designed base circuit you may keep putting hit at no time and optimal circuit (Refer Time: 38:24) output will come.

So, essentially in special that probably may happen in digital do you regards, but in analog you have to use your brain f in manual intervention is a part of analog design. So, intelligently only you can two things, if you want to leave this leave analog because that is the difference I want say I mean as I say I am just more reacting on that, but just to say a fun of part in that that analog designs requires knowledge of technology to great extend much more devices and of course, your circuit background has to be always good for any circuit course in electrical engineering.

So, we start with the basics of MOS transistor quickly today maybe will finish that. So, that next time we start with the real amplifiers.

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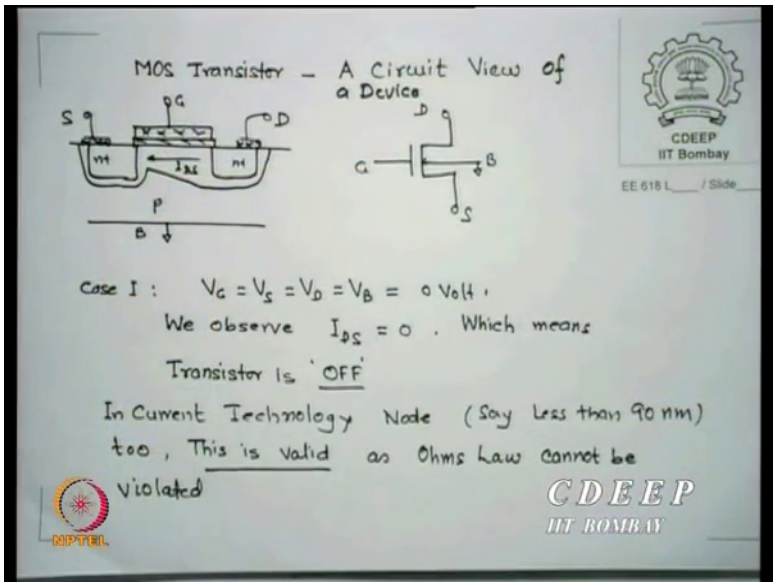

The MOS transistor as I say circuit view of a device is very relevant to us for a device first will talk and then will say how it circuit people realize it, but for them is the value here. I only a MOS transistor, so for me I say I have some sub substrate I created some regions, I have some gate some dreams on, which technology can give me. So, I have got MOS transistor, but how does it work and if it works how a circuit man knows how it has it work if that relationship what circuit wants from a device is what this few sometime this slide will show you how does specs of a circuit is controlled from the device parameters. Will not go further down how technology manages that maybe that is also relevant someday if now it leads today, but it is ok.

So, here is a typical MOS transistor shown to you this is my substrate which is p type. So, it is an n channel device shown to you. Two regions diffusion that or implanted in that is source entering n plus this is a two dimensional picture, but as I said you earlier also many times MOS transistor is a three dimensional device. I do not know I do not have anything maybe this please it has third dimension. So, if this is my source, this is my drain this width is the third dimension. So, what you are seeing is only this cross section, but there is a width part in this. So, that is called W this is the length this is w.

So, MOS transistor is not a two dimensional device as in most cases bipolars are of course, the current bipolars are also not true dimensions, but earlier what we used to do pn pn pns they were only two dimensional. Now MOS transistors are three dimensional;

however, they are 4 terminal devices not just three as one thinks that is the difference we should understand.

So, the first terminal is source the other terminal which is output as we call drain on this n regions there is a thin insulator layer put here in 90 percent cases are 95 percent case is a silicon dioxide of last 15 years silicon dioxide has been replaced by hafnium or hafnium nitride oxides or zirconium we are trying many high k dielectrics when the channel length goes down. But assume it is a good dielectric and for most purposes we say it is still silicon dioxide unless said otherwise.

Now, this is SIO 2 or whatever insulator you put. What is the advantage of insulator? Insulator does not pass any DC current. So, it is a good insulator. Typical insulation strength of a dielectric like SIO 2 it has a 10 to power 7 volt per centimeter as their dielectric field at which it will break down here break down to 30 volt per centimeter. So, you can imagine what I am talking about. So, this is my gate and there is a substrate contact which I call bulk B sometime I calls S once a while, but since source is there as S, so let us call it bulk. So, there are 4 terminals in a MOS transistor. If you show a equivalent circuit for that this is drain, this is source, gate is separated from this because of insulator and this is my bulk contact.

The symbols are known if the arrow is in it is n channel arrow out it is p channel. If it is a p channel device this will be n substrate and p plus p plus substrains. The only thing you will happen is whatever voltage be applying n channels the opposite polarity should go for p channel for the similar performance. So, the case 1, V S, V G, V D, V S, V B all are 0s. If everything is 0 there is no current between drain and, irrespective no current means no current because Kirchhoff's law says if there is no source there is no output. Unless of course, you can say noise, but that is source otherwise there is absolutely if everything is grounded no outputs everything is 0. Also we said transistor is off nothing is coming out.

In current technology nodes say less than 90 nanometer to unless even for that this is valid because Kirchhoff law cannot be faulted, at no supply no currents irrespective. There are cases maybe smaller current because something else, but otherwise if voltages are grounded no currents this is the trivial case, but very relevant case to say in real life therefore, device can never be switched off is that point clear because these conditions

can never met is that clear. Why I showed you this slide, just to show you in reality this case cannot be achieved.

Though I mean it is possible you can always take a transistor and ground and check, but in circuits this will not be relevant case it is called treviance, will not go for treviance.

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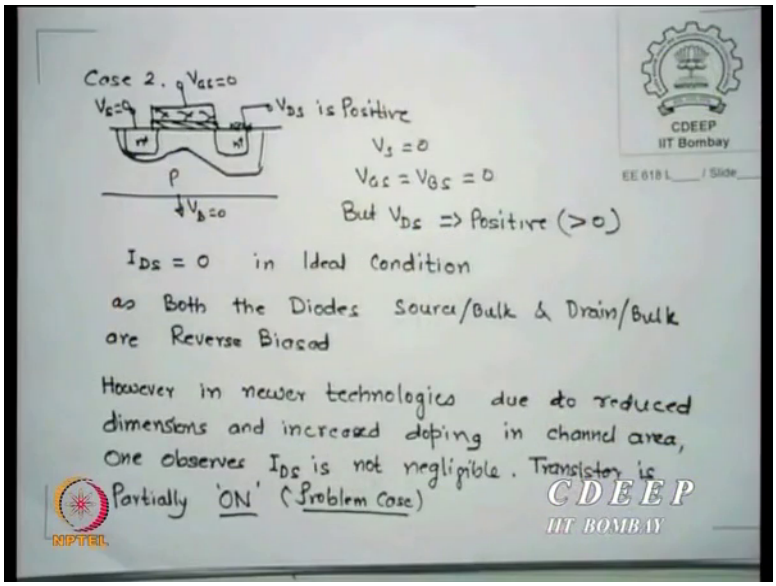

In case 2, let us say V GS is 0. So, gate is still first you will say ground source. So, what we say source is our reference voltage could have been anywhere, but over the years right from shock lay down everyone thinks source is why the word source came in the device here it sources the carriers nrp what your way and channel sources with electrons and p channel it sources holes drain d is called because it picks up drains. So, that is why it was given a name drain. Now this word gate essentially means if you open or close something ensured happen the output currents. So, it was given the gate and this B has to be given because it started with the bulk substrate and we say B.

So, right now we say V S is 0 we also say bulk is rounded, but p say we apply videos, no gate voltage, no source voltage, no bulk voltage, but we apply V DS which is positive let us say. I DS is 0 in ideal conditions you may find that there is no things getting 0 we thought that it should not be any equivalent you, but in reality there is there are two diodes sitting here np, np. If I apply 0 0 bias it is still reverse bias and if I have positive V DS and 0 here I am having a stronger reverse bias. So, both diodes are reverse biased and a reverse bias diode use reverse saturation currents is that correct. Since they are giving a

reverse saturation currents there will be a current from source to drain which is called the leakage currents.

The off state is always normally recognized when V GS its 0 we say when V GS input is 0 no current is a off, but in this case V GS was 0, but some finite current may be very small pico and sometimes on nano lames in present case it is becoming tens of nano hundreds of nanos reaching microns now that is our way of worry now in 11 nanometer, 16 nanometers.

So, this means that there is a leakage path. This we normally do not want to consider analog design because you say the [FL], but in digital this may hurt you hell particularly in dram designs this is what it will give you. So, one must say that pj 0 normally transistor should have been turned off, but in now newer technologies this is not necessarily can be called turned off. As I says called problem area which is called partially on keys is that ok. V GS is equal to 0 normally one believes device is switched off, but if V GS suggest there will be a leakage current which is essentially always available.

So, this is another problem which digital people are more worried not that we are not worried. So, this is the issue which will not deal too much in analog designs.

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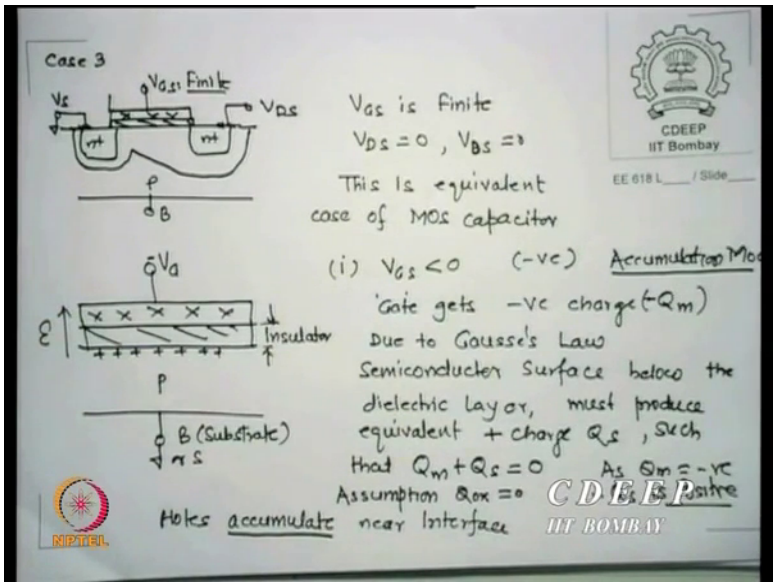

Now, here is the case 3, I have V S grounded V B grounded fine V BS is 0 I apply V GS which is finite; that means, finite means it can be positive or negative, but not 0 this is equivalent case of a mass capacitor. If this is grounded this is grounded, this is grounded, it is like equivalently saying you have a mass capacitor metal oxide semiconductor acting like a mass capacitor so obviously, a MOS transistor theory must actually a net from the behavior of a MOS capacitor.

So, here is a mass capacitor shown three voltages I can apply to V G, one I can apply negative other I can apply a positive, but small and third time I will apply positive fertilitively large value. So, three value the I choose one V GS negative, second one say which is positive, but small and third I say V GS positive enlarge, relatively large do not say large mean hundred larger than normal.

So, first we say V GS negative if I apply negative voltage on this metal plate please remember this is metal can be silicon also act like a poly, poly silicon can act like a metal their folds a metallic word we use. So, if I apply a minus V G on the metal plate with reference to the bulk which is grounded then the Gausses law does not like this system to remain like this [FL] it says that across the loop of V G to the ground the net charge must be 0 that is the system must be in equilibrium and that has to happen the charge there is no charger than insulator that is what we said right now. So, if there are no charges in insulator then whatever voltage I apply which creates a charge minus Q on the gate I must get opposite polarity charge in the semiconductor which is exactly same, but opposite polarity such that Q m plus Q S must be equal to 0 because the net charge around the loop should be [FL] electrical may [FL] nothing more, is that ok. That means, if Q m is negative Q S has to be positive which is.

Now, how do I get a positive charge? One sees that the device started with a p substrate. So, it has a certain number of hole density already available to you, but this is universal everywhere constant in each q Na, na is the doping concentration in substrate. So, those many holes are available everywhere, but at the surface I want additional holes because that is what you said minus Q m requires additional positive charge.

So, some way the holes must start coming near the interface the word is interface between SIO 2 and silicon or insulator and silicon are semiconductor line here is called interface, at the interface you must get extra holes. Now, from where there can come, is

substrate is good enough for you it will start providing larger holes of the surface, but does that mean that the substrate will get depleted of holes no, no battery of life battery will give you the addition. So, because of this why this can holes have to go upwards if you look at very carefully if this is minus V G with reference to ground which is the direction of electric field upwards plus to minus.

So obviously, holes move in the direction of electrically. So, holes move up and the sub additional holes which we are asking you will actually coming from power supply. So, that the thermal equilibrium value of concentration in p remains constant, the holes are actually picked up from the substrate itself the loss will be supplied by the battery or whichever go up. Now, this many holes will only come as much is the charge you put on the metal. So, every time equilibrium Q m plus Q S is constant is minty. So, if I have larger minus V G then what will happen larger holes will come. So, you can say larger negative voltage I apply larger accumulation of hole starts at the interface this is essentially accumulation mode we have accumulated holes we are a p type and we are accumulating positive charge. So, we say we are in a region of accumulation mode.

So, in a MOS capacitor with p substrate with minus V GS you are always in accumulation mode battery, always supplied charge cannot be created from here you know. So, it has to be taken from battery.

Student: (Refer Time: 54:06).

Now, the third case I say or second case I said V GS is positive, but not very large very small amount, but positive. Now, if I see that very small positive value.

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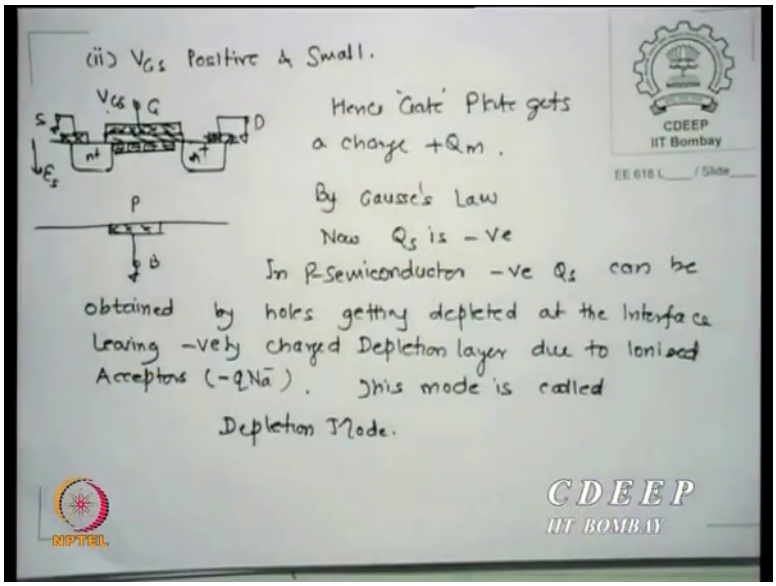

Let us look at this, if I apply V GS positive and small. So, I am putting small Q m and the metal now by Gausses' law we now expect semiconductor interface to get negative charge because Q n plus Q S is constant on 0 it is what Gausses say Gauss the God for us we say. So, it is be agree with it, yeah almost so many years no one has proved Gauss wrong, not even perturbation on it. There are many things in weak weak fields strong weak fields many things are coming bose on toes on, but no one has challenged Gausses law so far ok.

So, if case is negative, but the substrate is p type substrate is p type, now I want negative charge to occur. We said if you look at this way now the electric field in semiconductor is now downwards positive V GS, so field is downwards. So, holes can move in the direction of electric field. So, holes near the interface actually move away, as soon as in a semiconductor positive charge holes move away what we say it gets that region gets ionized with a negative acceptors and this region is depleted of free charges of holes is that clear therefore, the region is called depletion region.

So, we now get into this that we see depletion region. Now, this depletion region will enhance because a charge density issue if you increase charge the charge area is same. So, charge density of Q m increases. If cures has to increase its thickness must increase because there was equivalent charge density cannot be created. So, larger the positive V GS book depletion layer thickness or width as may be call will also enhance also

enhance to get same charge as you are putting on the metal. So, you remain in depletion as long as that condition is happening that Q S is to be supplied through depletion charge. So, this mode will call as depletion mode.

As I say many of you are learn this is capitulations because we need to understand device little better for analog.

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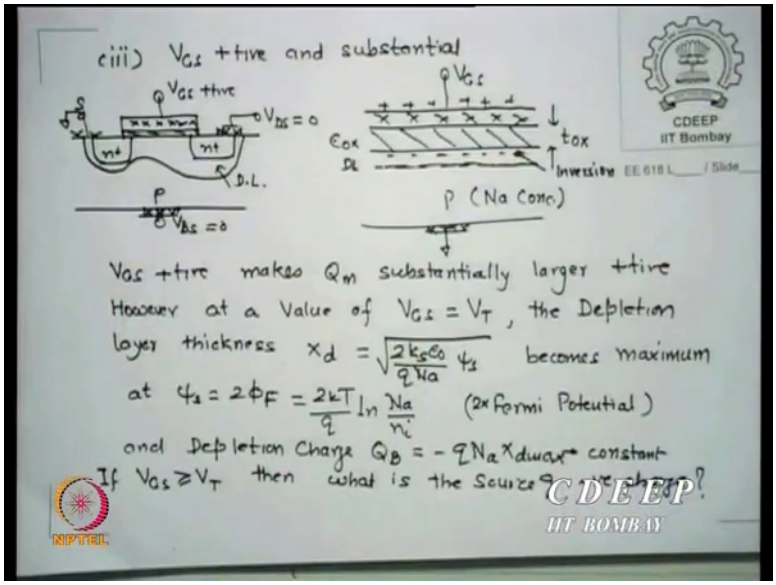

Let us say V GS is further positive and little better than substantially higher. Now, this value how much will see later when you say it is more than threshold that word threshold is what we want to define now. Certain value of V GS suddenly we find things will change and that word that we are exceeding that voltage right now as if.

So, if you apply V GS positive large. So, relatively large still keep V DS 0, V S 0 V, B 0 fair enough. So, you are still a capacitor and you say V GS is large, large positive charge requires, large negative charge. So, what could I have happened that this in thickness of the depletion layer should keep announcing because what is the depletion charge can anyone say already written somewhere if not oh yeah here. q Na X d, X d means depletion layer width this X d increases, Na is constants so q Na X d keep on increasing to adjust the extra charge you are asking for. So, the semiconductor charge is increasing with increase of X d in depletion. This surface potential psi s word which I has not stated somewhere maybe l can use a fresh sheet. This you should understand something like this.

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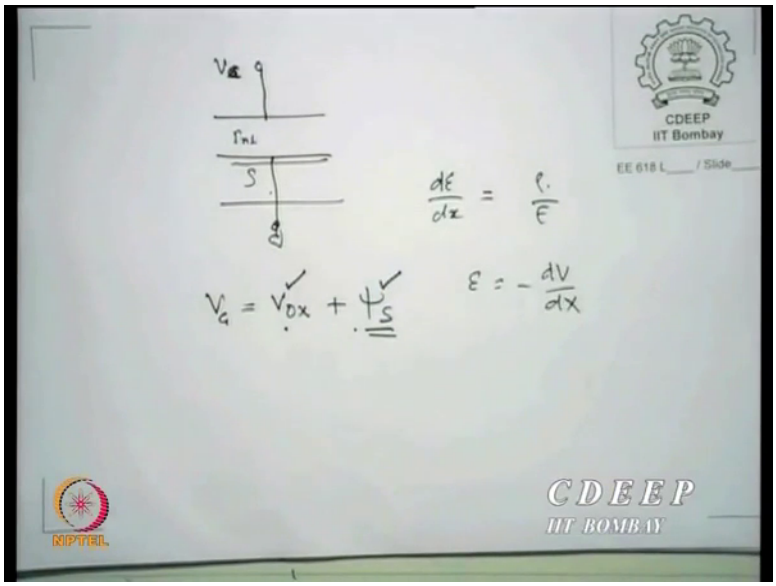

You have a capacitor, if I apply this is semiconductor, this is insulator, if I apply some voltage call u and V across this, this is insulator the semiconductor V must be equal to V ox plus semiconductor potential. This is Ohm's law you are divider you apply voltage to radius part divisions.

So obviously, the potential in the semiconductor is defined in terms of psi S and potential across oxide which we want to find soon is called oxide drop. So, if I increase a let us called V G either this will increase or this will increase or both will increase or one of them will increase is the game we are trying to play is that correct, is that point clear either each one of them will increase or both may increase or both may not increase which are the cases of relevance. So, this potential drop between two regions is we call it surface potential why it is called surface because charge is only near to the interface. So, potential will change only where by god which light potential appears because of charge, which law is the very famous which relates voltage to potential to the charge Poisson's equation, Poisson's law states d by dx is minus rho by epsilon e is the electric field x is one direction, but multi direction rho by epsilon, epsilon is the permittivity rho is the charge density ok. So, larger the charge larger is the electric field electric field is minus dV by dX. So, larger the field larges the potential is that clear.

So, we say voltage increase surface potential can only occur when there is a charge availability is that (Refer Time: 60:31) this is Poisson's law or Poisson's equation. So,

because of these as I say fundamental Maxwell's equations which are still standing strong electrical engineers are strong. So, now, if I say, if I keep increasing V GS psi S will also increase, but I figure it out that there is at some potential V GS equal to call it V T now, the surface potential becomes what we called as twice the Fermi potentially some other day maybe device theory may be more detailed a top, but not today. And Fermi potential is given by kT by q ln Na by ni, ni is a intrinsic carrier concentration, Na is the acceptor concentration.

So, if larger the Na phi f is larger. So, for a when psi reaches to phi f one can now say that this 2 phi f X d becomes maximum actually will see this is only one phi f should I happen, but we say 2 phi f X d becomes constant. If X d becomes constant and maximum then the charges due to depletion layer are fixed now, but you are increasing V GS beyond that value then what will happen, from where because depletion layer cannot enhance now you said it so that is the way definition you are putting. That means, there must be another source of negative charge this additional source of negative charge is always available day one actually, but was not so dominantly talk initially, but now suddenly we realized, we figured out that every semiconductor whether it is a depletion layer or normal thermal equilibrium areas, electron hole pairs are constantly generated is that clear to you. This is thermal generation nothing I can do the combination, it is constantly done there. So, any other constant so many holes can be given.

If law of MOS action has to agree every time thermodynamics cannot be violated in thermal equilibrium then electrons and holes are going to be created everywhere. Even that V GS was smaller positive there were whole electrons there also in the depletion layer, here also there were whole electrons.

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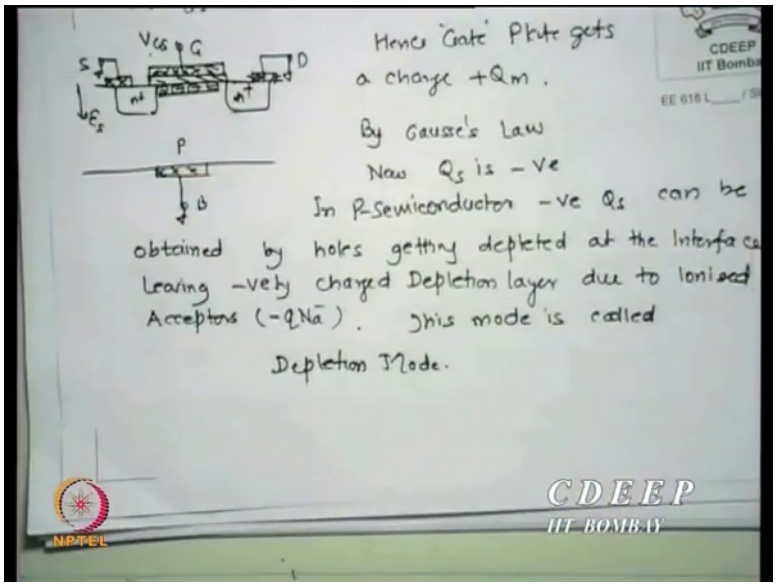

What had happened there? Which site because of the electric field which carriers in this in this upper region let us say the other region they will recombine because this is the neutral region. In the depletion region the whole electrons now see electric field which is the electric field downwards which carriers will move away holes.

So, the electrons can be made available, but at this time we say electrons are not there very much why we said because this electric field is so small that they could not separate whole electrons before they recombine they are recombining everywhere, is in the depletion layer the electric field which could have separated. What is the electric field are? It gives a force is that touch you into this is the force, it you into e is the electric force if you are e smaller the force on carrier is smaller. So, before they separate they combine. So, if they recombine there is no additional electrons real ability because whole electrons recombine.

However, in now when you have increased V GS sufficiently this electric field is very high because that is what V GS you applied size is very high now, at that electric field now you say depletion layer is not increasing fine, but this electrons and holes can be separated because of additional higher electric field in the semi semiconductor surface. The holes will move downwards and electrons will move which side towards the interface as they separate. So, more and more electrons start getting near the interface as you increase V GS is that correct because now depletion cannot give you additional

negative charge additional charge must come because gausses will not allow you to do otherwise and therefore, get you charge must come from free carriers electrons.

You started with a piece of straight you create add a layer of free carriers electron carriers. So, you say you are inverted p type the layer at the top or interface layer is now anti and therefore, you say you are in a region of inversion is that correct. So, larger the V GS now you put larger will be inversion charge because and that will be supplied by whom, by this thermally generated carriers which get separated now if I solve such the violence equation for this one can see if by of course, as I said theory I will not say. The inversion charge due to this thermally generated case its proportional to e to the power q psi as by kT which means very small change in psi s can create larger negative charge.

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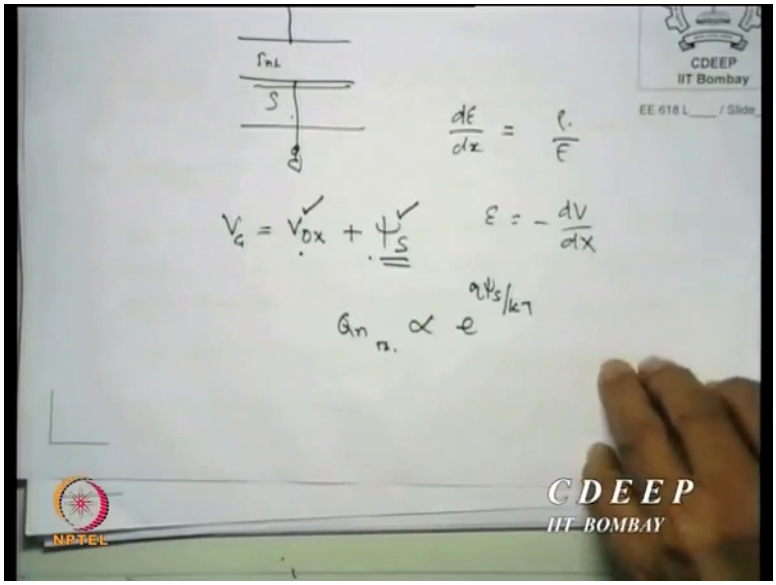

If you look at my this expression for depletion Q n na X d, but X d proportional to psi s, but which relationship it is showing root of psi s the in earlier depletion charge is proportional to root psi s, but inversion charge can be created e to the power q psi s by kT.

So obviously, exponential functions are stronger than root functions. So, you do not need now too much change in psi s to get this additional bulk charge or called depletion charge, but that additional charge may now come from the electron hole pair separation which is going exponentially with change in psi s. So, all the additional charge will be now supplied by this separated charges free charges and therefore, depletion layer will

become constant it is a pinch of sorry it will keep increasing a bit of it let us say 0.1 percent is from that and 99 percent from that may go it is not that it will not, but ratio as you say all of it is now coming from free electrons available through inversion layers through in the inversion layer. This is the crux of MOS transistor.

Now, we say V GS equal to V T this occurs the definition we said that at psi s becoming 2 phi f actually advanced when psi s becoming 5 f the material will become interesting you can put substitute this value and you say metal will be intrinsic. So, it will not p type there and the surface not p type say it entrancing. But then there are very few electrons, so we do not find that mean we want larger number how many electrons I say is good enough for me at least as much as the hole still below there. So, if this electron density is same as what the holes density I started with I say I have sufficient electrons available. So, I say good inversion layer and that word be good we say strong inversion.

So, from psi s equal to phi f to 2 phi f inversion is already available, but very less number of electrons available. As you reach to phi f huge number of electrons can be cleared because it is exponential function you can see exponential function initially it rises slowly and then shuts shoots up that procedure is same here. So, initially you see lesser charge, but then it shoots the larger charge. This fact is been utilized here there are little bit higher psi s 2 phi f is the number we gave the depletion layer now will become constant whatever for 2 phi f and will say rest of the charge will come from the free electron generated through thermally. That is why we say threshold voltage is defined at that point where psi s is to phi f is that correct. It is called strong inversion.

Now, there is a catch there between psi s equal to phi f psi s is related to V GS V GS equal to psi s plus V ox if psi s changes we know we V GS changes psi s is changing, we say between phi f and 2 phi f device is still not off it is on, is that clear to you. Why it is on because electrons are made available to you this means this region is called weak inversion and this is also called sub threshold region. One of the way analog circuit will be designed is using sub threshold characteristics. V GS less than V T, but it is not switched off its not 0 there is a weak inversion going on and that region itself can be utilize in some devices in some circuits. Most cases will not use it, we will see that psi s is two phi f strong inversion is set in more and more carriers will come from V GS now all of it go to psi s and psi s will increase as much charge as you want on the equivalent of Q n.

So, with MOS capacitor works and therefore, MOS transistor works is that there is a threshold voltage at which this can occur is that correct.

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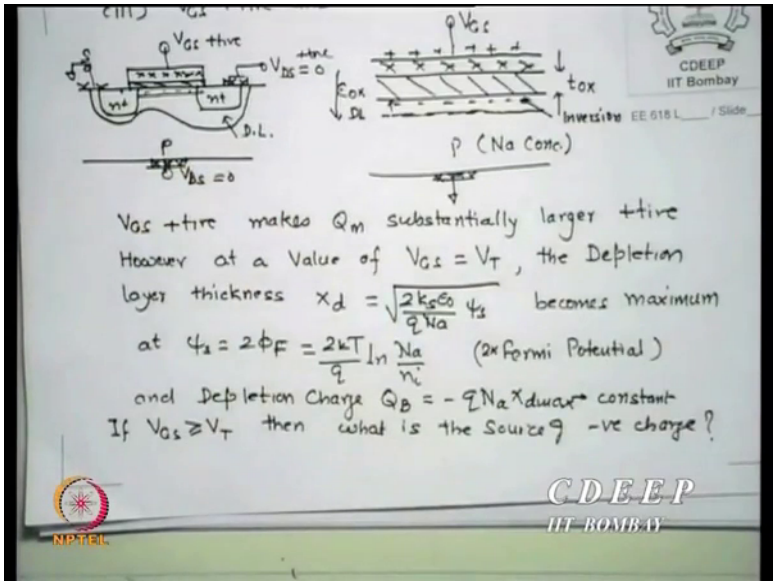

Since at this the as I said this figure since this channel can be created somewhere here f V GS is positive like this and V DS is also positive then there is a positive this is a like a register n channel n area is like a semiconductor n bar some conductivity it has this is source grounded, this is drain positive voltage this is like a piece of semiconductor with two contacts. What current it will flow? Ohms Law which are depending on the are here current will flow. So, a MOS transistor gives you a current which is proportional to b which is very interesting, but latterly figure it is not linearly going. So, then how about what makes it change will see you next time.

I hope that those who are not done device course in their careers or not done the course the way IIT and think they should do. I said the initial availability in a capacitor is essentially because of the minority carriers. However when I make a transistor I have a source of electrons infinite source. So, the electrons will actually come from the source and not from the minorities. Minority will keep that channel, but the current which will pass will be subcarrier supply otherwise you know one time this carriers will be swept off.

So, the carriers which are required to maintain a channel will always be supplied in a transistor by source electrons, that is why it is called source I will keep giving a electrons

as many you want and this is n plus means heavily dope infinite carriers. So, I will keep supplying any number of current carriers required, but the channel will be maintained essentially because of the V GS minus V T available, is that clear. This inversion cannot be done from source side it can only be done from gate side. So, the inversion layer maintenance is because of the minority charge, but the charge movement is supplied from source to drain by the source is that clear. All the carriers there are thermally generated there is nothing else a inversion layer is always thermally generated carriers is that ok.

Student: Sir, metal is not supporting any (Refer Time: 73:00).

Metal is insulated by a from the semiconductor now, there is a oxide so nothing it can do a below is that clear.

Student: But (Refer Time: 73:09) metal any substrate it can (Refer Time: 73:10).

No, how can the current can flue move through a insulator. You may like this over that is the circuit in a way circuit the cap, that is what is say curve finally, carriers through source from where it is coming through battery there is no other source of carriers. Carriers can only appear from a battery, there is no other source, is that ok.