CMOS Analog VLSI Design
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Lecture – 29
Oscillators

We were looking for oscillators and pardon oscillator which is used in most of the circuits, analog system as well as digital.

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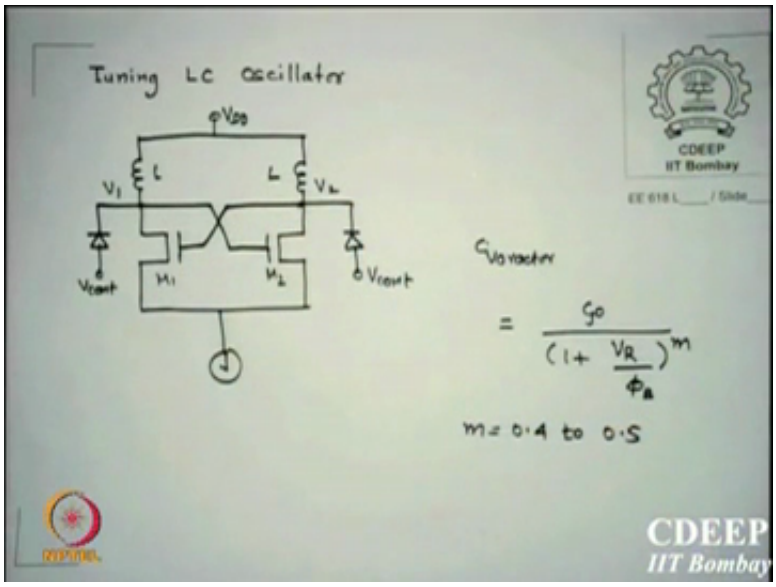

Is a VCO shown here which is a tuning LC oscillator and here the capacitor is essentially created out of a diode which is called varactor because a variable capacitor with voltage or variable reactance, cap the other word. If you know a PN junction depending on whether it is the abrupt junction or it is linearly graded or exponential, the reverse bias capacitance can be given by 0 bias capacitance divided by 1 upon 1 plus V R by phi b, where phi b is the built in voltage of the junction, V R is the reverse bias and m is the factor which is decided by the kind of junction I have. For example abrupt junction is half, it is one-third and in between it may vary from 0.35 to 0.5 depending on the grade you get, get constant you get there.

Typically in most cases 0.35 for one-third is assume because the exponential function in a long range acts like more like a linearly grades, but it is not 100 percent true because if

it is a error function profile it may be slightly different, caution may even little different than exponential.

So, please take it that values are normally provided by the technology people for their device. If it is half then it is much easier to find 1 upon c square V is a straight line. So, the slope is the m factor. So, now, with this in this case the diode the V R essentially stand for the reverse bias, phi V is the built in potential which is for the given junction of source drain in the substrate that is the same diode I will use that may have the typically 0.7 volt or 0.65 volt kind of built in voltage. So, I just have to vary the controlled voltage to get variation in capacitance and you remember larger the voltage I apply smaller is the capacitance.

So, the range up to which I can do is from the cj 0 to a lower capacitance that is higher frequencies. So, at the at cj 0 it has the lowest frequency and as I increase voltage the frequency will also increase because capacitance will decrease 1 upon 2 pi root LC, so C decreases frequency increases. Of course, for a 2 large voltage the breakdown may occur and normal PN junctions in a CMOS technology may have breakdown or 6 to 10 volts. So, do not go beyond 5 volt or something normal devices do not permit more than 5 volts.

I can make diodes which are as they are called power rectifiers can stand 5000 volts, but this is not a power rectifier. So, it is a diode which is the out of a normally even each PN junction is surrounded by an N plus region which is called guard ring, which does not allow currents to spread out the reverse current. So, some other technology something, but this is what essentially and so it limits the breakdown for very low values. So, typical voltage which you can apply is 5, 6 volts and no more. So, the variation with this, whatever is possible that is the maximum range tuning range with this CMOS technology will allow you for the VCO.

The little bit of math's be of interest which we already done, but I repeated again for the clarity, this is called mathematical model of a VCO.

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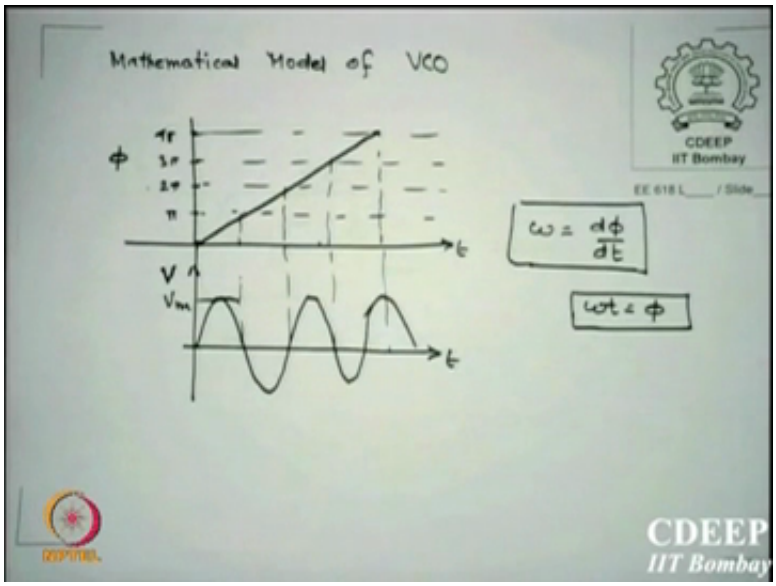

We know if I write a voltage V is equal to vm sin omega t or cos omega t, omega t has a unit of phase that is what it is the omega t.

So, one can say that d phi by dt is essentially omega, rate change of phase is essentially the frequency or angular frequency. So, if I plot phi versus t and if it is this kind of relation exist it will be a straight line; that means, the frequency is constant and corresponding to this you may have a sinusoid which may have a peak voltage of V m here. This is V m sin omega t or cos omega t depends on where they starts at 0 or is started half ok. So, this has a frequency decided by, you can see the way it is the phi actually represents the frequency that the phi t curve essentially represents the frequency pi 2, pi 3, pi 4, pi correspondingly d phi by dt is constant here so is sinusoid actually has the same frequency.

So, you can see d phi by dt here in 1 1 and 4 2 pi there will be one sinusoid and it repeats. Now, if I have 2 signals, V 1 and V 2 which I have different frequencies omega 1 and omega 2 or has 2 phases phi 1 and phi 2.

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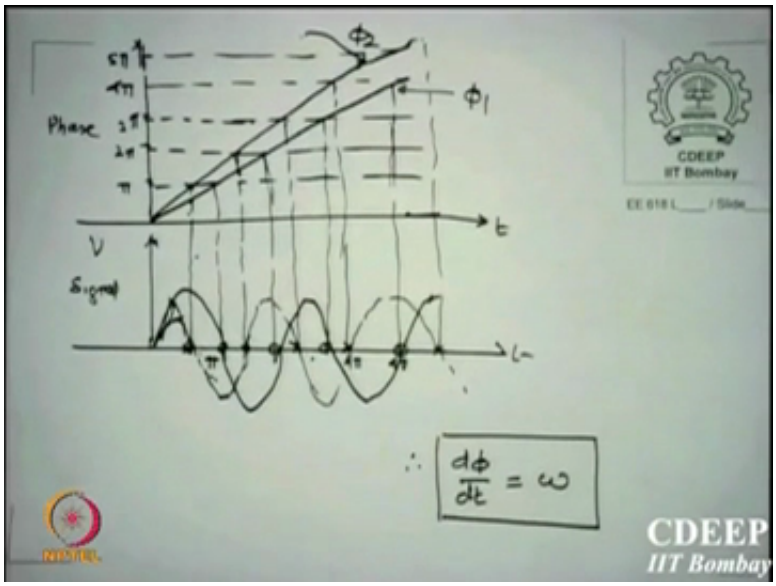

If you look at this, if we just to prove what I made statement, this has a higher d phi by dt or this has a higher phi 2 has a higher d phi by dt then phi 1, slope is higher there. So, if you came now I can do the same thing here for pi 2 pi 3 pi for each such angle I figure out the frequency and you can see from here for d phi by dt higher this point is on the left compared to the lower one, which means the frequency of d phi by 2 d phi 2 by dt will be larger, we can see from here this moves has a larger frequency compared to this one.

So, essentially slope of phi decides the frequency of operations this fact we actually utilizes, utilize in PLL S that is what we do, phase and frequency are related. So, if I can control phase then I can control frequency that is exactly what we are looking at. So, this figure this, is this point clear to you what I said that if I have d phi by dt larger or smaller is essentially means the frequency is larger or smaller corresponding to it and that can be depicted if you have drawn the. Of course, this is 3 this you can always draw 2 lines, put 5 pi, 2 pi points and you can see the frequency here is lower compared to this which has because larger d phi by dt will have higher frequencies, this is just to prove that point which I said and given in many books including Razavi boys baker and everyone.

So, the statement I have making d phi by dt omega is a valid statement and therefore, we can represent any phi t curve, this is t curve into its equivalent omega curve.

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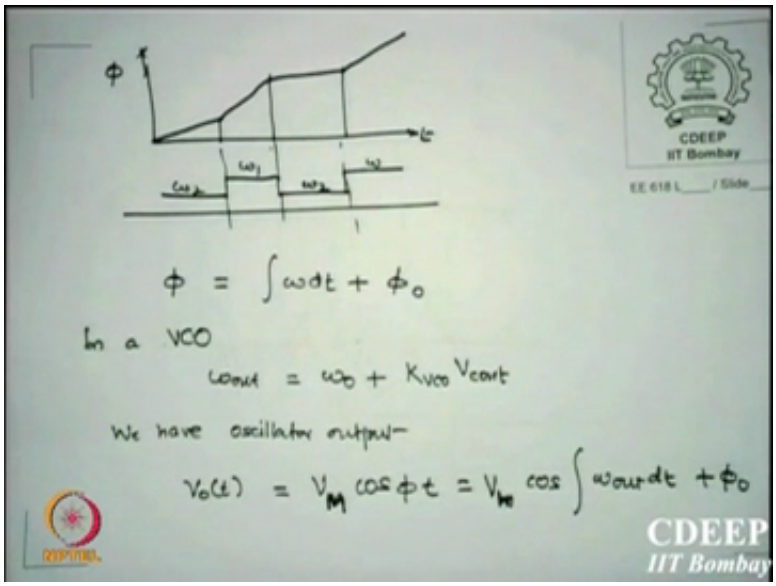

So, we say if this is the slope then it has a frequency omega 2, higher slope it has a frequency higher than omega 2 which is omega 1, as long as this slope is maintained frequency is omega 2, let us say same phase same slope again occurs. So, you go down to omega 2 again it rises at the same slope that, if it is different it will have a different frequency. So, this and this are essentially same.

So, mathematically if I say d phi by dt is omega. So, integral of phi phi is equal to integral omega dt plus integration constant which is phi 0 which is called initial phase at t is equal to 0. In a VCO we have done this expression earlier that omega out is omega 0 plus some constant of the VCO, KV CO into V control this is the principle of VCO.

Now, we have a oscillator output which is say let us say given by V m cos phi t. So, I represent cos phi from here in this expression. So, I get V m capital V m maybe you can take because I have use small m again. So, if I write V m cos integral omega I dt plus phi 0. So, I now say the output voltage of a oscillator has this kind of representation is that clear, if this is what you agree then this is what you should also agree. Why are we trying to do, we want to figure out this is very important and that is what PLL S are used or worries are if let us say this control voltage which I am going to apply is not constant right now for example, if I substitute this I think I have made cos omega I allowed to write now cos this omega out in here also.

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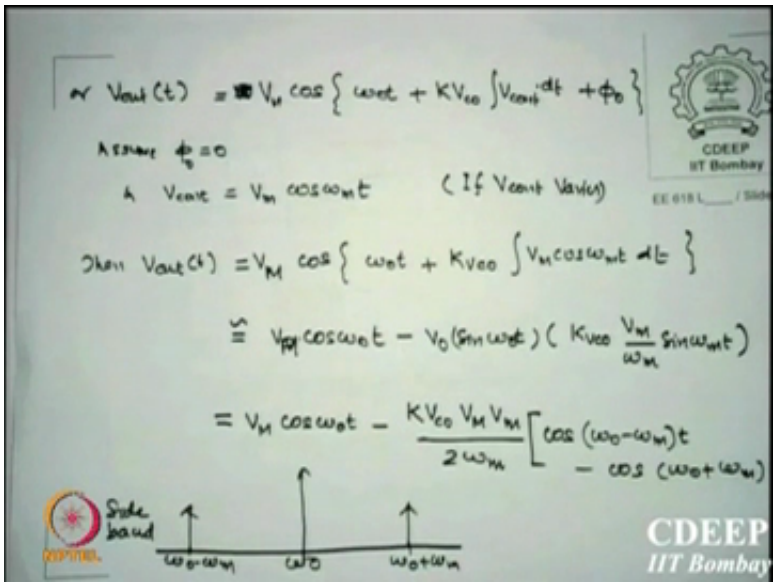

So, maybe I do that first. So, if I allowed this V capital m cos omega 0 t KV CO integral V control dt plus phi 0 this is the expression I will get for V out t, if V control is constant then there is not much an issue, but if it is not constant and noise overrides. So, let us say generally the way it is expressed assuming right now phi 0 is 0, initial phase 0 V control has V ms cos omega t as its voltage which is a sinusoid controller which may be overriding the dc value of V control. Now, if that happens I substitute for V control V m cos omega mt here an integral expand it integrate and expand it and leave some terms which are smaller. So, I get it is V capital M cos omega 0 t V 0 sin omega t KV CO V M you can expand and get this kind of express.

Just put this integral here expand small term be neglected and you get this, now if you see now I can further do little adjustment here and this can be done written as V m cos omega t minus KV CO V M, V M upon 2 omega m into this cos omega. This is omega 0 plus omega m term and omega 0 minus omega m term, if omega m is not present this whole term will go away and what you are expecting would be essentially receives. So, control is constant you have a excellent oscillating frequency at omega 0, but if V controlled varies you have 2 other frequencies surrounding it which are called side bands, these are essentially noise bands ok.

So, some energy will be lost in sidebands. So, in many cases how do I retain control voltage constant or noise free that is essentially what we are saying we will do through

PLL is that clear. So, this whole issue of math's was shown to you that if there is a change in control voltage that reflects in sideband power which is lost to you because remember if this is not present all the power would have in the spectrum would go to omega 0, if not part of the power will go on the sidebands.

Now, this is very some in real life and one must actually see that your frequency does not change of course, there is a word which of course, it when it comes I will talk to you later. So, is that clear I am trying to see that, why it should be some locking has to be done for the reference which I am creating and that is done through a system which is called phase locked loops of course, they have many other features, we will see one of say or few of them. I saw that this course is concerned this is good enough PLL may not be of course, except for the bonus part or some small queries no mathematical theory because it is a huge area I can actually spend these 6 hours to 8 where 9 hours only on PLL designs.

By the way most of the Indian so called startup or industries in Bangalore or Hyderabad, Noida essentially are making PLL S of different varieties, different IPs they create as they have major bread and better. So, do not think PLL is very trivial PLL is very very strong chip which so many people need different applications. So, is that point clear; that there is a sideband power loss if control voltage is not retained constitute.

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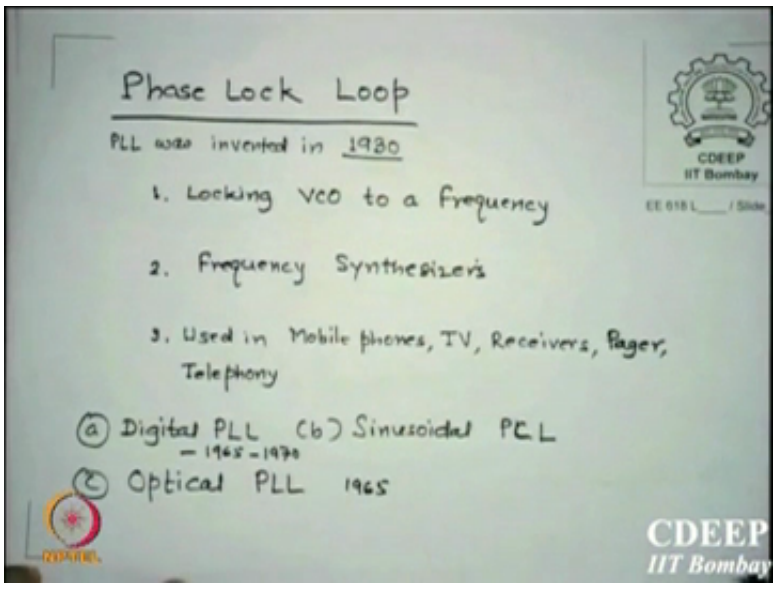

So I start with phase lock loops, as I say for most of you people may not be aware, but this was invented as early as 1930 ok.

So, it is not a very new thing or something, phase lock loop was word was known and even circuits were made as early as 1930; however, the first digital first IC PLL came in 65 and first digital PLL in which digital signal were locked appeared in 1970. By the same year 1970 even sinusoidal or analog PLL were observed or actually made and similar time there were another PLL was used in optical signals and they were called optical PLLs. So, it is not just electrical signal, phase lock loop does not have to do about electrical signal any signal you somehow phase it back adjust it you get it called PLL locking.

So, these are something where you can use it, lock the VCO frequency I want VCO to be or whatever frequency I am using that should be constant VCO may generate something, but I want that frequency should be constant of my choice I decide what is my frequency. Using VCO and PLL I can actually synthesize, I can increase the frequency or divide the frequencies. So, it is called frequency synthesizers and almost every mobile phone or every television or every other kinds of receiver pagers telephony optical transmissions everyone uses PLL S in one way or the other and I keep saying a small company called core actually have 80 IPs produced last year on the PLL.

Just like a small company or 24 people of which 4 of IITB students and they produced 80 PLL chips as an IPs. So, you can see the business itself only for that company small company is on PLLs. So, think do not think this is trivial this is very money making system right now.

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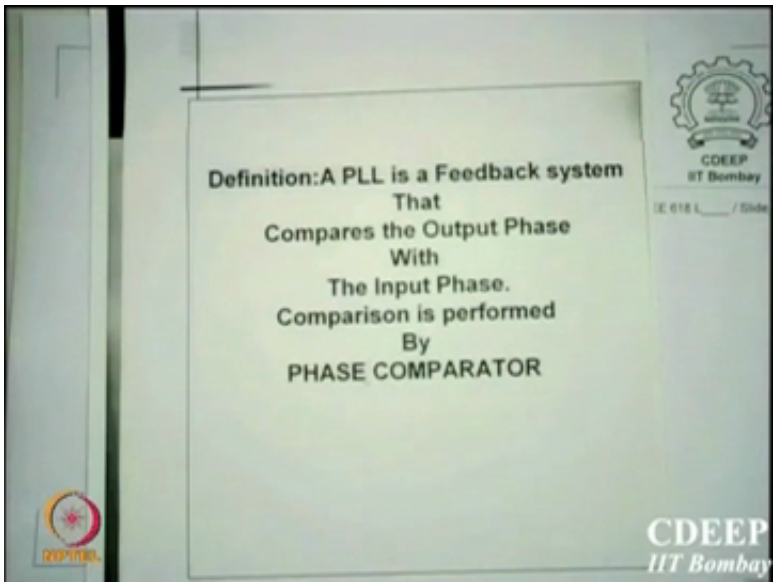

A typical definition of the PLL since I am not teaching this at the power I did not prepare heavily for every word of it. So, some game [FL] as I say if you really need some maybe next semester, next citizen course we insist that they should teach you there if he or she who does not want to be there I will come and teach that part ok. This is very important area from I like this many of my students are developed is PLL. So, I will like to actually tell you how what is the problem.

PLL is essentially a feedback system that is what I say control. That means, it must have some feedback control, it compares the output phase with the input phase please remember phase and frequencies are related is that clear. So, do not think that phase connection is this, the comparison is performed by what we call as phase comparators FC we will say phase detector first and that we will detect compare as well. So, you call PD or FD, FD called frequency detectors, p stand for phase detector and together you call pfd phase frequency detectors. Normally phase detectors are sufficient, but much more accuracy and much longer range capturing if you want you may need a pfd, that also can be fully digital circuit which is called charge pump method some other. So, first comparator is essentially what we are looking for.

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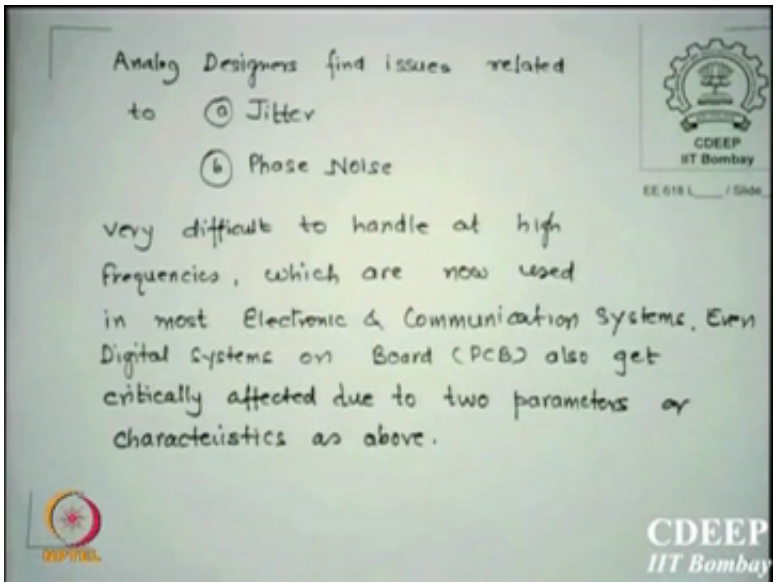

I suppose some of you are communication so you must be aware of these 2 terms, but for microwave term is should not, it should not be Greek and Latin.

So, let us see what is a jitter and what is a phase noise? This is something which I always want to tell people, there is a confusion and there is not a clear understanding between the two though they are similar if not same. So, please our major worry in all analog designs are occurrence of jitter or equivalently saying occurrence of phase noise, it is very difficult to handle these jitters or phase noise at very high frequencies and we are working these days on gigahertz, is that correct we are working on gigahertz and at those frequencies this is very difficult to handle.

At lower frequencies this typically I may tell you there is a word which is common anything below 1 megahertz the change in frequency or change in phase is called drift and in if you have a my timer we used to call wonder its wandering. So, now, it has changed to drift, but anything beyond 1 megahertz it is actually called jitter or phase noise depending on which way we explain it. Please remember even on the board if you have chips and interconnects PCB for example, these 2 parameters there as I say is essentially similar, but not same they are very important in board designs. So, not now remember the board design of 90s or 95s are become chip designs of 2000 plus because now you are integrated more, but the same issues which were occurring and the board

has now common silicon itself. So, the design issues are same as we earlier looked into board designs.

So, let me tell what exactly is these two words which comes into our mind, jitter and phase noise. I will not derive the expression for this how to derive one from the other look from some Google paper you will get it.

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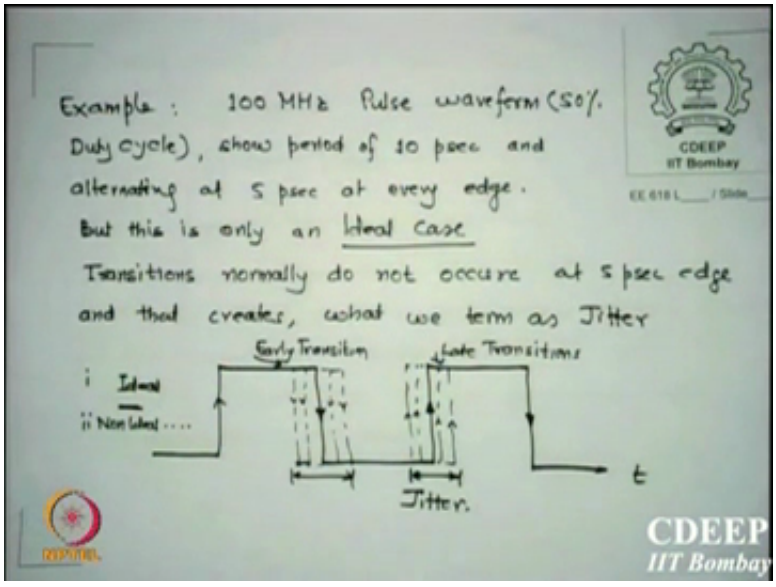

Let us say we have a pulse of 100 megahertz and let us say duty cycle of 50 percent that is square wave. So, we believe that if it is 100 megahertz pulse the pulse period should be 10 picoseconds, we believe that actually and it alternates at every 5 picoseconds it should come in every 5 microsecond. But, this is only if you think you are right that is ideally it should happen that and if it does not, the difference which is going to come is essentially called jitter.

So, one I have shown you, this is your ideal pulse which you are expecting, this is the period. Now, what happens in actual transitions they can be early transition or they can be a late transition, so the maximum early to late transition width in time is called jitter. There is a early transition, there is the late transition the max min difference of early to late transition is called jitter, ideally what should be jitter 0 because I do not want any all transition to occur at 50 percent duty cycle if I fixed it at t by 2.

But if it does not what is the range in which this can change the and any time change essentially we will say t plus delta t or t minus delta t which is equivalently saying in omega terms there will be a change in phase for that, omega t plus something means time shift means phase shifts have occurred. So, jitter essentially gives you phase shifts those who are communication again they know much more about this, but from a microelectronic side few more words are important for both jitter and determine this phase noise.

If you are written down, as I say these are I mean these are interesting part and I do not want to spend hell of a time on these, but I wish I will have a time enough to really teach you a period. Something you know in digital I like to teach memories for long simply here I want to teach PLL , but somehow my course was so organized by me and no time left to those PLL s and I was told by make signal people they do teach that so hopefully they do. In case you take that is also a elective in case you need you can, all RF people all analog people all digital people need a PLL come what made irrespective.

If it is only digital we say DLLs, but DLL is also one other name called delayed low lock, delayed delay loop locks. So, there is a difference there also so please do not confuse with dpcl, dp, dpll and dlls some books do not differentiate, is that where this is trivial. So, jitter is the maximum spread of time in which signal can shift from high to low or low to high is what we called as jitter.

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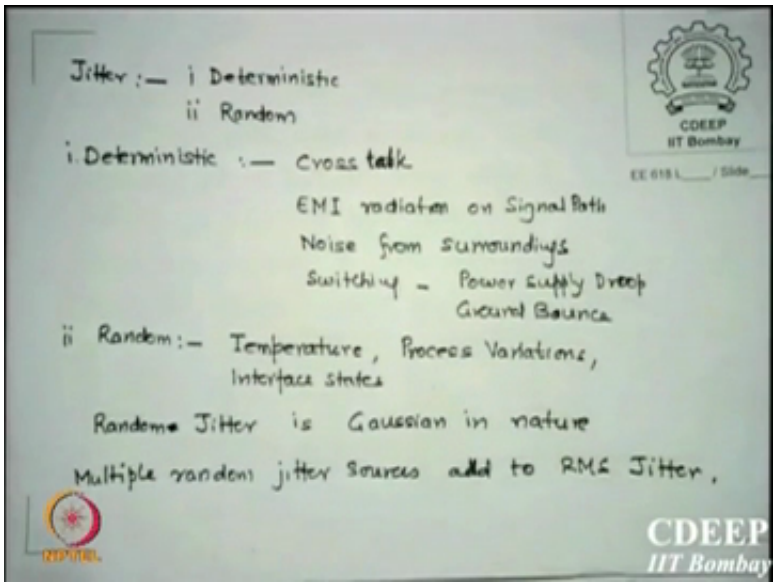

There are 2 kinds of jitter seen one of course, is deterministic, the other is always the random one. Typical deterministic jitters are crosstalk, 2 lines closed by signal going across one can have mutual coupling between the 2 and depending on the direction of signal going it may have a larger coupling or it is smaller.

If they are opposite in direction there is a larger coupling, they are in senses lower coupling, forward crosstalk, lowers crosstalk. Forward is easy comparative to maintain, reverse cross talks actually boosts the values too much and difficult to organize them of course, then there is a EMI, electromagnetic radiations interference has the word growth these EMI radiations may come from the next line which is resonating at high frequencies or may come from other systems around in the block, other chips can actually have this or in a [FL] of microprocessor or such thing either come including my power supply may actually emits EMIs EMs.

So, if there is a EMI in signal path we actually get into jitters and same way word is if not electromagnetic even the noise, simple noise can be coupled between the 2 because of mutual couplings. So, there will be noise surrounding which may actually over read the EMI radiation coming from outside. So, they are similar, but different sources and finally, there are 2 digital people are much worried that in a block of circuit, lot many inverters or lot many days all of them switch one move. Out of 8, let us say your quad are 8, 8 in 1 and 8 switch together, they may lead to 2 major worries there we call power supply droop and ground bonds that is the (Refer Time: 25:36) will shift up power supply voltage may go down. These are also essentially deterministic, they may need any change in anything will lead to jitters ok.

The other of course, is random and in general if you have from micro Newton is we always look in to the upper part which we think we probably has some control, if you are a communication plan he is very happy here or she is very happy here no control. So, she is very, he or she is very happy, random is essentially may be because of the temperature, may be because the process variation, may be because of the interface states, different interface states and since it is random most likely it follows Gaussian in nature. Gaussian distribution it picks up and since there can be more than one jitter sources average value of you have to calculate it is called rms jitter.

Please remember these are like a noise so noise is added up, so same this is also added up. So, jitter is something this of course, deterministic jitters can be of drift whatever will come we can offset it, we can some compensations we know how much. So, we compensate partly for example, if you want cross talk between any 2 interconnect line put a ground line it is space extra space, but every signal line is surrounded by shield which is the ground line. In normal cable you have a shield on a chip there is no shield. So, you actually every alternate line is a ground line ok.

So, only link between ground no signal on that, so that is how coupling can be minimized anyway at the cost of both size or silicon size.

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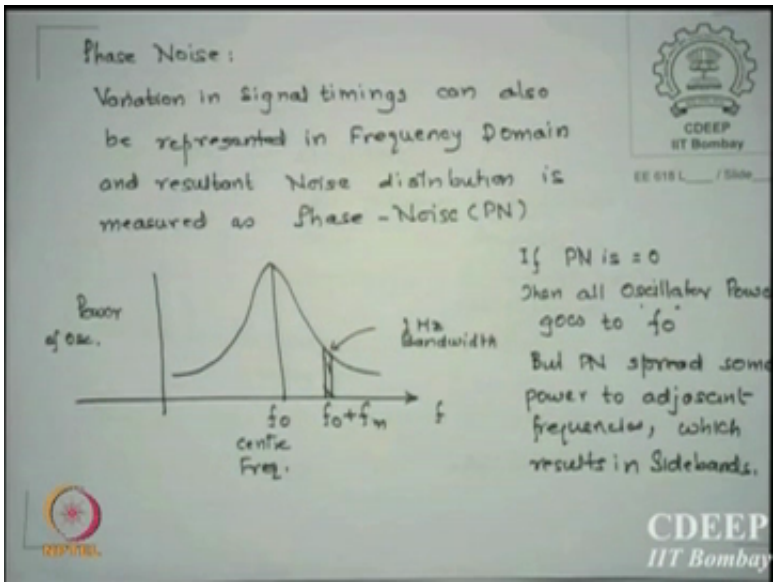

The second part is phase noise, which is as I say it is a relates a term, but not same. So, if you have a variation in signal timings they can also be represented in frequency domains and normally they show a Gaussian distribution on this time. This is let us say ion oscillator whose power is shown here against frequency, if there are no jitters or there is no noise all the power should have gone to the tailor frequency which is my center frequency f naught ok.

So, at that time oscillator will oscillate at that. So, no issues find every, but if there is a distribution like this as shown here, some power is actually given to adjacent frequencies which results in sideband just now I showed you this same word shown here. So, now,

we define a phase noise out of this, you can see what I do at this frequency of whatever band it has come f 0 plus f 1 fm.

Here I take a bandwidth of one hertz and figure out what is the power density here total power and then integrate all the power which would have actually have got integration of total at this power and ratio of the two is called phase noise, is that figure drawn as I said this is not necessarily part of a our course per same design. But good designers must be aware of everything this otherwise, when things do not work we do not know on what to explain it may still not work, but at least you should be happy it is not working because of this. So, that because what is how we know about and this spec is specifically normally given to which you how much phase noise available or allowed there.

So, it is not that this is not a spec, this is a spec.

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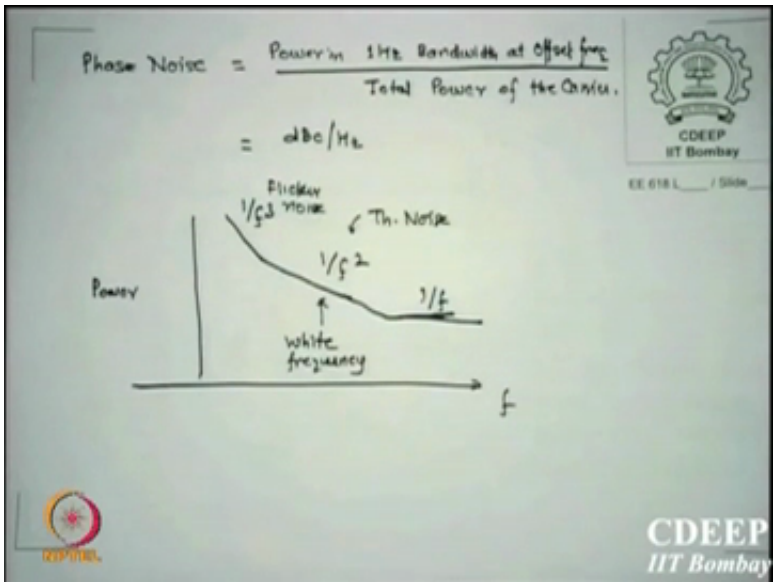

So, phase noise is defined as power of 1 hertz bandwidth of offset frequency that f 0 plus fm is the offset, at that 1 1 have bandwidth. If you find the power there divided by total power of the carrier then it is called the phase noise and it is always expressed as gv with reference to carrier divided by hertz dBc per hertz. So, we must actually defined like an error, if you have a solving a numerical analysis what is the way we do it, within this truncation error all what is the error about we say truncate things.

So, your PLL be a particular error [FL] stop [FL] what is the permissible phase there are 5 percent, 1 percent, 0.5 percent you decide design, that much time it will go through loop and will actually settle, yeah actually 0.5 percent sorry most permissible phase error is half percent.

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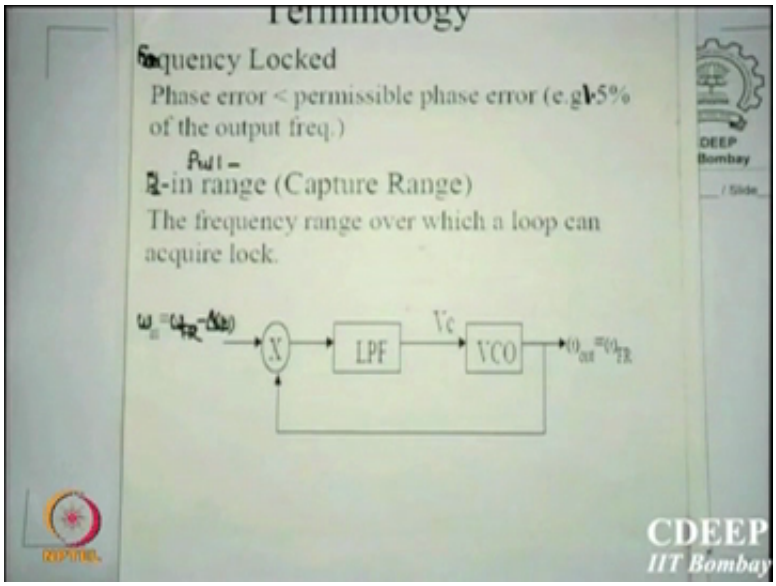

Now, there is a circuit which is shown below which is more like a PLL, we have a summer here, we have a low pass filter and we have and we want to have output frequency same as center frequency, VCO is the output frequency should be the same as and there is a variation in input frequency from the center frequency.

So, as soon as you that small delta t occurs this loop will operate and will bring center frequency to close to VCO frequency or rather opposite. The VCO output will be exactly same as your reference output of frequency you want, even in jitter there are a few other words which of interest to some. This sigma part is essentially is what it does by a detector phase detectors no, no this delta t is in the omega form itself 0.5 percent that is that if phase for the center frequency whatever is the phase acceptable to is half percent. That is if let us say I have 1 mega or half percent equivalent phase whatever is allowed their lock should stop.

Let us say 1 megahertz half percent change is 0.99 megahertz, 0.996 megahertz we do not want to go beyond further to make it 1 megahertz. So, it lock should stop there, ideally it should be 0 it should log exactly at that frequency, but it may not because the

components can never give 100 percent locks. So, [FL], but that should be permissible for you [FL] jitter [FL].

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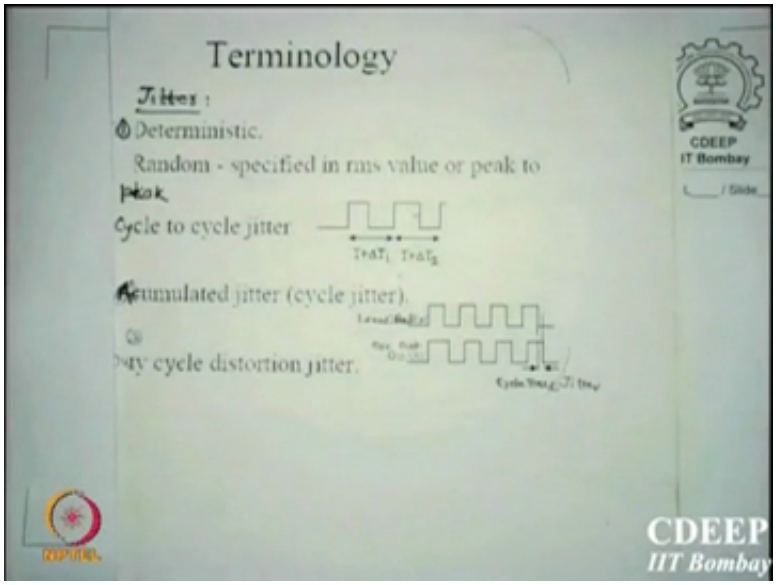

There is a word which they say cycle to cycle jitter like for example, here it is d plus delta t when the next time it is t plus delta t 2 first of course, is the rms value. So, average value of that is average rms not average rms value is normally taken for peak to peak or rms 2 values of jitters are measured.

Then there is called accumulated jitter over a given time, after certain cycle how much is the net jitter occur to you it is called accumulated jitter for example, here you can see now it is small small for f band, this may be large enough a jitter and that may change your final phase itself. So, that is the accumulated jitter is also specified 5 percent of course, I am doing a jitter and duty cycle distortions 50 percent may become 49, 51 that also can create more problems.

So, these are essentially either is a terminologies in PLL books or PLL chapters if you read in a analog book, as I said we are not going into huge detail of that some other days some other time or some other people.

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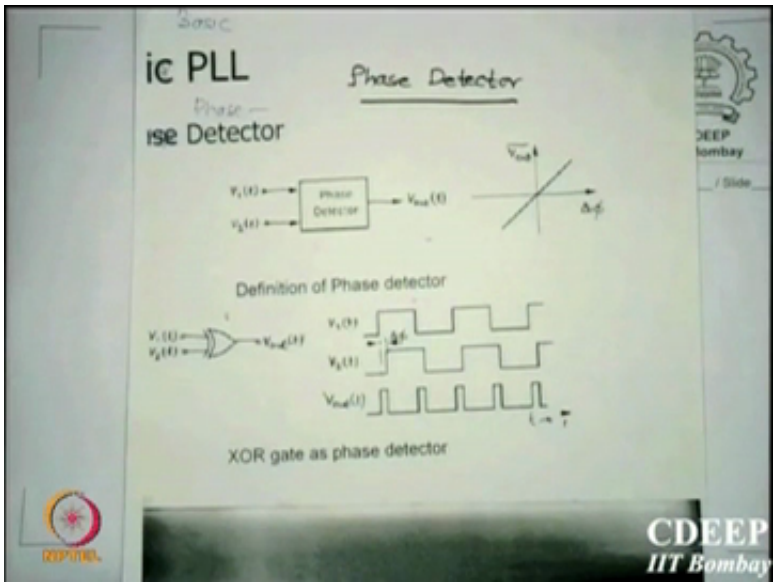

So, here is a phase detector part which essentially is shown here, they are 2 sigmas V 1, V 2 which passes through a phase detector and create an output and the way we actually are looking right now is the phase difference which is delta phi and the average value of this we have should be linear. Now, definition because this is one which is going to control the VCO frequency which is the control signal of VCO, typical phase detector could be as simple as an XOR gate, if you have 2 sigma's V 1, V 2 in the square form you can see at every this is an XOR.

So, whenever they are not same values the output V 1 otherwise are 0s, since there is a jitter between these 2 at this frequency this is 0, but this is 1. So, it rises it becomes 1 at this point again this is 0, but this is 1. So, again come down. So, there is a small width pulses or markers come depending on this jitter you have and you will see once this kind of output voltage this, then you take an average of this is that correct how do you take average filter.

So, you will get a only average value of that, that value you feed it to V control and shared frequency is that the point is trivial, but that is what it is I have just copied from Razavi some other things. This is of course, is trivial as I say this is the DLL part essentially it is only simple digital phase lock loop which is shown here, there is also a problem of jitter in PLL , there is the jitter in signal and jitter in phase lock loops [FL] issue [FL] second loop [FL] stability [FL].

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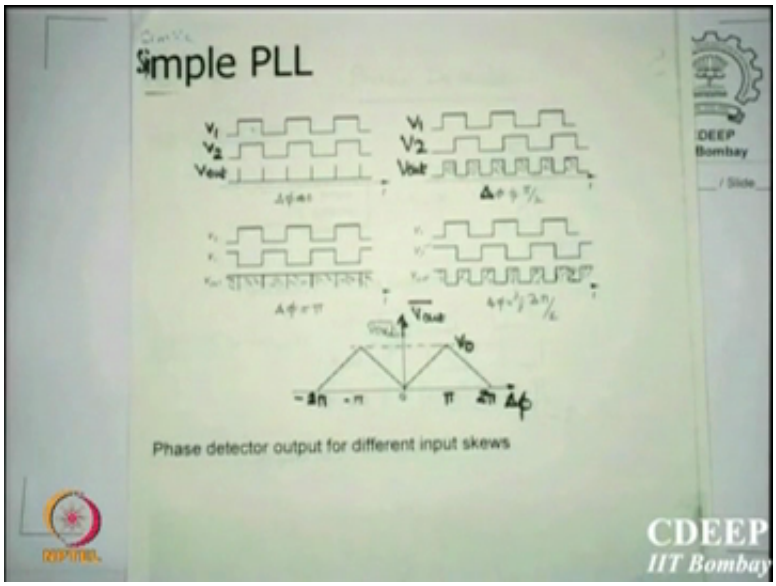

So, there are issues and issues the 4 cases that I was discussed if between the two V 1, V 2 there is no change in phase.

So, only at the you know for a very short duration transitions occurs. So, the output also transits because this even if we say it is 0 it is not level 0 so it is marginal. So, it gives markers; however, if it is pi by 2 as it is shown here 50 percent. So, for this time 0, but half the time there is 1. So, you get an output of square waves of this kind, is that correct 50 percent of time you can see here, this is one this is 1. So, 0, but this is 0 and this part is 1. So, wherever 1 0 occurs, a 0 1 occurs xr we will give 1. So, correspondingly you will get such purses and you what you actually you have to do is a average of this is your control voltage integrator also can do the same ok.

Then you have pi, opposite face opposite markers, the transition wherever goes strongly negative we will show a mark on that. If it is 3 pi by 2 it will give a different frequency part in this and you will get again pulses. So, depending on the skills you have, you can always get the output and this output when erased can change the VCO frequency and bring it back V 2 and keep comparing between V 1 and V 2. So, that finally, they lock to a close by value up to 1 cycle, yes 1 cycle phase ranges this phase detection is possible and ranges on scroll locking is also possible.

More than 2 parties second clock starts no lock starts, it does not pick up it should follow this models rectangle model.

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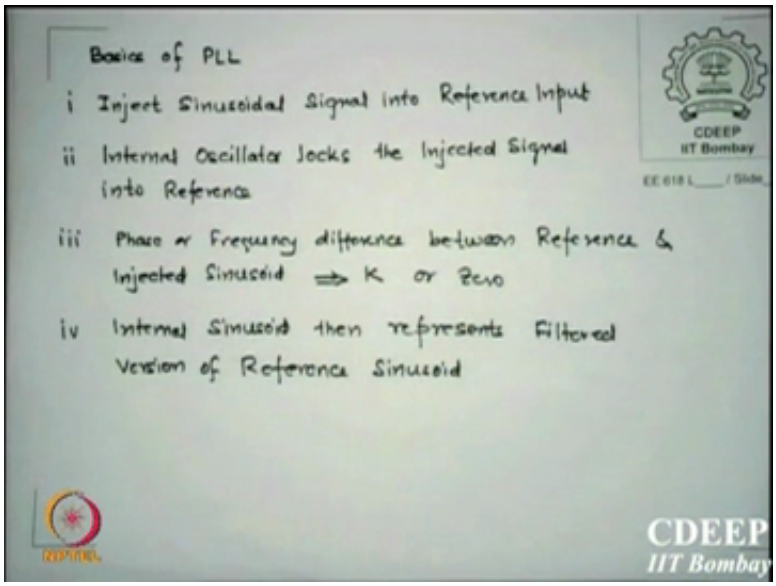

So, before we click PLL there are a few interesting things about PLL which analog PLL S use or analog signal processing people use is they inject a sinusoid signal into difference input which is the frequency at which you want the reference signal. The internal oscillator means VCO, locks the injected signal into reference that is what you want whatever this it should lock to that phase or frequency difference between reference and injected signal is proportional to the k of the VCO all right if it is locked it goes to 0.

And internal sinusoid then represent the filtered version of the reference sinusoid and that is what you are looking and that you use as your output of a VCO is that clear. X implies g minus gmc filter k the gmc oscillator k fact gm minus gmc means what, compensating the hard p value, yesterday I showed you know negative resistance this ok.

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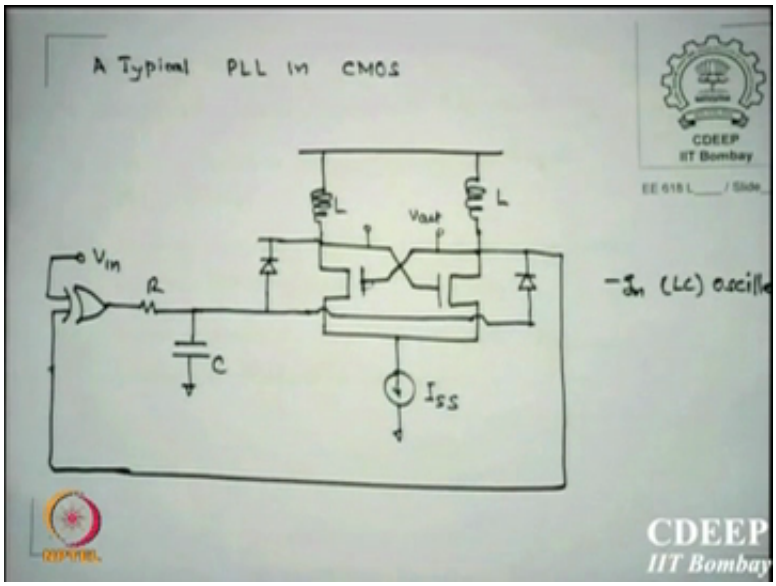

Here is the PLL base PLL for a CMOS technology, this is your VCO minus GMOS, VCO yesterday I had already discuss with you these are the diodes which essentially, this is the control voltage. This is that average or RC filter I just showed you the lpf this is that average or RC and this is your phase detector, your reference input the frequency at which you want to lock the input. This is your VCO you tune it to this close to this frequency, feed it back compare it and the output here is locked to the difference or if you must have observed there is no p channel device anywhere still is called CMOS because technology CMOS VCO [FL] control is coming from the phase detector averaged out.

So, this essentially why also PLLs are very crucial for real life requirements because you want to hold this frequency to a constant value before you use it in to any particularly RF applications. Where this called image is very strong there and we will actually it will pass through the digital side and that may actually huge noise your capacitor requirement for a to d converters will be very large. So, it is very difficult to maintain large capacitances in chip and therefore, always we will write to reduce down frequency from the higher ones and you do not want images to move through.

So, no dc signal should go out, so very important that it settles to a frequency exactly some other day, some other time. Before we quit this today last introductory part which is again as I say not the part of the course, but I think you should know before you quit.

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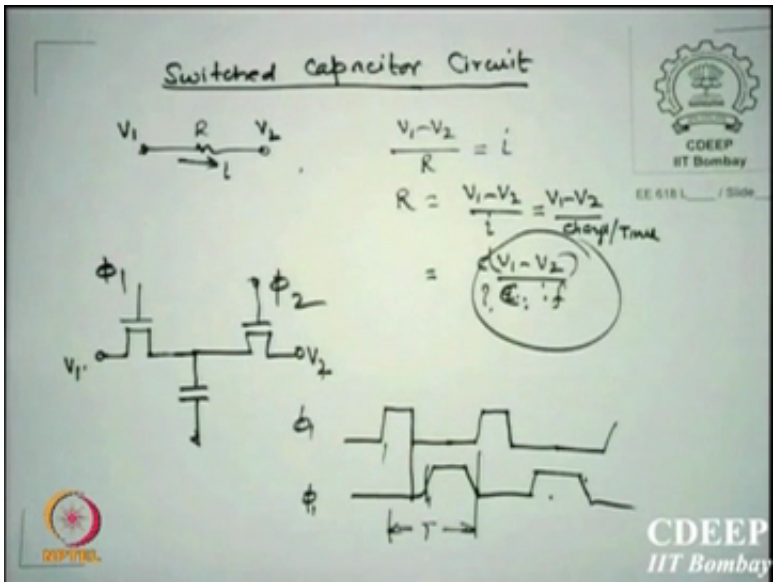

Switched capacitor circuits are very very popular in e to d converters or many of the filters, like you can even make ladder filter, LCR filter using switch capacitors. Why we want to change everything to capacitance because we know the resistance and inductance are always troublesome in taking areas and accuracies, capacitors are well within my control.

So, I prefer all circuits to work with capacitors. So, here is something very interesting let us take a case this is your resistance, we have a voltage V 1 we have a voltage V 2, one of them is higher let us say V 1. So, V 1 minus V 2 upon R is high ohms law or R is equal to V 1 minus V 2 by I or V 1 minus V 2, what is current charge per unit time charge per unit time, but what is one upon time frequency charge is essentially q times something and total charge will be decided by the capacitance available there some way into frequency something of this kind not exactly.

So, I have an idea that I can replace Rs a CV [FL] either CV cv. So, I can replace a resistance by a capacitance this is my thinking, this is what essentially it means show one what we do. Let us say there are 2 switches which are driven by phi 1 and phi 2, phi 1 and phi 2 are clocks which are what kind non overlapping. So, maybe I should draw a rectangular [FL] actually rise time 0 [FL] if you want further you can do like this ok.

So, essentially I am saying there is a depth time in which both signals are 0, both clocks are 0 of course, the period is say from this to this or from here to here, whichever way

you look at the period is same. So, here is a phi 1, phi 2 non overlapping clocks and let us say I have a input voltage given here V 1 and input output voltage expected they are also actually put by me is V 2. Do we see this I am trying to replace the registers by this network is that clear V 1, V 2, V 1, V 2 [FL] R [FL] I am replacing with 2 transistors switches and a capacitor.

If you have written down I will give the maths on that ok.

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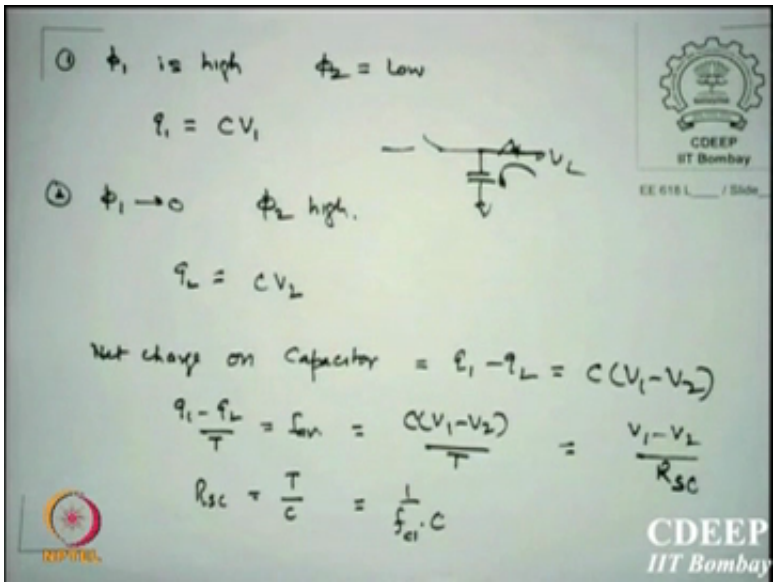

So, when the phi 1 is high and therefore, phi 2 is 0. So, what is the charged on the capacitor q 1 is CV 1 if phi 1 is high phi 2 is guaranteedly low because there are no non overlapping [FL] 0 [FL] 0es [FL]. So, q that is the capacitor is charged to potential V 1 and holds a charge of q 1 which is C 1, V 1 second time I close phi 1 and make phi 2 high.

So, during dead time it is retaining the charge of C 1, V 1 after some time my phi 2 starts, the problem why I get dead time because I do not want charge to be not reaching its maximum. I want that charge to be retained as the fixed value of dc which I put p 1 around the phi 2 was high the charge of the capacitors from this side you can see this is V 2 and this is your capacitance. So, this is like a switch closed, this is like a switch open. So, now, this tries to charge this capacitor depending on initial it will decide what the new charge should be, but it will assuming the charge which it should go if initially there was no charge should be C V 2.

However, if both are one by one, so the net charge on the capacitor assuming C 1, V 1 is higher its q 1 minus which essentially is C V 1 minus V 2 in one clock cycle of the phase q 1 minus q 2 is the average charge current which is flowing through this charge divided by time. So, this is the average current which is essentially equal to C V 1 minus V 2 divided by t, but we know from our earlier theory current is essentially V 1 minus V 2 by always have whatever r switch capacitor equivalent may we will say it the equivalent register have a [FL] V 1 minus V 2 by R that is the high current flowing through this.

See if I equate this the switch capacitor is t by c or equal to 1 upon s clock. So, if I know my 2 phase clock and I know its frequency I can create a resistance upon 1 upon fc equivalently, is that correct before we quit we make a simple filter [FL] [FL] is the last figure [FL].

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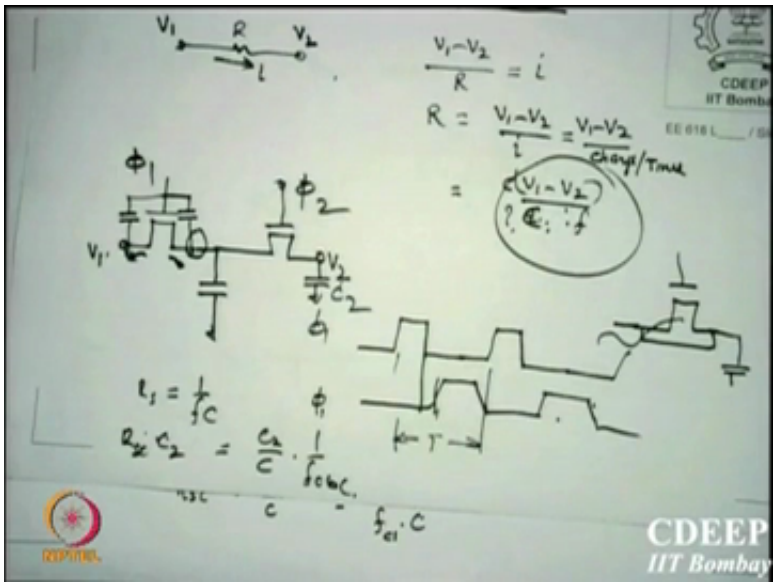

Say it will be C (Refer Time: 48:09) time constant is C 2 by C 1 or C 2 by C into clock, 1 upon clock R is 1 upon fc. So, if I want R RC into C 2 then it is C 2 by C into 1 upon f clock [FL] cutoff [FL]. You can see from here I can create any filter between these capacitors and an integrating capacitance also I can put switches there any resistor I want an amplifier I replace that resistance by a capacitor switch and then the ratio of capacitance will give you gains.

So, I can make an amplifier, I can make an integrator because I do not put R there I put only C I get an integrations. So, I have I can create every circuit of OP-Amp which

requires R can be replaced by a switch capacitor, one of the advantage because capacitance of the easiest to make in MOS technologies or even bipolar technologies compared to every other resistor or any other values you want to fix. It is partly digital because switches are there and that is where the problem started before we quit no reason to explain, but this switches I have not ideal or they create hell of an issue.

One problem is which everyone should know whether it is digital analog circuit, non circuit, if when it is on there is a charge in the channel when you make for 0 you expect this charge to collapse. So, where it can collapse either of the source end or at the drain end yeah charge has to be withdrawn, but there is a capacitor sitting here [FL]. So, the next value [FL] offset [FL] circuit [FL] charge [FL] transistor [FL] short. [FL] charge [FL] capacitor [FL] technique [FL] charge induction [FL] problem switches [FL] capacitance [FL] they share the charge feed forwards feedbacks both are possible.

Their output levels are decided or what frequency you are turning on and off and what is the feedback it receives. So, the final voltages are not exactly known depends on the frequency which you operate, this is another problem much probably this feed forward feed for backwards problems are very difficult to solve, but can be minimized. [FL] method [FL] CMOS [FL] problem [FL] device [FL] kt by c noise and that kt by c noise always exists. So, switches being non ideal the issues of non idealities play a role in any switch capacitor systems, but otherwise they look to be very promising, they look to be very promising.

So, this finishes is whatever I wanted to tell you in this course. Not that it is enough, not that it is less, but this is enough for this semester.