**CMOS Analog VLSI Design**
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**Lecture - 27**
**Oscillators**

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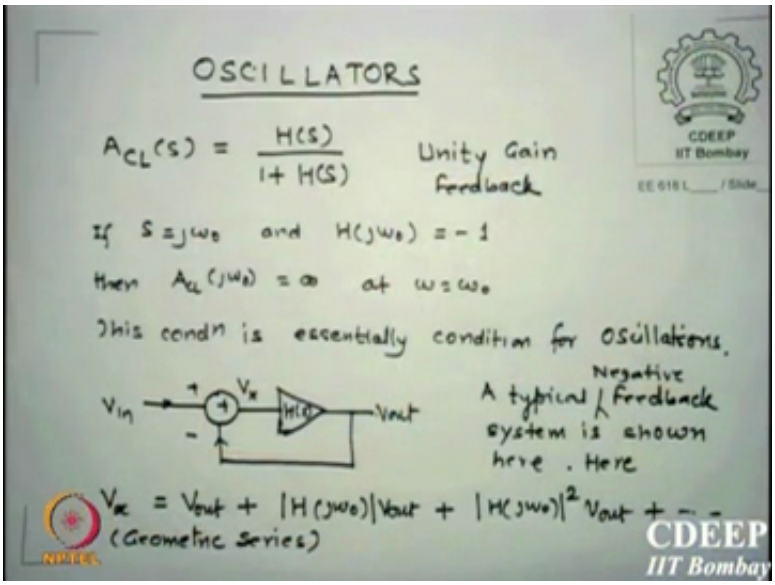


So, we start with the new topic today oscillators; all of you are aware that unless there is a some kind of a signal generation, which sinusoid be it triangular wave be it ramp or be it finally, the square wave, or rectangular wave. You need to generate signal in many applications in analogue are sinusoid oscillators are required. There are many applications in digital as well as mixed signals you need some kind of a square wave or rectangular wave generation, or pulse waves some other applications like synchronization you may require ramps, but all these are not very difficult as far as the periodicity is concerned. So, we are more interested in signal repeating at a given period. So, that is why it is called oscillator. It changes a repeat itself after a particular period or it has certain fixed frequency.

A typical feedback system is shown here, which has the transfer function of HS open loop gain, and if it is given a feedback and assuming the beta network is 1 unit as a gain of unity then a closed loop gain will be HS upon 1 plus HS and the way it seems here that the output is feedback to the input, because that is what beta is 1 essentially means. And it interacts with the input and forms a new output and this process goes on. Now there are of course, 3

possibilities which one of course, I have shown here, one is this may be positive this may be negative both may be positive, this may be positive, this may be negative and one maybe stronger positive positive or stronger minus minus which all possibility exists.

One of them shown here that actually input signal some way adds to the feedback signal, and therefore, if I look at the output of this summer it can be expanded in a geometric series; which says Vx is equal to V out at j omega if at omega 0, at the frequency at which I am interested in and to be out h j omega 0 square v out and go on and so on and so forth, and one can see from here from this series; that f h j omega 0 magnitude is larger than one positive quantity, then what will be the series look like, a diverging series because each term will be higher than the last one. So, it is a diverge in series and therefore, in some cases this is called growth conditions. So, it something keeps increasing and it will finally, help to the saturation value whichever it reaches well start oscillating it is only going in one direction and may be saturating.

The other possibility is H j omega 0 is less than 1 or minus. Then of course, as the term go ahead they will start reducing essentially means, and one can say that this will be a converging series, and if there is a convergence in series; then one may say that somewhere it may go down. At some frequency it may happen that the series some we can calculate and one knows the geometric series has the let us say there are p terms. So, 1 minus 1 upon 1 minus p is the sum of any geometric series. So, I can evaluate for it is such divergence series converging series the net sum value for this. This is what is my next slide is trying to show.

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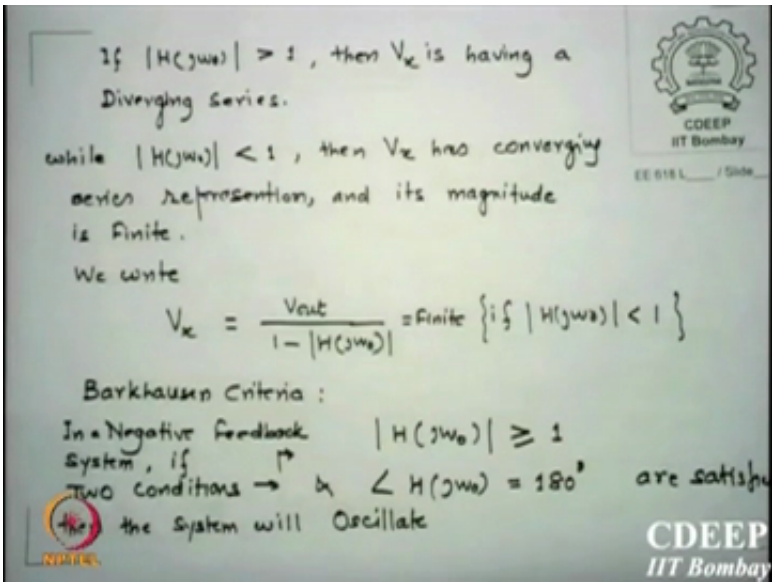


The first part already I have said if H j 1 it is a divergence series, where the if it is less v h convergence series representation and it is magnitude is finite, and can be given by 1 minus h j omega 0 omega 0.

Student: Only omega 0.

Omega 0 we are only interested in the frequency at one frequency. This is the frequency where system will oscillate; that is what we are trying to find out. So, what backhouse said about this condition that, if you have a negative feedback as shown there and if your this H j omega 0 is larger than one, and if the condition second that H j omega there is 180 degree then the system may achieve, let us say this is minus sign it should decrease. So, this is the condition at which we are already seen this is the condition for stability if it goes up other side system becomes, unstable.

So, we are right on trying to see where systems start becoming unstable. We must see that this instability can be used to generate the signal, because instability means something is feedback and it keeps returning back. Now this bar column backhouse criteria which you can you have done in second year I will not repeat again, based on this thinking I can make number of oscillators.

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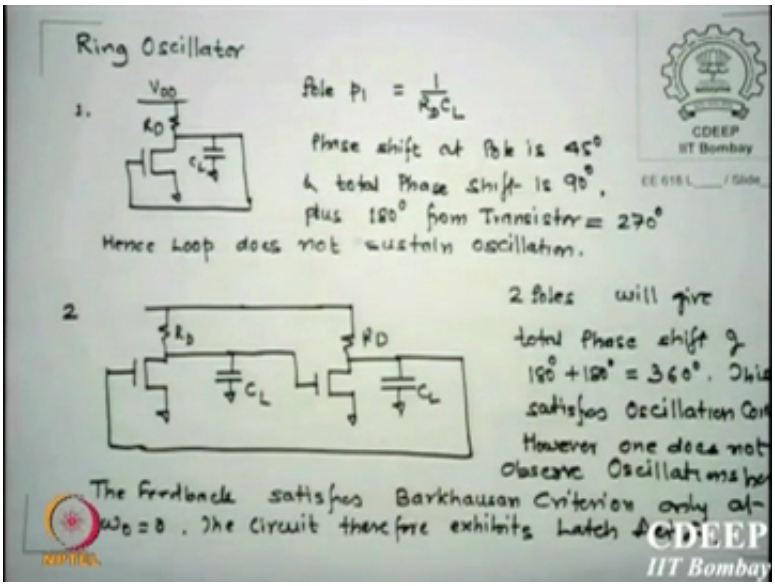


Yeah, that we can read in a second-year book this is just main important part you should look if you have a signal transistor and you have a single capacitor, which may be the cdb of the transistor itself and may be some output into wire connections. Then we see it has a single pole it has a single pole which is 1 upon Rd Cl.

We know a pole the phase shift goes 45 degree per decade. So, the maximum phase shift which a capacitor can give is 90 degree j, transistor will give you 180 degree out of phase signals input output, since I am feeding it back difference is essentially one 80 plus 90; that means, 2 70, but for sustained oscillation signal should return back to add or 0 degrees or 360 degrees, which is 360 is same as 0. So, when the signal returns to same phase, then only it will start actually operating as oscillators.

So, a single transistor with a capacitor does not give any oscillations, it is like a system which will die down at the end of the day, and no oscillations can be seen. He said if that is so, I had to such systems connected in series. This is essentially the principle of ring oscillator you have a one inverter is feeding to the next inverter you once CL here one CL here. So now, you can see 180 plus 180 is 360, this is 90 plus 90. So, total 180 out of 180 the return signal is 360 degrees is that correct? This is 90, 90 and this is 180, 180.

So, essentially now you are saying you are satisfying that backhouse criteria that the sigma has to be 180 degree and we are satisfying backhouse criteria; however, we see this does not oscillate; though it looks to that it is satisfying your condition of oscillations, but it is still not

oscillating. This is what is it call essentially this is a latch, 2 inverters connected back to back is essentially a latch. So, if you put 1 the output of next is 0 you get that 0. Why this does did not oscillate? Assuring, that CLs are same the loads are same if you have a cmos kind of inverter what will be the output resistance of them very large ros. So, the games will be gm times ro, or even here are deal with you tens of kilo ohms. So, it will be roughly large gains will be available from both these inverters.

And if there are larger gains, the output which you are looking at; will be already reaching towards V DD saturation values. So, essentially what happens that even if you are satisfying the condition, the output becomes one or 0 depending on the, you know if it is one here it comes here 0 and it latches itself to 0 one combination whichever it starts with. So, it does not oscillate. So, even if backhouse criteria is made, it is not always possible that system will be stable and the condition there is the gain is extremely high, if the gain are very small this may be able to and one of the oscillator will make is exactly this.

That we will reduce the gains; low then the system may be oscillate even with 2 inverter systems. So, this essentially is the feature which we want to utilize. So, in most ring oscillators, how many stages you find? Always odd number of stages 3 5 7 or whatever numbers, and we never put it even because that even we look always reach to it is saturation values and it will only latch up it is like a shift register, and it will never be able to oscillate. Now, this issue has been taken care let us say I put now instead of 2 inverters I put it 3 inverters.

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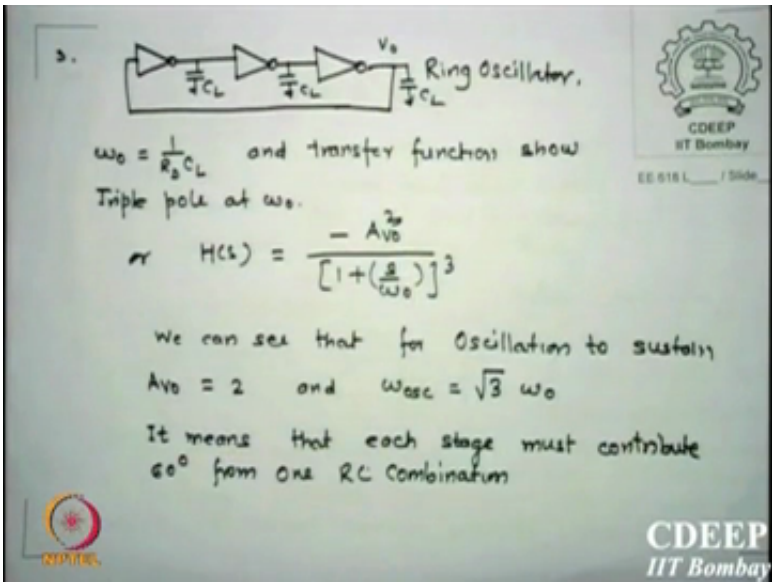


I have one inverter driving capacitor CL all of them have a same CL. If you look at the these are amplifiers with H j omega 0 as it is transfer function.

And this is A v 0 essentially is the dc gain, or low frequency gain, confusion really very low frequency gain or a dc gain. So, a transfer function for individual this will be AV cube upon 1 plus because a triple pole 3 of them. So, it is A v 0 and there is no feedback right now it is only open loop system. So, it is AV cube each has Av AV0. And each has same pole at omega 1 upon RC. So, we said there are triple pole at omega 0. 1 plus S by omega 0 to the power cube. This is called a triple pole system and we will like to see does this then provides an oscillations, somewhere close to omega 0 it is may not oscillate at omega 0, but where does it done oscillates. We can see and that is what we going to show later.

If we say we can see that oscillation to sustain we can figure out this is the proof will do, that the gain has to be at least 2 for per stage. And the then the oscillator frequency will be root 3 times the pole frequency. This is what we should get, and we will try to prove that you probably get this value as we suggested, but; however, it essential is trying to tell that 3 capacitor must give you phase shifts of at least 60 degree per capacitor so, that the net is 180 total is 360 plus 360 720. So, we all you must get the oscillations properly. Now how do I get each RC combination to give me a phase shifts of 60 degree. This is what the basic principle of designing a ring oscillator, but before we go to actually deriving these frequencies.

Let us look at this triple pole system, with a negative feedback. Is that everyone? It is trivial, but this is a proof I want to do it, but I will prove later that why I am right, or I am wrong let us see whether I am right hopefully I am right is that okay?

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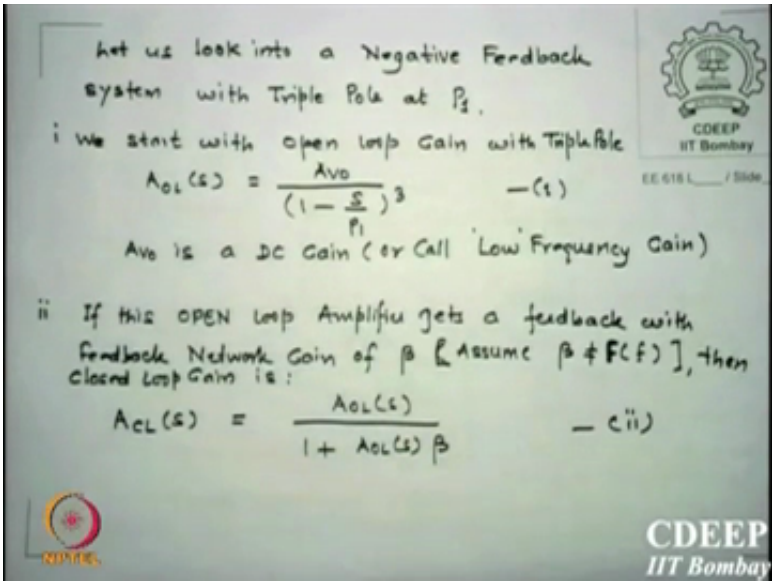


Let us say open loop system for a triple pole 1 is AV0 and right now I am gone making cube, I am just saying AV0 is the net gain for triple system which is AV0 upon 1 minus SP1,P 1 is the actual pole remember it is minus side it comes so, is magnitude wise you can like this. So, it writes1 minus S by P1 to the power cube I repeat again AV0 is the dc gain or if you wish, call it a very low frequency gain there is a confusion going on about the end of the course so, I am we started rewriting that again and again.

This is your open loop amplifier gain a transfer function and you get a feedback, with a feedback of network off which gives you a gain of beta,and right now my assumption is beta is independent of frequency. So, if I has closed loop gain I look at it AOL S upon 1 plus AOL S time bata. Beta could be 1 or beta could be whatever network actually you want to create. You may have a capacity network, resistive network to return back to the inputs.

If you write closed loop gain AOL S upon 1 plus AOL S beta. What I am now going to is substitute this AOL S in this, and then get the closed loop gain in terms of S by P ,1 and AV0 as we want to right now, you have say AV0 is not individual this total gain of the triple pole system. Later we say it may be cube, because each stage will give equivalent of that. So, is that okay everyone? If this open loop amplifier gets a feedback, with a network gain of beta

and beta is not a function of frequency then the closed loop gain is AOL S, what is the purpose of doing all this. I want to find a condition, in which the oscillator frequency is decided by omega 0, which is essentially in my hand. Is that clear? Because RC is my time constant, I can get RC by design and therefore, I should be able to relate my oscillator frequency with the design parameter, which is only thing which I have maybe I also had a gain, but I do not really have large gain because we have seen if it is too larger gain maybe, I should reduce the gain possibility is one only requirement although, I am not very keen about gain so much as I am worried about the conversion of omega 0 times something to be oscillator frequency, which allows me to actually design a oscillator of a given frequency of my choice if I is that okay?

So, if I substitute here. Of course, this is has been done in second year, third year wherever book you have studied I am just repeating it again. So, that you once for all you get this clear how a triple pole system or may be all pole system, actually gives you the oscillator frequencies. So, if I substitute here. I can get AV0 upon 1 minus s 5 P 1 to the power cube into a just this multiply here, this

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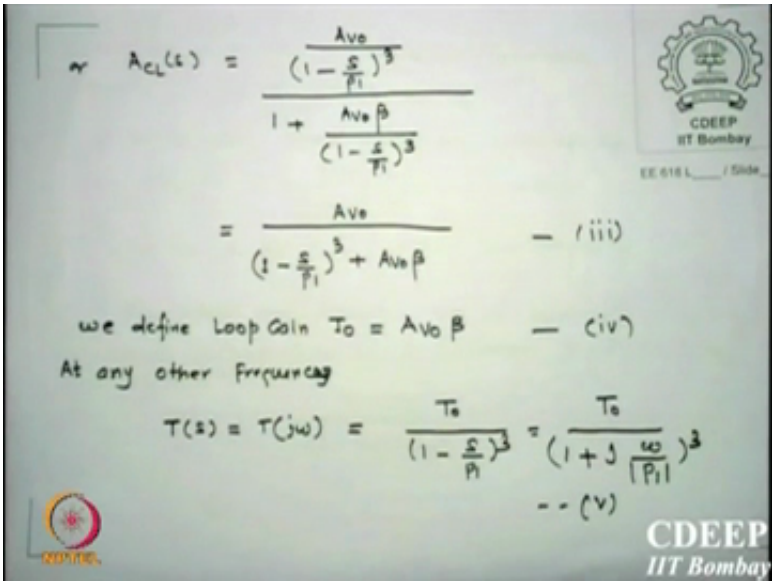


Multiply here and then you get this term. Now you can see from here, a loop gain can be defined as AV0 times beta t 0 remember, both terms are independent of frequency and therefore, is called t 0 is AV0 beta. Now any other frequency also we can find the loop transfer function which is essentially t 0

Upon 1 minus S upon P1 to the power cube this is essentially frequency dependence, this is essentially frequency independent term; or low frequency term. So, if I write this, and I write that s is equal to j omega, and then put P 1 as it is magnitude value then it becomes t 0 upon 1 plus j upon omega upon root p magnitude P 1 to the power cube this equation you keep will use it later, but since I was writing t 0 I said we can also write t j omega, at any frequency in this fashion I will use this later on, to prove that what also gives the same result as the solution of this equation, what are these called? Which technique I am trying to show you? Solution of this equation of the denominator is; will give you roots and the technique to figure out whether system is going to grow or not, is decided by root locus technique.

So, I am trying to now bring back something which, third year students must be doing control course or must have finished no, no next semester 4th year of course, you have done and m tech of course, should say we have done, they cannot say they have not done except with there are few M.Sc. students then they may say well I have not done it. So, we observe.

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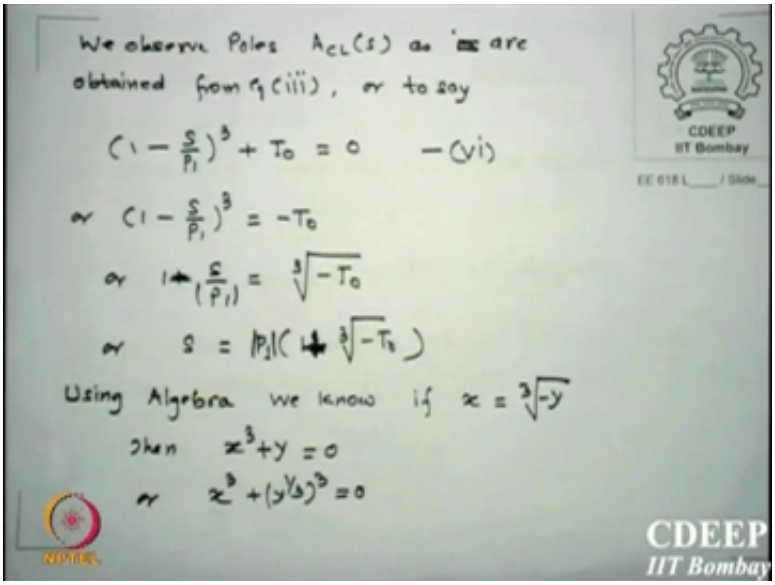


The poles for close loop gain, as the denominator solution equal to 0. So, 1 minus S by P 1 you everywhere either plus 1 upon j times or put P 1 like this. Then I get a solution from this, 1 minus S bar P 1 to the power cube is minus t 0 or 1 minus S by have.

Cube root of minus t 0 equation, how do people solve. This is a trivial maths, but I always realize that sometimes triviality has forgotten by many so, I solve for you this is essentially

say let us say, x is equal to cube root of minus y then I can write x cube plus y is equal to 0 or x cube plus y to the power 1 by 3 to the power 3. So, this is like a cube plus b cube equal to 0.

Student: (Refer Time: 19:05)

which one.

Student: is equal to P1 into one (Refer Time: 19:10).

Yes; you are right, but that this relevant to right now, this minus will be taken care when the solution will come plus minus.

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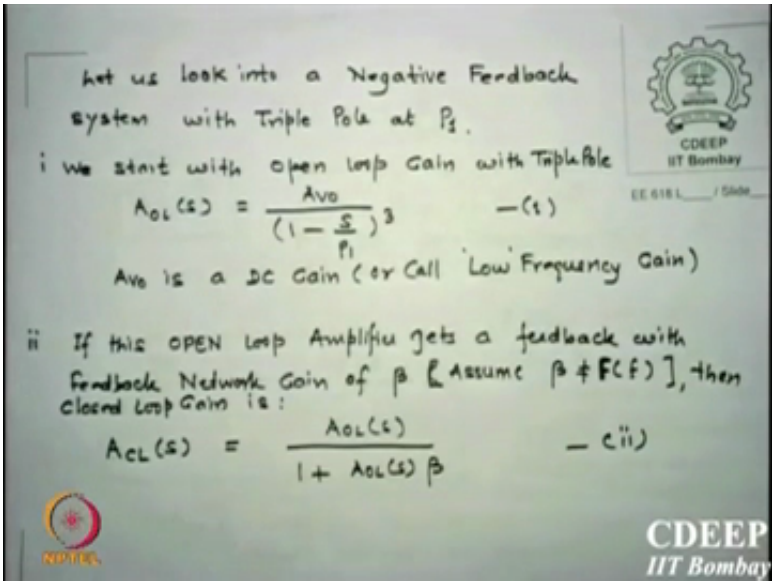


Or may be mod on put a sign plus whichever we. So, if I solve this.

Student: sir.

Yes, sorry he is saying plus. So, maybe I will do this. No, I think that was correct know? This 1 plus was correct why did he say so? If I bring it 1 plus t 0 was correct in fact. Right now, whatever mod will see later, 1 minus this then this is 1 minus sorry if this is 1 minus. So, 1 minus root 2 0 is correct. So, 1 plus, your right 1 plus now is correct sorry. So, if I now have an equation which is x cube plus y cube y to the power 1 by 3 cube.

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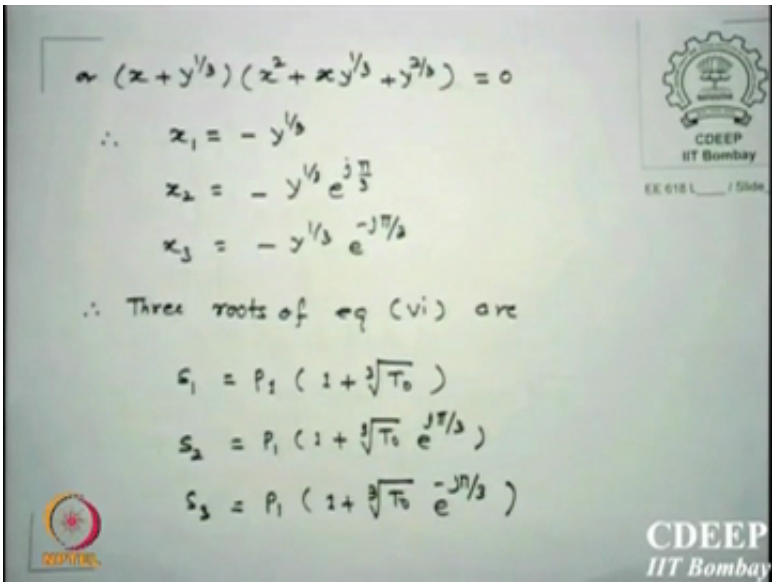


I can expand this x plus y by a plus b into a square plus a d plus b square this is so, known to every one of us. So, there are possible solutions out of this one is x 1 is minus 1 by y to the power 1 by 3 x 2 is minus y to the power 1 by 3 e j pi by 3, and x 3 is minus 1 by 3 a j pi by 3, pi by 3 is root 3 by 2 or 60-degree v. So, e to power j 60 degree. So, if I now substitute the pulse.

S 1,S 2, S 3 I will get p 1 plus 1 plus root 2 0, P 1 into e to the power of this, and the other to the power minus j power by. So, they are called roots of the poles which we you have actually wanted to find for the acl; please remember this is closed loop feedback, regard a feedback system they are still working on negative feedback system, and we want to see does that give you oscillation edge, where it will start oscillating. After all, what is negative feedback I is used for stabilizing something. So, if I can get to the edge of instability I may have growth conditions starts and you may say we how oscillation conditions met. So, if I if we assured this.

Maybe I can written down these expressions. So, if I.

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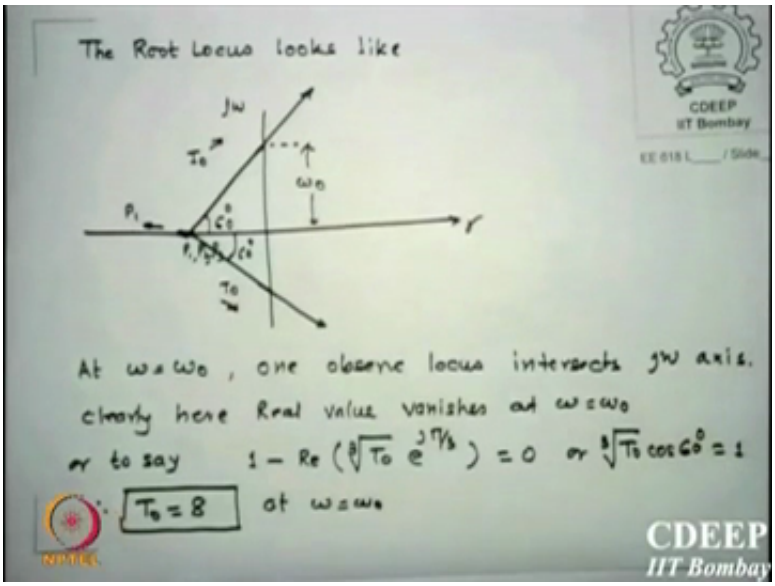


Plot the root locus that is our plot sigma H j omega for these 3 roots, please remember all 3 poles are at t is equal to that we already initial at the same point for the open loop system. Now if I change the t values a beta values. For initial value 0 t 0 you have a pole at one which is minus of whatever that P 1 value which we got; however, if I get it e to the power j pi by 60 or pi by 2 3 I see this is the curve for that, similarly for the minus 60 degree.

This is the curve for that. At this point, at that is that where the j which this axis cuts a j omega axis with now see e to the power, this this divided by this is the tan inverse of tan theta 60 degree. This is essentially a frequency omega 0 at which, what is the omega 0 definition was? We observe that omega 0 is the frequency at which this locus interests j omega axis. So, this frequency is omega 0. Clearly, here the real values must vanish whatever j omega axis, real values must vanish that is why it is called imaginary axis. So, if I find the real value to be 0 from the expression which I have, one mark for this point 1 minus real value of root 3 t 0 e to the power j pi by 3 must be 0.

Solving this, I get t 0 equal to 8 at omega equal to omega 0 at omega equal to omega 0 the a beta requirement is 8 value; is the and a beta one and there are 3 stages gain how much should be individual stage again should be 2. Is that point clear? So, if you can now create an inverter or amplifying system which has a gain of 2. Then at the same position if you have triple pole equivalence this will give a some kind of a frequency at which system is now at the age of instability, and still at the j omega axis. This point we want to clear, from the root

locus figure, this divided by this is how much? This is P 1 this is omega 0. So, tan 60 is omega 0 by P 1.

Mod of that is that have you drawn? So, if I substitute tan 60 is equal to omega by P 1 then I get omega 0 is root 3 P 1 1.73 times P 1, is that clear to you? Now at this point what is the frequency above omega 0 if you exceed little bit omega 0 sigma is slightly positive. As you cross t 0 slightly more than that, you are a slight sigma higher than 0 and imaginary part will only exist. This is like a positive feedback system, which will show you growth response. So, at this point ahead there is a growth. So, we should have gain not exactly 2, but slightly more than 2 which naturally parasitics will allow you to get it.

So, you had that one you say system is start, into equivalence of positive feedback is that clear? So, a negative feedback system has been converted to; a positive feedback edge system you can say, by just adjusting the values of t 0s. Is that clear? And the frequent we can see typically if you look the solve that, this it is e to the power sigma t sine omega t is the growth equation for.

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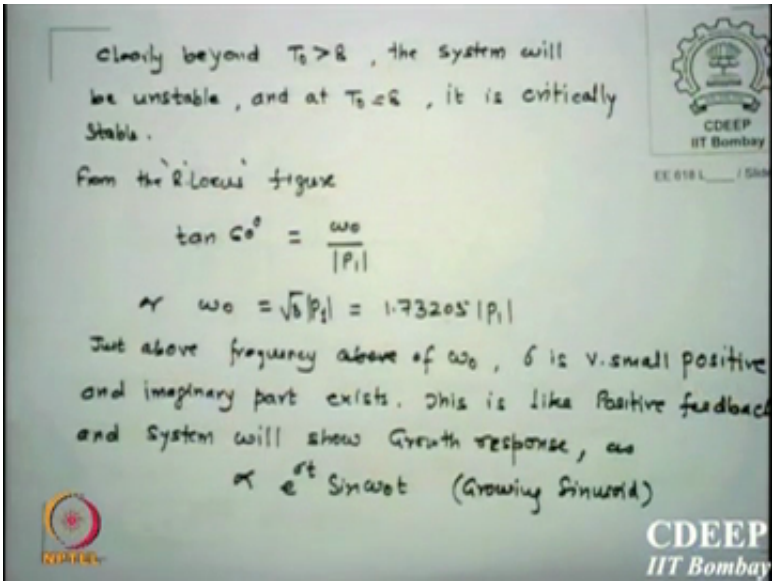


The wave form to go this is how it actually grows. Now we see from here if this is. So, then we can use. So, we are figured out that the oscillating frequency starts at when a 0 is roughly equal to slightly more, but equal to 2 or the other 8 right now t 0 is a beta.

Which is 8 if you keep it then you will be able to have start of growth system. Now we can also figure out the same frequency which we are talking about using a bodes plot. Bodes plot can be plotted for the loop gain itself. So, I will as you finish this writing then I will show you, I can do the same analysis using bodes plot also. So, what is the frequency it will start oscillating? Root 3 times the 1 upon RC whatever you are fixing for yourself R and C are within your hand and therefore, you are fixing the oscillating frequency. And what is to be guaranteed, that t 0 should be just about the 8. Is that okay?

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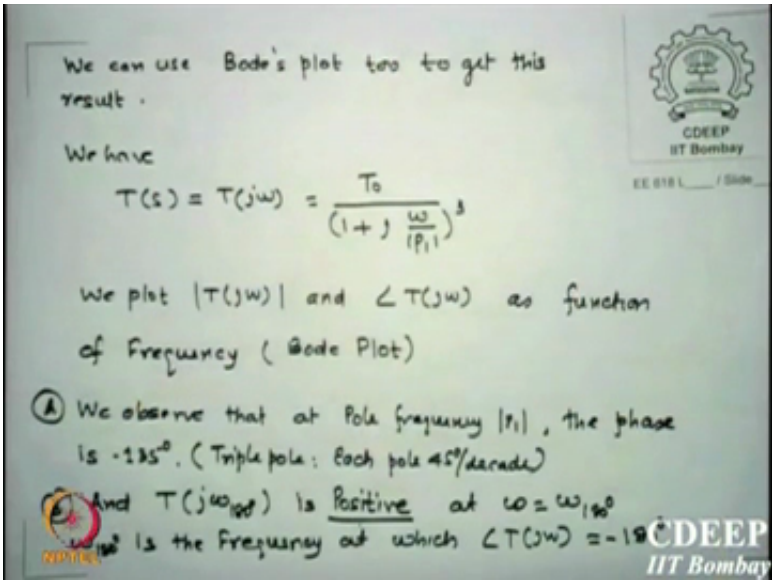


So, we can use of course, this I as I said this is not the part of this really course it should have anyway, everyone should know this. So, we can use the bodes plot for the loop gain ts is tj omega which I have already written a function and then we plot the magnitude of tj omega 0. And we also plot the angle that is the phase phase for that which we called the bodes plots. Please remember each pole gives how many how much degrees per decade what you find degrees. So, there are poles. So, it should reach 135 degree at the pole position, is that in a bodes plot at P 1 frequency at P 1 you must get a phase shift of minus 135 degree we also know if tj 180 is positive there is a magnitude at 180 degrees positive.

Is that clear to you? And phase as use one 80 they are growth system is that clear what is the stability or criteria was that if one 80 should not reach before the gain goes to 0 degree. Here, gain is positive and you are reached one 80 degree now let us see how it looks. So, what is

the gain for? How many degrees per decade? Minus 20 plus minus 20 plus minus 20 minus 60 db per decade gain starts falling.

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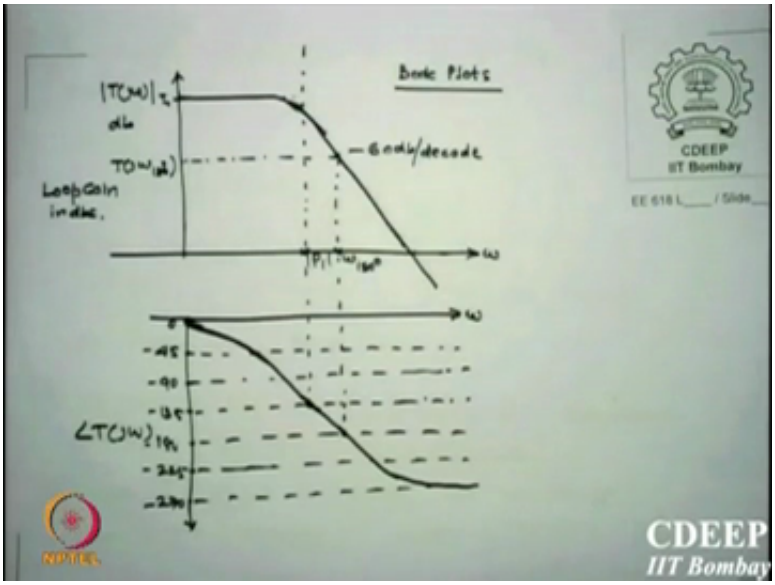


So, if I do this I have find the magnitude, which is the loop gain in dbs is minus 60 db per decade this is my pole 3 db down point and at this point the phase should be 135 if I extend it whether there is no other pole it will go straight.

And then matches saturated by another 135 degree to 0, or minus 270, 135 here 135 here and somewhere here we have phase of 180 w one this minus 180 extend it on the gain axis. So, what is the gain margin, now positive you have this much gain available at w equal to w 180-degree phase this at one 80-degree phase minus 180 we have positive gain there is that clear. So, what does this mean? What does this expression means? It means that the stability is disturb and if you can make that t 0 equal to 8 as I started with this point will get exactly equal to root 3 times a pole frequency.

This is what essentially bode also said so, and also the root locus method the third method will be want request criteria take how many times minus 1 0 actually in circle, and get the same point again if you wish we can do that is well, but is that. So, you have just look at it either use bodes technique or use root locus technique or use request criteria and at the end of the day we figure it out that the oscillator frequency is root 3 times the pole frequency, let us say if omega 0 is the pole frequency then omega 0 tan inverse pi by 3 is root 3 by root 3 omega 0.

So, essentially what is they trying to say, at that point the loop gain becomes 1, when here is let me redraw it. So, we now return to ring oscillator, we now return to, is that okay everyone? Has drawn this. Pole 135 180 gain positive. So, this is the condition of oscillations.

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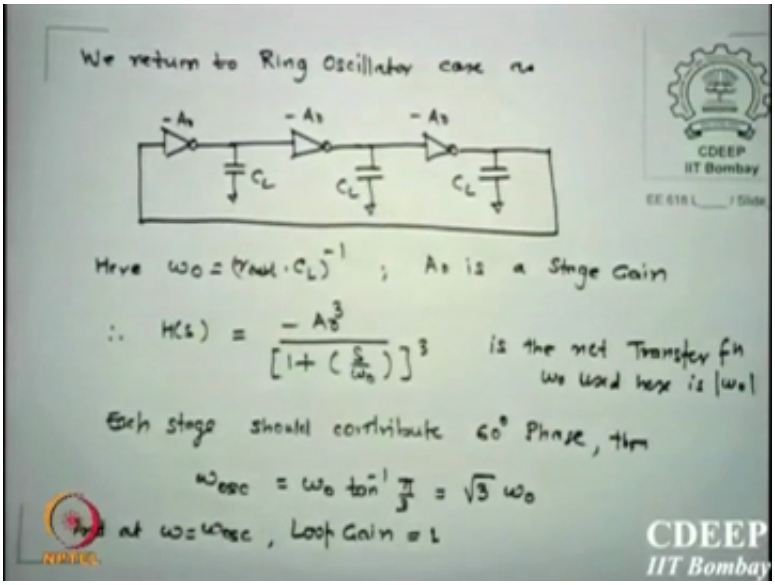


So, we return to our case of ring oscillators. Omega 0 here, is r out time CL to the power minus 1 please remember r out is normally their output this if it is a rd kind it is much easier to control omega 0 and a 0 a stage gain. So, Hs is minus a 0 upon 1 plus S omega 0 to the power 3. The net transfer function omega that used here is omega 0 each stage should contribute to 60-degree phase. Is that clear? That is what we said know 60 60 60 must appear. So, that total is 720 or 360 or 0 whichever you have call 180 180 180 plus 180. So, you will return back to original faiths 0, or 360 degrees. So, if you do this I writ e omega osc should be tan inverse pi by 3,60 degree means pi by 3. So, tan inverse pi by 3 is into omega 0 should be the, or root 3 times omega 0 should be the oscillator frequency. And at that time loop gain is unity, loop gain is unity. So, I can, how can I design oscillator? All that I have to design an oscillator is to decide my R and C.

That is for r is decided by in transistors by what? W by ls. So, CL is also decided by cs because cdb and other capacitances are also area dependent turns, is that clear to you? So, adjust your CL and R such that you get oscillator frequency of your choice that is how oscillators are designed. So, what is the typical a 0 therefore, you should have now for each stage, for a loop gain equal to one at this omega 0 what does that mean?

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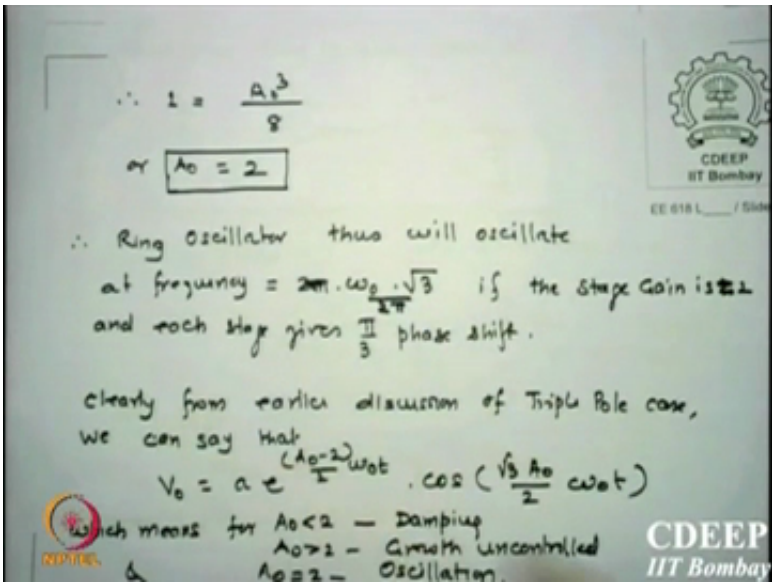


A 0 by 8 is cube by 8 is one. So, a 0 should be 2 ring oscillator that is will oscillate at frequency 2 pi omega 0 into sorry, 2 pi not omega 0 by 2 pi. So, omega 0 root 3 by 2 pi if the stage gain is equal to 2.

Each stage gives you a gain of 2, and then at this frequency ring oscillator will start oscillating. Clearly from earlier discussion that triple pole case says that v 0 is a some constant, e to the power a 0 minus 2 by omega this is the growth equations into cause of this is the expression for the grow growth form which you generate. See more on the solutions so; obviously, if a 0 is less than 2 to start dumping. A 0 is gone to un control growth may start, and equal to 2 sustained oscillations will be observed. So, a number of number of inverter stages should be always, or why because otherwise the net face can never become 0. So, if you have 5 this will be a to the power 5 by something and it will still come to 32 it may come and a 0 may still be 2. And you keep on doing this for any number of stages typically in a large ring oscillators which we test, how much you typical in cmos it delay per stage, you have any idea? What is tau per.

Student: (Refer Time: 35:58).

Picoseconds. So now, if you want a frequency figure out how many stages you should have. So, that n 2 n plus 1 times so much will be the frequency of your ring oscillators. And to get that w by ls for each stage is adjusted by you is that clear? So, the design is essentially only on, the w by l and associated please remember cdb, which is the output capacitance of the

transistor is essentially is governed by area. See input the next stage is also governed by area, and therefore, whatever w by l you chose this situate it satisfy both your current conditions as well as your capacitor conditions, is that clear? So, that the gain is 2 as well as you get the frequencies of whatever your choices is.

This is the most standard square wave generator which we use in the case of digital hardware, everywhere you find the easiest method of generating pulses are the ring oscillators. Just put large number of stages for lower frequencies if you anyone who is doing an m tech project or something you must have seen.

To test your process, we have one of the test area which we have create is the ring oscillator. What is it tells? I have 125 stage oscillators so that the time which it will require will be large enough frequency low. So, I can exactly monitor my frequency, and by stage law I know how much per stage the delay is essentially coming, and that will decide my speed at the digital hardware which I am going to use, is that clear? So, if one of the test block on any chip test area is always a ring oscillatorand typically it has 125 or even higher number of stages simply because of what, because the delay has to be measurable on a cro otherwise the inaccuracy in your measurement may actually cause the problem and since, you know the net delay, you know how much is for stage delay you have.

So, that is how ring oscillators are used as the test block for all digital signal processings then which please remember all chips you have one test chip itself. What is it? There many transistor areas or many components on a chip, each representative of that is brought on this separate area of a chip each like you have a d flip flop. So, you have few d flip flop you have error you have small error there, every block which I use in real life is actually brought for tests individual testing so, large parts are used to test individual blocks large parts are normally not available. So, what do we do? You put a multiplexer there to use same parts one after the other.

So, this is how the test patterns test a parts are created once every chip must have at least how many test areas can you think? Wafer test area. Top, bottom, left, right centre all variations are taken care. If it satisfies everywhere you are well within your design to work at every possibility, is that clear? So, please remember chip when you make many of the students have been told, but they do not want to think that way whatever component you require first must

be brought on the test chip so, test chip must be designed and put in the centre 2 corners and to bottom and a lower corner. So, that the test is performed.

Before the chip is. So, because chip will have no pad internal to test anything let us say there are number of registered number you cannot probe there. So, how do you know which part did not work. So, in real life whether it is analog chip or a digital chip the test chip area must be left for you. Sometimes you know more tests are done, but at least these many tests are even for example, process test is done, whether the metal is going through down. So, I have small trenching which I did here put a metal and actually to part I test whether your continuity was or not. So, all test things are always provided on a test area please remember this is something no one tells, but I figure out my own students do not do it in spite of being told.

I mean I cannot blame anyone, but that test is essentially if you are really getting your chip fabricated and want to test. You apply input and nothing verse then what do you? This hope for the best every time god may help once a while, but not every time, test is something and it is required lot of thinking what testing we should do. So, what is the best technique is go to the earlier chips find what test area they are used, implement all of them with your (Refer Time: 41:07). This is the game all of us have been playing and no new things come. Our aim was not to do this theory as we did. So, long that why you should oscillate our interest was only in VCO, which is what we have want to use. VCOs you all know stand for voltage controlled oscillators.

That means by changing the voltage as a control voltages, I should be able to change the frequency, but why did I do all this to once for all make it clear that from where everyone is bringing the theory to utilize and design of an VCO, the part which I did here is no direct bearing on my VCO designs, but as a concept you all should know that how I actually get oscillations in real life, and why I just gains to these values is that clear? So, why do inverters things will never work as oscillator, because they immediately their gains are. So, high. So, the is that clear? Gmr 0 is. So, high that a 0 2 is already crossed long time. So, this fact that there is no oscillations can be understood.

If you know what is the theory behind it.

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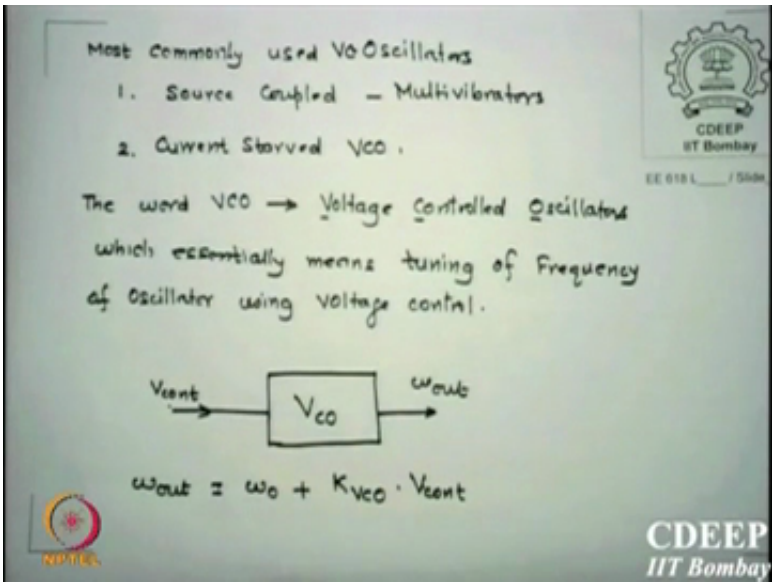


So, this is something I repeated what second year, third year student should do anyway or no. There are 2 kinds of oscillator which I did not say here one is called which only generates (Refer Time: 42:35) sinusoids, the others which generate other than sinusoids. The names are relaxation oscillators or phase shift oscillators the other way, but anyway right now I have not separated all of them I just want to use a normal sense VCOs. The 2 VCOs which generate the square waves, which are shown here one is called source coupled VCO, which is also popularly known as free running multivibrator.

The second is also a similar like a ring oscillator, but it is called current starved now this word is very interesting current starved, it does not I can draw more current I want more current, but my current source or sinks I have not providing is that, I am limited by someone else my vgs s wants this much current to flow, but the lower current source is interesting says it is name. So, these are called start, start inverters. If you look at the VCO, all that I am asking is we should have v controlled which will give me output frequency of my choice. So, if you look at simple expression the omega of 0 is the frequency when I said there is no control signal or 0 control signal. It is called omega 0. Then I say omega out should be this is equal to omega 0 plus k th some constant times.

V w out v controlled so; obviously, the unit of this should be what something radiant per second, per volt kind of thing because it should convert into radian per seconds. Is that okay, this is the schematic of a VCO this is what I want to design is it okay?

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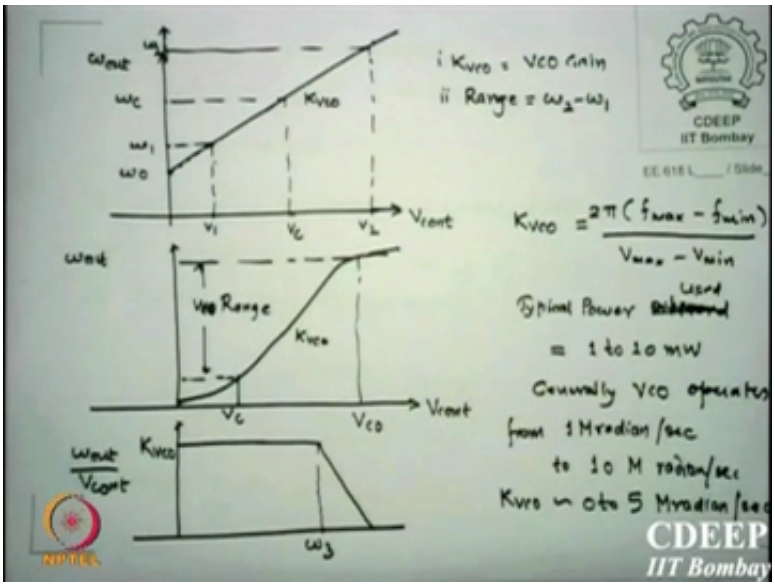


Now, what are the features of a VCO if I plot the same curve which I just now same expression w out versus v controlled. I have linear relationship that means, k is treated constant. I may vary the k, but k is slope which is constant; that means, I can do this, but forgiven this k VCO is there giving a slope for this curve, y is equal to mx plus c. This is the frequency omega 0.

At which typically we control is close to 0, intercept as we called. So, we operate our VCO, say this centre point some base call it vce centre frequency of centre omega c, is come kind of a centre frequency and v one and v 2 are on it is left and right. So, what is the range in which this was VCO will give me outputs for v 1 there is a frequency of omega 1 and for v 2 there is a frequency of omega 2. So, I have a range of omega 1 to omega 2 as my tuning range what is it called? Tuning range. So, a VCO I should be able to tune at least in a band of say w one to w 2 or to, say the range is w 2 minus w 1. And on and average this is half of that is roughly the centre frequency it is need not be exactly half, because there is an intercept going on, but magnitude wise it should be roughly half.

So, from this expression I can write, K VC0 is 2 pi f max minus f min, call it f max, call it f min divided by v max minus v min, is these called VCO gain KVCO is called VCO gain. Typical, power dissipated or used here, and most VCOs is of the order of one to 10 milliwatts typical; that does not mean I cannot make low poweror I can never make high power, but larger power will require larger currents, and therefore, larger w by l so, you will have a

lower frequency down. So, they are given bands will have limited or some maximum minimum powers available. Generally,VCO operation is one mega radian per second w max, sorry w minimum and maximum may be 10 mega radian per second, omega these are radian per second is omega because it is a naught f multiplied by 2 pi and you get rather divided by 2 pi and you will get frequencies. So, for this subst typical values K VCO varies between 0 to 5 mega radian per second per volt. Let us look at the real characteristics of v control and w out which is extended beyond. This vc and, this vc they are not same this is central and this is not central. So, we say prior to this and ahead of the VCO frequency which you have, the relationship between v control and w out is not linear. Only at this region to this region K VCO is constant ahead of it goes down and goes saturates.

So, we say as long as K VCO in linear this that is the range of a VCO maximum range. Is that clear? If this goes in the non-linear area, or this goes beyond this region then the VCO will not operate the fashion in which I thought it should. So, in real life, the characteristics of this to this relation is not linear everywhere for all frequencies. So, the minimum frequency from whichlinearity start and up to the maximum frequency up till which the linearity is maintained is the actual VCO range. Is that clear? This is also VCO range fair enough, for this actual max to min what you will do, but this is the ultimate limits. Beyond this or, beyond this VCO will not operate in standard w 0 into k times omega kind k times v control.

So, we must for a given technology, first to these markers are figured out how much is the range in which my VCO can operate, is that clear to you? So, this is something physical range you know to which you can really operate. If I plot w out by v control and this may have a frequency dependence. So, this is what it says K VCO is constant and then it start decreasing beyond those frequencies. So, we say this is the range up to which VCO should be used in your application. Corresponding to this frequency whatever voltages are possible only those voltages should be allowed to swing on, is that clear?

So, otherwise you know you may swings from 0 to 15 volt what do we do you may do it, but system may not responded because you may reach somewhere here, or poles may start actually get reducing the kv 0 terms, is that one clear? To you these are something limits which many a times a should be known for a given technology, and once these known then you can actually go to this curve, and you know what is the value of this. This possibly is normally measured values; these are not derived values these are normally measured value for an VCO and this data is many times provide in your analogue models.

Please remember VCO design is very, very crucial in some other circuits in rf, where do you think we need in rf circuits? I have shown you first few days my many slides. Any receiver when the signal arrives from antenna and you actually boost it through a low noise amplifier that frequency may be very, very high and your processing has to be a digital low frequencies. So, what do we do we mix it with some other frequency which is close to this frequency, and we create big frequencies, or you scale down that frequency by VCO tuning. So, this VCO has to be our variable frequency. So, that I can tune out this is called the mixer has one and as VCO there is the signal. And that together will give me the output which is omega 1 minus omega 2 which is small frequency.

Of course, there is a image which needs to be rejected. So, please remember VCO is a essential part in any mobile system, or in any such system in which signals is received from outside. So, this is why I thought that, you should know, you need VCO irrespective, the problem which probably I do not know whether you I will be able to cover by Friday if VCO changes it is frequency because of the drifts.

Student: (Refer Time: 52:39)

Or I want this range to be different. And I should be able to synthesize another frequency out of same VCO. I want one frequency f range is over, but I want another range. Like in bands in the case of many this you will have bands. So, you want to tune different bands what do you do? The another circuit which is used is called phase locked loops, which is also called frequency synthesizers normally you will be lower than the VCO you. So, you first design highest frequency VCO keep dividing as much as you wish this is required. So, VCO is the kind of VCOs I am talking is more useful for digital applications, but. So, is true for any analogue applications if needed.

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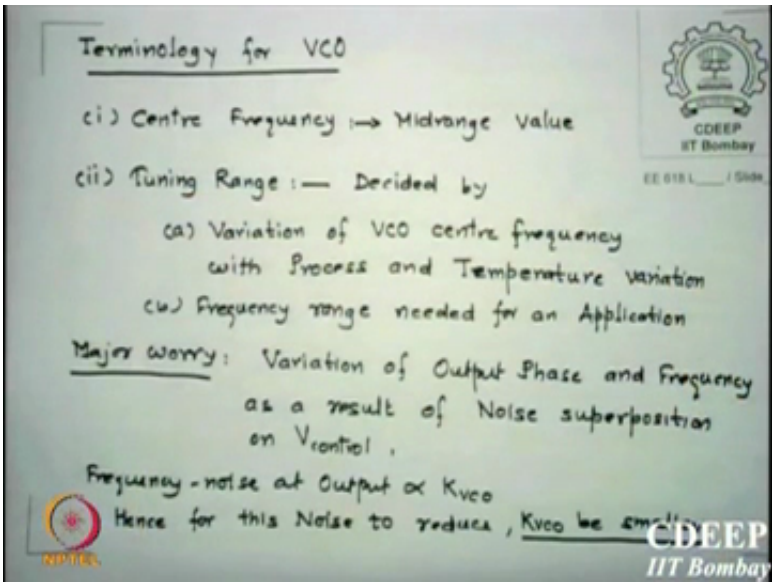


Before we start working ahead let us have some terminology given in a rezavis book nothing much from my side. A mid-range value of the VCO is called centre frequency. I already said, I just a minute, in the range somewhere in the mid band is we call it centre frequency mid-range value.

Then the second terminal second term which is of relevance for the VCO is decided by as called tuning range and is decided by variation of VCO centre frequency with process and temperature. Now this is another issue which I was just talking you need stability lock you should need. So, you need to have variation of VCO centre frequency with process and temperature variation it is limited by that and the frequency range needed for an applications, how much which man you are working at, and how much process variation and temperature will decide the range up to which circuit can give you proper performance.

Now there is an issue which, I do not know whether it rezavi has written, but I think I remembered it maybe he has written he is we said that after the phase and frequency of any circuit, will also be decided by the noise sitting on the control, because if v control itself changes other things will proportionately change anyway isn't it? And that maybe I said essentially how much noise it picks up. So, we must be able to figure out frequency noise at the output and which is proportional to K VCO this noise output noise is proportion to the VCO gain larger the noise give VCO.

Larger is the noise output you get. So, what should I do, to reduce this noise at the output? I should reduce the VCO gain K VCO because proportion to that. So, I reduce that value itself, but the tuning range are proportional to what K VCO. So, if you want the larger tuning range I want larger K VCO I want to low noise outputs, and I should have lower K VCO this is the design is that clear the 2 cases one you need higher VCO this K VCO for larger tuning range and you need lower K VCO for low noise outputs, is that okay?

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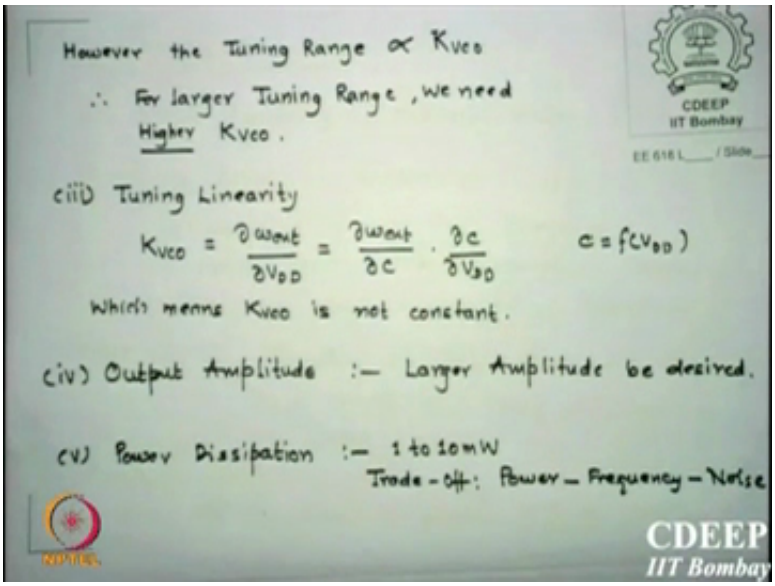


So, therefore there is a design issue; which how much noise you can tolerate and how much gain see frequencies limit you have the third parameter of interest is the tuning linearity, now we will see this latter.

Since the capacitance tuning is normally done by change in capacitance. So, we can say K VC0 output by dv V DD how much is my power supply variation output changes, which can be written as d upper word dc where capacitance is a function of power supply voltage. What does this means? That if I change the V DD my K VCO is not the constant quantity. So, I am also worried how much it varies actually. The 4th term of my interest is I need larger output amplitudes, because you want a largeroscillating signals, but; that means, limit the gain part from that because if that increases you may get instabilities.

So, how much maximum amplitude I can reach, before stability criteria is violated stringently I mean excessively. Typical, power as I have said for VCO is around 10 milliwatt one to 10 milliwatts and you have to trade-off between power, frequency and noise. So, whatever we

started the saying this is still valid for even in VCO we need to have trade-off between noise power and frequency. So, you cannot have a large tuning range low power and low noise there is nothing kind like it is like a triangle system you stitch one the other will reduce anyway the last part for the VCO property this is I repeat. First was we talked about what centre frequency tuning range.

Tuning linearity output amplitude power and last, but not the least.

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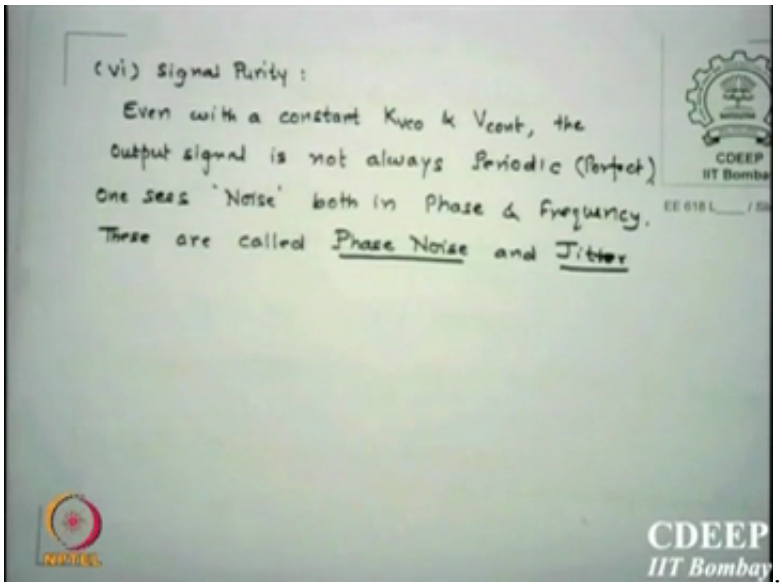


The last property of VCO which is a relevance a signal purity. Even with a constant K VCO and v control that is no noise on v controlled VCO is K VCO is constant output signal is not always periodic. There is still noise sitting over output frequency output signals, both in phase and in frequency these are called phase noise and jitter. The pll essentially controls this phase lock loops, essentially controls phase noise and jitter. Please remember phase and frequency frequencies time. So, frequency domain and time domain, they will they seem to be different, but they are always connected.

So, one can figure out not very straightforward way if you are given a jitter what will be equivalent phase noise or given a phase noise what will be equivalent jitter. Jitter is always in timeframes phase noises like between the frequency domain. So, is that to you? So, these are the property so, please remember. So, we need an pll at the end because otherwise this will take care of this. Your noise part which you thought is not there, even if you maintain K VCO and you maintain the control voltage even then. So, this is very essential in any VCO design.

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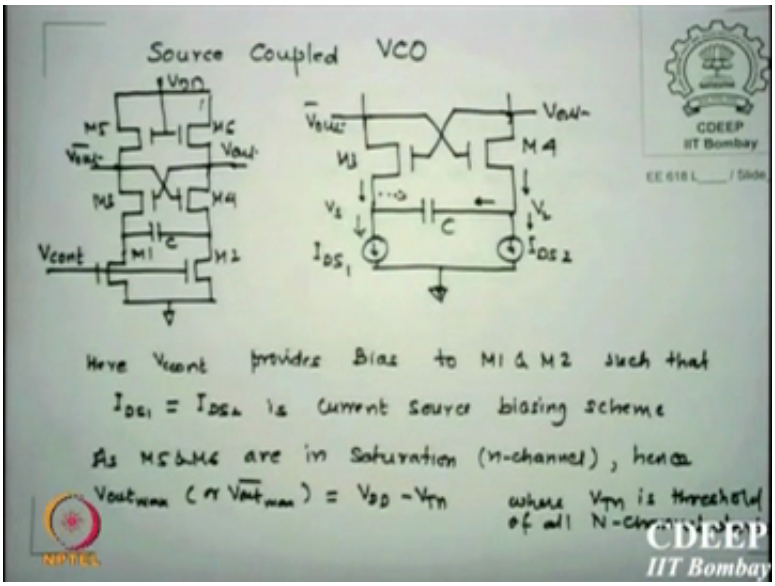


Which is the most common VCO, also popularly known as multivibrator; because we have got mostly on the bipolar circuits you will not immediately guess this is same circuit, but it is essentially a multivibrator. And implemented in cmos technology or nmos technology. If it is a this is all nmos, if I wanted to make a cmos transistor m 5 and m 6 p channel gate ground.

Student: (Refer time: 60:47).

That's the only difference between a cmos and the fully nmos. I repeat if I want to make a cmos out of that this m 5 and m 6 are p channel devices and their gates are connected to ground. Essentially making them saturated either way, is that okay? You can see from here what is I am trying to show you. That this m 1 m 2 are essentially controlled by the v controlled. For given w by l and excess voltage available to me for a given technology they may give me current sources ids one and ids 2.

If I make sizes v t same; these 2 currents will be all say equal. Right now, I showed a difference when a reality I will make them equal. I have connected a capacitor here why I need a capacitor, because unless I create omega somewhere I cannot trade omega oscillations. Route 3-time omega 0 is okay, but omega pole has to be created. So, here is one capacitor; of course, right now in my analysis because this is what generally everyone does, I have not taken up parasitics, but if you put all parasitics this may go little haywire and you need a simulation to perform.

Right now, to make analytical thinking we assume it could be one c constant in reality you will have to figure out net capacitance at this nodes and that is the values you will have to figure it out, but theory wise what is it happening? Since these are 2 current sources for some reason we will see we will come back after noon because it is already time going if one of them is conducting.

Let us say m 4 conducting and m 3 not conducting. So, there is no current coming from m 3,because you said m 3 is not conducting this partly may occur because of the values which I get on v out v out bars. If there is no current here, and m 4 is providing your current. This requires ids, because this transists current source require this. now this is connected through a capacitor. So, when I switch over from state, not only one current it has to supply to maintain this, but to maintain this the other equivalent current must flow through the capacitor down. So, how much current this should supply twice.

Student: Yes sir.

So, that is the theory we are looking into inverse happen if this is on, off and this is on; this must provide 2 ids current. So, is that one ids goes there and one ideas goes through capacitor to create.

Student: (Refer Time: 63:43).

Let us see for reason this is digital circuit and therefore, m 3 is on and m 3 is off and m 4 is on fully on no current goes through m 3. If this current is coming from m 4 from power supply side, like this this must maintain one ids, now this current source is connected to the other end and requires an ids current. So, when I am switching from this off min some value here and this I switch this immediately at switch point must provide twice the current, one to go through this, and one to go through down.

So that means, it must applied twice ids currents by same logic if your inverse is true that m 3 is on, and m 4 is this, m 3 must provide twice ids currents to go through these 2 and then the capacitor, will be charge like this or charge like this, is that clear to you? This is essentially the feature of source by stable element and that is what by stable is it is not by stable, by stable is essentially it does not come out of it, it remains stable latch this is not a latch ok.

Student: (Refer Time: 01:05:04).

It is a, a stable; or rather it is called free running. So, we will come in the evening and will now study the waveform for this also for this third one. And we will also look into other oscillators time permitting.