CMOS Analog VLSI Design
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Lecture - 26
Layout of Analog Circuit

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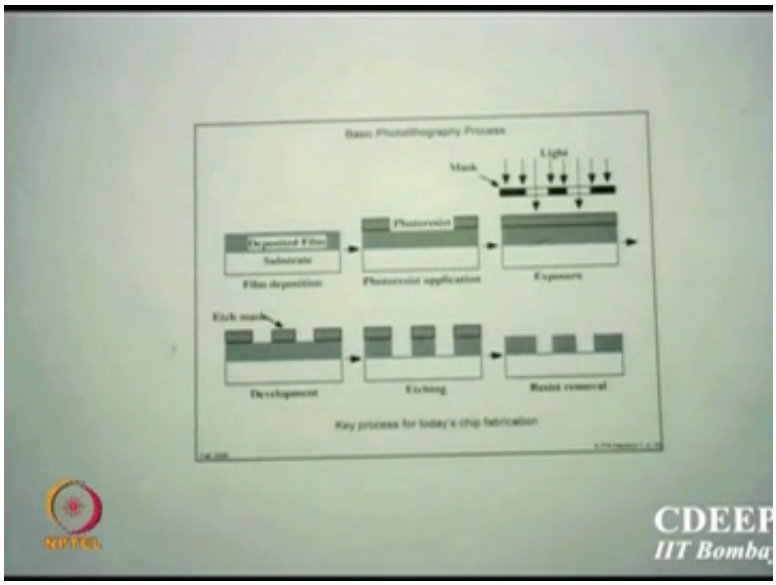

We are looking for layout issues. Last time I did quickly show you some technology maybe it is once better way to show you the exact process, which makes IC possible, this is taken from hertz handout from MIT lecture series. So, you can go on web and check. Basic idea in all the making an integrated circuit or a device is to allow you selective area processing that means, in certain regions I want to do a processing rest should get masked. So, the word itself suggests something has to be masked. So, they process which allows that particular area which you want to protect from the next process to go through, this can be created on a glass plate like a photo plate. Normally, it is the photo a multi plates, there are other methods metallizations can also we tried which is what hard masks are, but those masks have already pattern on as if like a negative at the photographic film. So, there will be dark areas and there will be clear areas.

So, this idea that the dark area can be opened or clear area can be opened decided by something what we call the resist type you use. So, for example, here is the substrate and I have deposited a film in which I had to do some selective processing. So, I say ok fine,

I coat this with a photo resist something like this and then I put a mask which has this area clear and the other areas dark. So, if you look at the pattern this is only cross section.

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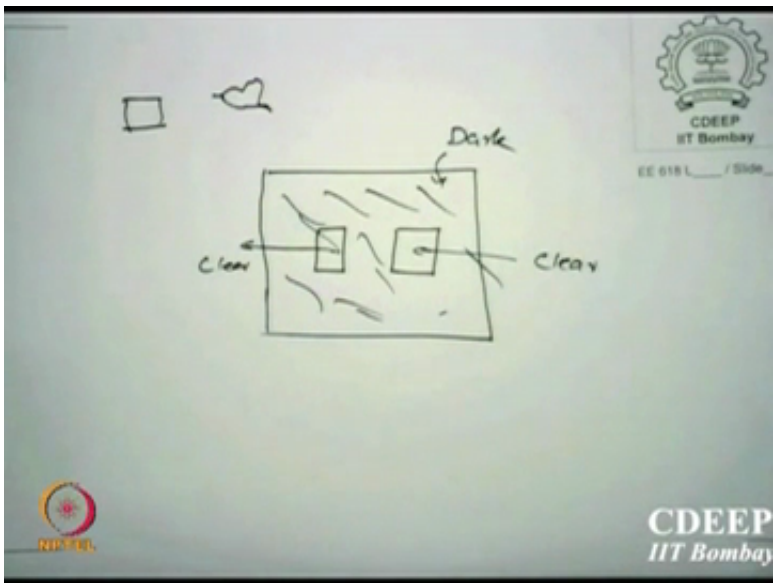

But if you look at the pattern, it is something like this. This is dark area and this is clear areas clear means, light can pass, no light can pass. So, this is called dark field mask, the inverse can occur, this area may be clear and the windows may be dark. So, it will be called clear field mask. So, the mask is kept on this court is right now kept as if it is kept distance, normally it is touching or very close to it using what we call proximity alignments. And when I shine light, light cannot pass through black areas, only it can pass through clear areas. And if say the kind of resist I have been using is called PPR - positive photo resist. So, what does essentially it means that the positive or photo resist are generally material of regimes which are a long carbon cross linking chains. Whenever that link actually fixes itself it is a huge circular rings and then it is called unachievable bonding is complete; whenever chain breaks then you say it is achievable.

So, the PPR - positive photo resist has a property that it is it is initially hard; that means, it is completely linked. Whenever light shines, photons actually received the links break. So, whenever link will break that area will become soft, soft means achievable. The compress to this would also be having a negative photo resist, which says that initially it is open that is it is a soft resist. Whenever light shines on it, it will become hard that

means, cross linked and therefore, unachievable. So, the same mask with a different resist can do two jobs is that clear or is that one clear just change the resist or using the same edges, the complementary of this mask wherever dark area they you become make it clear, how do you make a complementary just take a contact print. So, you have a complementary mask, the dark will become clear a clear will become dark, so that same resist can be used for either areas to be open or closed.

If I shine light, the resist which is below this clear area, let us say it was a PPR becomes soft. So, these area PPR become soft the darker area PPR remains hard, hard means normally achievable in most of the agents which we use. If I do so then I put that wafer on the inside achievable what is called the developer like a photography we also develop here. So, you push this into developer, the resist which is soft dissolves resist which is hard does not dissolve, is that clear? So, you since this part was soft, when I put into HN that part got dissolved and since these were the dark areas where light did not go through so that remain hard. So, I removed resist from this area.

Now, if I want to create a window in this deposited film, which is the mask area which I decided then I start etching now that the film etching itself can start with the resist already on the top. Resist is a hard material, it does not get etched in the HN for this film. So, it protects this mask itself. So, these areas resist a film does not attack only which is clear area the etching starts for the film, and you create a window down and then the rest area is already protected, is that clear? And then you remove we call strip the resist there are HNs which finally, can remove the resist they are normally organic materials some other it is some other time what are though.

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It depends on the film, if it is Si O 2, hydrochloric acid it is a HN for this. If it is any other metal like for example aluminium goes in orthophosphoric acid are HNs and HNs, silicon HN since HN O 3 mixtures, so all chemical HNs, all chemical HNs. So, I remember those HNs do not attack resist, and therefore, H and normally it is believed and which is what we shown here that there is no lateral etching going on, but it will. In fact, the way it is shown, it will be lateral, but assume that lateral this depth is not too much. So, the lateral etching is smaller, but in that is called isotropic etching.

We can do an isotropic etching where is go vertically down, but then we use gasses which call plasma etchers. So, the ion strike vertically down. So, they just etch straight way down. So, I remove the resists and I have the window of the film. Now, I can say I have frames at different areas, the waste frames I could remove. The converse could have been made if I will have just replace this PPR by an NPR, these have been protected the rest area would have gone out. So, this is a lithographic process goes through. When I say I mask I do this processing every time let us say a CMOS process is 24 masks, 24 times reference will see each time this some different masks and you keep etching some areas is that clear to you? So, this is essentially the crux of all integrate circuit manufactured.

Now the problem started the wavelength of the light, which is used typically in photolithography that is why it is called photolithography is to be order of the ultraviolet light, which actually allows resist to exports 2900 to 4200 Armstrong is light wavelength which we use. However, this wavelength itself if you see lambda is very large right now 4000 Armstrong is a sufficient wavelength, so if you are reducing your feature less than the wavelength itself then the diffraction, and refraction both starts and the pattern cannot be exactly a stout that lithography will not be correct. So, we will have to reduce the wavelength of the light.

So, from photo you may go to electron beams which can have then higher energy and lower wavelengths and their photo resist will be different. There will be other organic material like polymethyl acrylate, many other materials can be tried. If you want further lower wavelength, you can go to x-rays; if you want further ways can go to ions the larger. The mass you pick up the hit it will give to the material will be hard and material will become actually non-crystalline. So, one cannot use the analytical fee very easily because it will actually damage the wafer itself, but no one wants to really do electron beam lithography, because even electrons have high energy therefore, their lower wavelength. So, they will also actually damage the silicon below.

So, somehow what we do we create the mask this mask using electron beam lithography which is on a normal glass plate. And use that corrected mask and use lithography like photo lithography, but the problem they have done etch how good the patterns transfers. So, there are different ways of doing it, and now what is the wavelength we are using is called extended UV below 193 nanometers. And there is an latest process which

probably Intel will start working this year EVU extended UVs. So, these are the things which are going on. They are all problem, which technology people now getting because of 20 nanometer-30 nanometers or less is there such a small disk when I actually do whatever etching the pattern, which I see and nothing to do a pattern, which was on the mask.

So, for example, I may have this actually, but what I may get is something like this actually. Now, how do I get that area which are W by I was looking forward. So, now, the issues are. So, do we what we do called phase masking, we do some do DSP or image processing. We figure out for different patterns, if you have this pattern what do you really get because you know the transform and see if I want this, what should be the actual pattern, but creation of that is not so trivial then there is called projection mask alignment. There are many techniques, which are tried now for going to less than 20 to 30 nanometers. Lithography was very simple till 1 micron. As you gone down scaling, scaling, lithographic will first hurt the major effort therefore, went in lithography process.

So, electron beam can directly write on the wafer you do not know any mask you actually wherever resist you want you open put lie electron beam can be very sharply focus through ACM. So, I can actually write patterns on the wafer itself, but each chip will have so many transistors to write and then the 100 subscripts on a wafer on hundreds of wafers to be done. This is called direct stripping, direct write is very costly because you know every wafers has to go through hours of printing before you that is very accurate, but that is very expensive. So, people who have money and who can sell the chip for million dollars can value do that direct stripping; otherwise look photolithography then has to be performed for the larger numbers to be created in one go. Some image for assessing new techniques mask production printing many tricks are being tried lower UVs are being tried externally UV as record. And this process is very right now no one knows exactly what is the way length Intel is going to use the machines are made by themselves. They resist of their own way and they are not right now allowing people to know what exactly this extended you will be and can they go up to 7 Armstrong’s or 7 nanometers.

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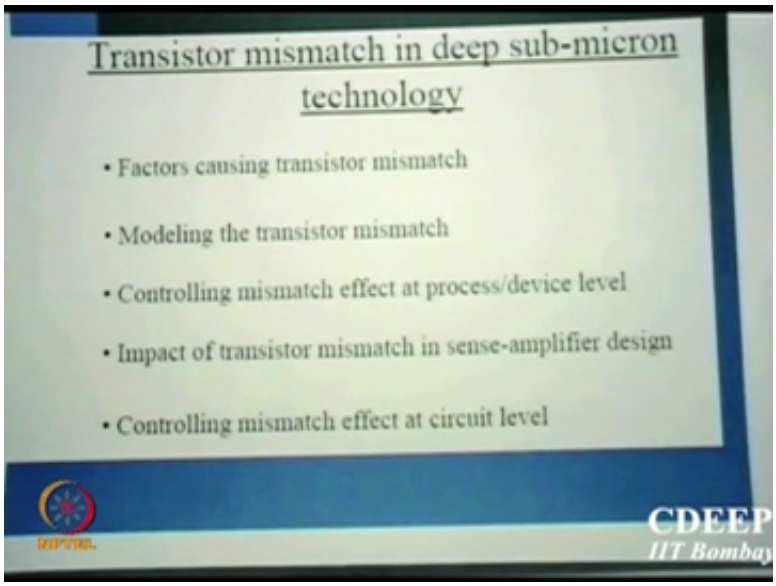

The problem which we say in real life is essentially called the mismatch problem. We are already seen in our analysis that if beta is delta V beta plus delta beta plus minus what can occur. We have seen all such variations can create what kind of actual problems for you. So, now how to elevate some of them not that everything can be minimized, everything can be removed, but minimization can be tried. One technique is to get into a layout problem, which probably can say some of your mismatch problems.

So, what first look at into mismatch, factors causing transistor mismatch. As I said there may be number of way because of this it can happen. One of course is I yesterday said there were many, many transistors on a chip, each mask will have different chips; and when you align they have further different chips at the end of the day each chip will have different everything different. So, a misalignment then there is a something called misalignment. When you fixed one by one over the other, whatever you say it is not hundred percent matched, and add this base sideways it goes further different. So, there are issues which is mismatched issues.

Now, first thing you must do how to model that mismatch. If you can model it partly we can take care in designing. There of course, can be computed the process and the device level like threshold can be controlled to a great extent by different methods. So, we try that. Then impact of transistor mismatch you know one of the major variant design was or the sense amplifier design. They are the mismatch created the hell of this one zero was

never guaranteed them and we are looking fast exorcist, there is first time people realize that this mismatch can create huge problem in the reliability of a design. Of course, one possible main technique is to control at the circuit level. So, you know how much is offset, you have you try to cancel as much as possible; if it is a systemic offset. What is systematic, way in one direction.

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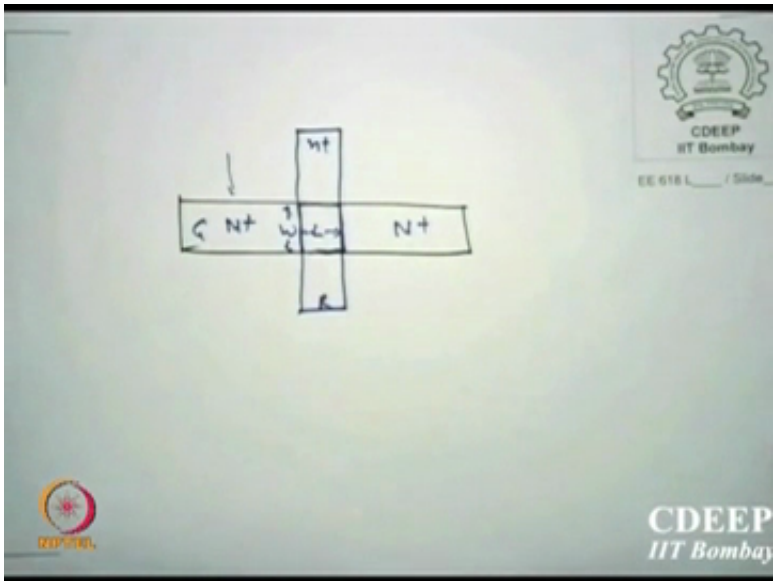

So, here is something which looks trivial the way transistor works you have a diffusion area of course, there is no colour the four colours here, but maybe blue I will call it red; black I will call it green, this is red and this is green. So, normally what is done is first poly is printed instead out and then implants have been done at the age of poly. So, this become n plus or people as whichever turns that you are making, and this also becomes n plus, but below there is a oxide, below all polys will be a thin oxide gate. So, since this is the area where gate oxide below is available, so this is the channel length and this is the channel width. So, fixing this, this is an area or such an area and the poly widths decided W by L of any transistor. So, whenever I show you a green line intersecting red, there is a transistor below wherever is the common area. So, it is called G intersection R.

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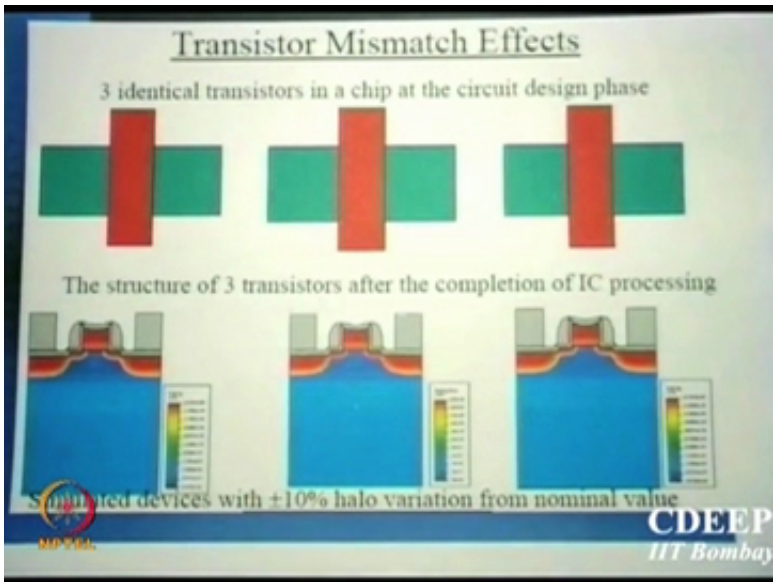

So, where is that G intersection R shown, this is diffusion or is n plus and this is poly which also we will receive n plus, when I am doing this implants. Now, use tend to see three are almost identical as far as if you see the pattern that say but in real life the colour shows that somewhere diffusion is larger, some is smaller some is shifted left or small is shifted right that is not visible so much from the pattern itself. But in reality the process down has created the shifts, because as I say lithography process is never guaranteed process. Now, this three structures after IC processing are not identical to each, and therefore, these are so closed by to each other and still they are not identical. If you are far away unlikely that all will be of same value; and how much you can tolerate is your design space, this is called some other process say, hello, but let us call it.

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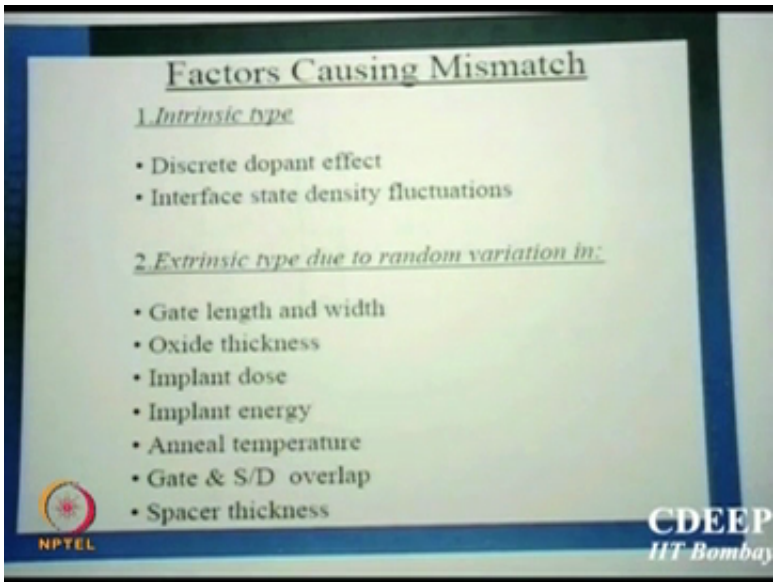

There is a intrinsic factors which is causing the mismatch which is called discrete dopant effect; then there is the interface state fluctuations. Extrinsic because of the process there is a random variation in gate lengths gate widths, oxide thickness, implant dose, implant energy, anneal temperature, gate and (Refer Time: 17:09) overlap, and spacer thickness spacer generally comes in the case of infests. So, there are many variations going on, these are called process variations, designers must take care of process relations, these are statistical in nature. So, some statistical analysis should be actually attempted that is what we do sometimes one of my Ph. D student work for this process, how to correlate process variation with circuit performance.

As you reduce the channel let say the concentration because of the V T, which you are adjusting is such that the volume there that is at 10 to the power 15 for sake of numbers, the channel length is less than 10 to the power minus 5 centimeters - 0.1 micron or lower. So, what is the volume 10 to power minus 15; if it is lower, it will be 10 to power minus 16, 17 per cc as per cc. So, what would the number of carriers there is less than 1. So, one cannot guarantee say where is the electron where is the carrier. So, there is an issue which is called dopant effect random dopant effect.

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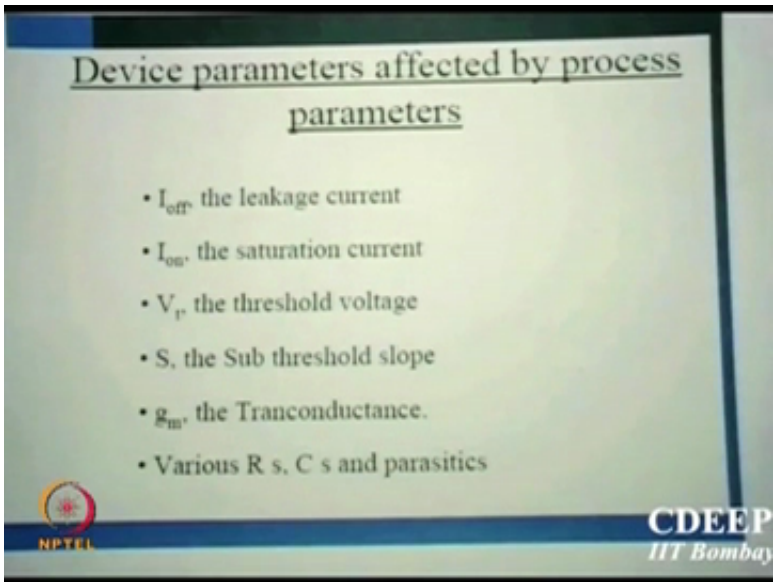

It will affect the off current, it will effect affect the on current that is the saturation current, it will affect the thresholds, it will affect the sub threshold slopes, and it will affect the transconductance and all R s, C s and any other prosthetics which are area dependent and dopant dependence we will also get variations. So, if you see a device parameters which worries you most at the in circuits because at the process variations all will be moving from one and please remember about our worry is on chip variation chip to chip variation result wafer variation, and run to run variation run means two hundred one run next two hundred run. So, run to run variation, so huge problems. We do everything fantastic we say everything is controlled and then we see all variations.

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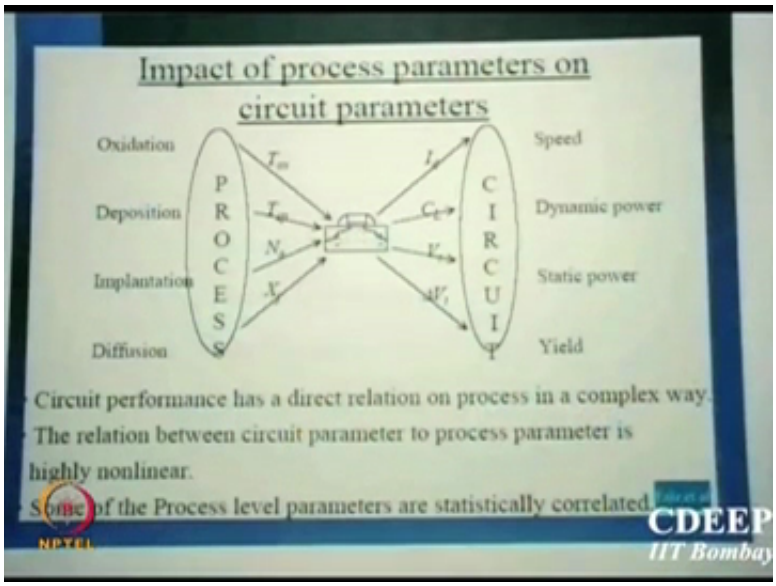

So, if you look at the impact the process parameters on circuit, yeah already I said current capacitance threshold variation in threshold. So, they may change speed dynamic power static power and the worst is the yield it will actually reduce, the what is yield as I said this is the minimum specs I will expect, anything goes beyond that that should be is not up to the mark. So, that chip is wasted. So, we say yield. So, at the end, if you find your gene going 50 percent, the whole process is of no use. This statement is very interesting that there is it seems that there is a direct relationship, but there is a non-linear relationship because all the expressions are non-linear at the end of the day.

So, it is very difficult to actually predict which one will hurt you most and when and that is the analysis someone has to do is called statistical analysis. Of course, as I said some of them are co relatable some are uncorrelated processes and then this much difficulty actually predictions. I will not going to detail of statistics. This is an area of our students Ph. D work, just to give an idea a threshold varies and there is a reliance, which is different for different processes sigma of delta V T.

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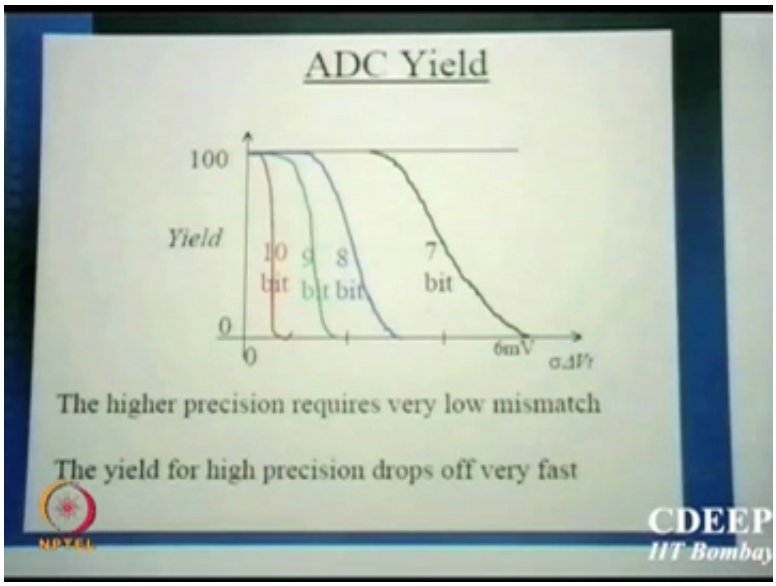

If you see this term, and I had taken an example of ADC, ADC is one of the major device in the analog to digital converters with almost mixed signal most important chip or circuit. So, if you see if I have a 7 bit ADC, the sigma allowed to me is around 5 to 6, anything below let us say 5 yield is ok, but if you look at the 10 bit ADC even a half a millivolt shape of sigma then we will may go down 0. So, the decision of making even this was done only for 0.25 micron process. If you do either further down god knows what will happen if 12 bit or 16 bit ADCs are use somewhere. So, the precision and mismatch are very, very crucial in analog designs as one example I am showing you this is how the sample hold actually changes the equivalence of analog to digital.

So, 1001 pattern may become 10111 kind of things and which will not be representing the actual digital data for the analog. So, there are issues which essentially process people know that at the end nothing will come. And therefore, layouts become extremely this is all just to tell you all that why layouts are so crucial at the end of the day and layouts are the only thing which as a designer we create the W by L sizing. And then when you lay it out things may work or may not work if you have not taken enough precautions on that.

As I say basic layout design techniques should be taught by Prof. Madhav Desais course that is the issue where digital designers should learn more about that. This course has no such area left in my course where we say layout design; otherwise layout editors is a part

of any design process ok is that point clear? Why I am worried about mismatch so much because money economics is worry, (Refer Time: 22:57) no yield then what do we do. We made so many of them and there is none working well. So, that is the issue which companies like nationality everyone is worried about where who sell ADC chips or analog is that ok, the issue is clear to you why a mismatch is really worrying.

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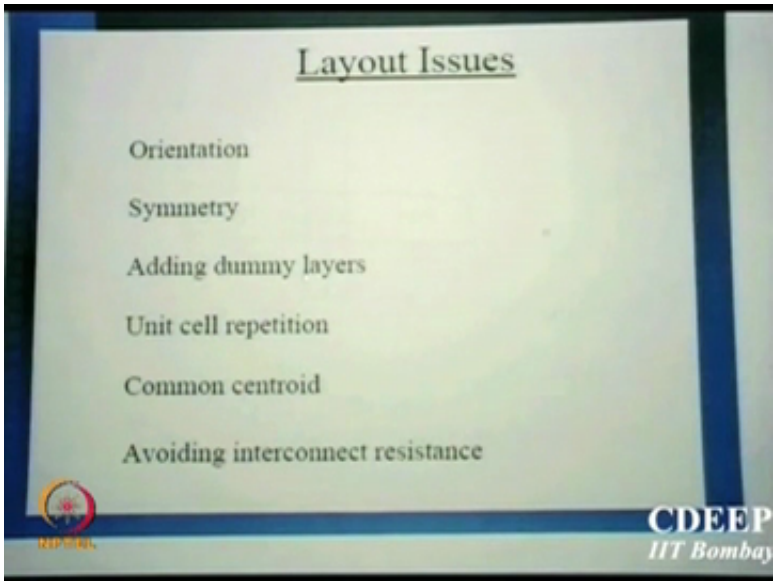

So, there are issues in layout one is called orient we will come one by one. Whatever is now following I have been figures have been taken from Razavi, there is a chapter on this mismatch word itself is mismatch there. So, look for that chapter. And I will show you what is the worry there. The issues of orientation of layout symmetry, adding dummy layers, unit sale repetition, and the last, but not the least the last, but one is most important called common centroids, and avoiding interconnect resistance. These are the issues which as a layout designers you must be in by the way in design when you will design a chip, do you make the before the metal mask comes, the process is called front end that is designers W by L s have gone in. So, it is called front end. The rest of the process to make interconnects back end whatever and this all issues related to this, these are called back end processes. These are torturous, boring but they are paid higher than front-end engineers, because their testing is the last part which they come to it and there is where they start looking things what is happening.

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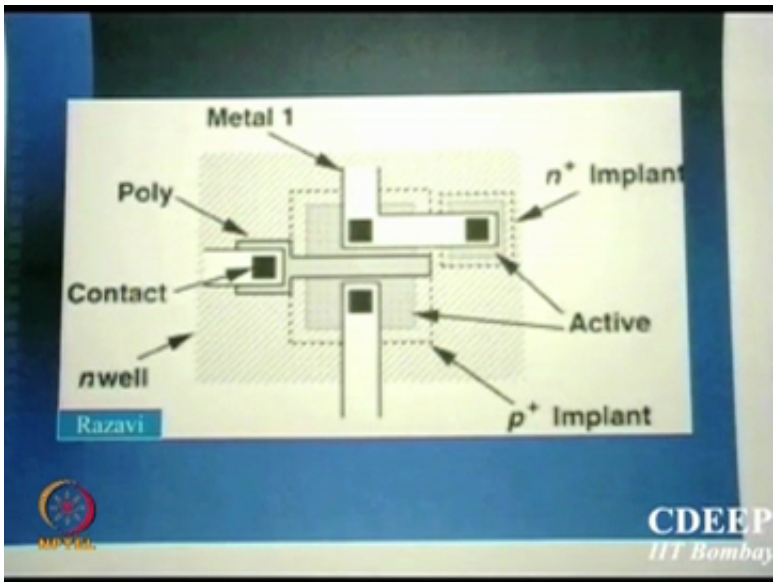

So, here is something typical this is shown to you. There are two devices shown here; one can see from here this is the poly that is this is the gate, which is shown here. This is the p plus implant; this is an n plus implant. And one can see the items only one terms shown the other partner has not shown. This contact is essentially called metal one there are more than one metal possible each metal is separated by oxide on the top. So, what we did is for they say people has implant for size n we did here , but we will now did that open the contact to the gate to the source and to the drain. So, this is essentially called active regions. And the ends of the method is any metal one normally runs vertical, any metal two runs horizontal; normally they are not running in the same direction or no angles at layout should never be at 45 degree or 30 degree parallel this normal x y system is always used, these lines are called Manhattan lines.

Why ok, some of you might have visited USA and you have, Manhattan has avenues and streets exact some type with if you go some way in the Mumbai avenues and streets actually we will copied from there. So, Manhattan has all routes like this, and all streets like this. So, this is called Manhattan lines. So, the way right now you can see there are different directions, I am taking metal out and that is not acceptable to me, because if I do this process for n number of times, it will show you much more variation from this unless I am symmetric to something. So, I will show you what symmetry would show. So, this kind of interconnects, I am not treated well where you will pick up connection anywhere, anytime, and run anywhere, anytime it is not a good way of putting your

layouts. This is given in Razavi's book specifically written, so you do not write can look into figure there.

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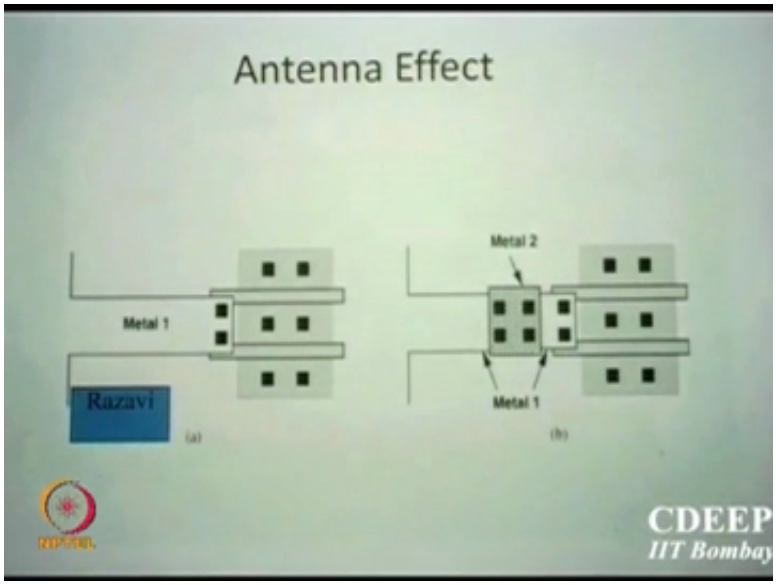

The another issue which is called antenna effect and one can see, this is a normal transistor, these are two devices shown here for example, polys. Please remember these are two transistor in series, do you see them source, drain, source. So, drain up the two have same, but it is only a matter of decision to say because they are symmetric this also be can souse drain. So, you say connect source and drain in between are called drain of both together whichever you feel like as long as the devices are symmetry. There are other devices called asymmetric those devices like L DDs and others they do not have source same as drains. So, do not connect like that. Now, what we do is there they look to be in series essentially what does two transistors in series means equivalently of one transistor what does the show two transistors, before we go there may be a simple figure can explain you.

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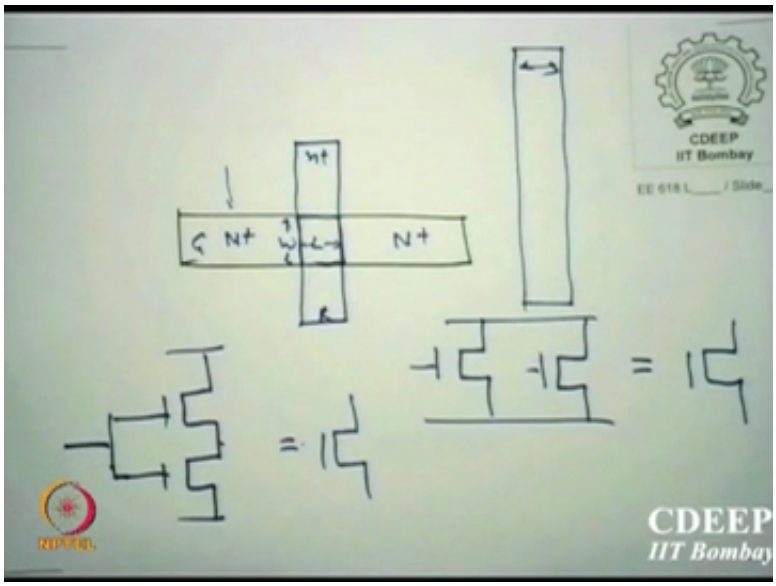

This is one possibility same connection (Refer Time: 28:10), this equivalent of what and this equivalent of what.

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In this case, the lengths are doubled, widths are same or whatever we would said; in this case, widths are doubled and lengths are same. So, transistor sizing whichever you come normally do not put huge size transistors, break into either series or parallel combinations, so that the uniformity of each probably is much more maintainable. There is a word, which we use in layout which is called aspect ratio. What is the word aspect ratio? Let us say this is the line - length, this is small much smaller compared to this. So, whenever I will do etching, I cannot guarantee etching here to here same, because I am going through a huge lengths. So, the length here may not be same and length, here this is called aspect ratio issue.

So, do not run too long issue lengths break into as many as you want either using if you want W to be higher or length to be higher use either of the methods to actually break into smaller number device large number of devices to equivalently putting. Well digital people, they have doing digital course, this also has an advantage this called gauge stacking [FL] important [FL], low power [FL] [FL]. This is one of the most important technique of reducing power in a digital circuit.

So, now, what we did it this is the similar transistor shown here. So, one method you have that you connect common gate together and put one big metal. There is a suggestion that if you have a single metal layer connecting to the contacts here, and you run it longer as we did here, it gives like a some kind of a resonator circuit on a oxide. In any insulator, if you run a metal line it acts like an antenna it is a radiating system. This is what we do in the MICs instead of there in alumina substrate or other substrate you have silicon-silicon dioxide substrates. So, it runs like an antenna, so it radiates power. So, much of the if you calculate the pointing vector here the huge power losses at the same.

So, to derive this we say the metal one where is the contact is coming, which is the dissimilar discontinuity as we say you made it that small and run on the other metal on the top through oxide through a window to that which will actually take care of those contacts away from the actual this. So, that the radiating patterns will be restricted only here, which has a smaller power loss. This is called antenna effect. So, [FL] designers [FL]. If you like this yeah in some frequency it may still work, but higher the frequency you go this will be one which will say there is the relation is much more than the power delivered to you. So, these are issues.

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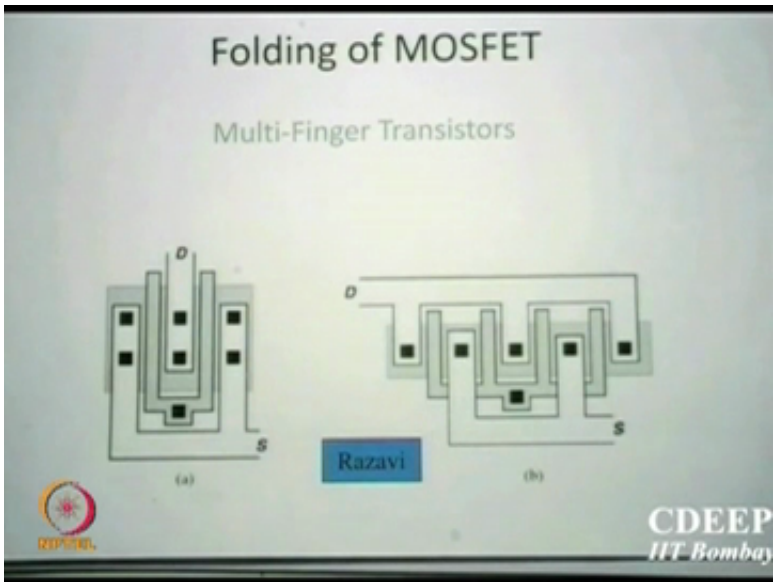

Another issue which I just show random disconnection. So, one method is for example, this can surrounding you can see here what did I do there I have two gates. So, here also have two gates finger these I have a called fingers common point here. And the drain

contact is taken in between. This is drain, and this is source, is that clear. Source from the outside and something is the drain. So, I took drain here, source outside and connected them also this is still a single transistor. Please remember sources are common drains are also connected. So, what does it means its parallel transistors two are connected here is that clear to you. This is essentially how is called folding or finger structures. You can do larger numbers, if you have large number of W by L is to be connected put equivalently this, sources on the top drains on up or what you opposite called source drains are same, whichever is which are is drain and in between run colleagues likely zigzag.

So, you can make, can you can make can you now see these structures are more symmetric, you take symmetry across this or you take symmetry across this. So, there is a symmetric structures can be created by actually folding them, hold properly as much as you can and then see to it that symmetry is some way attained. It is called multi finger transistors, the same statement, which I made, if you have a very large sized transistor wide, you can have two sets of them and in between connect multi fingers and then connect together. So, there are not larger the size tricks to be.

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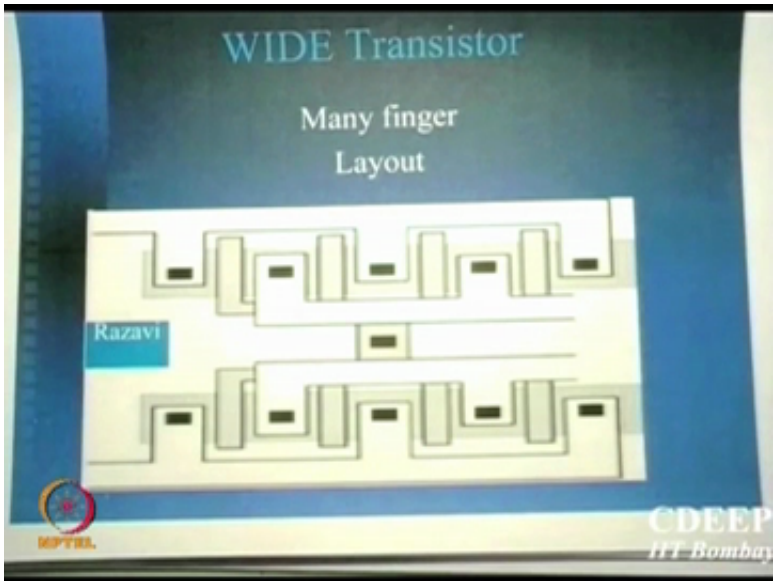

Again you see from here it is trying to get into more symmetric systems; our ultimate aim is getting symmetric systems. Why I am looking for symmetry, anyone? Because whatever processing I do, if all sides is similar then they are likely to replicate everywhere the same aspect ratio issue will never come into picture. So, larger the

fingers I create more likely I will get symmetry structures and more symmetry means much more uniformity of etching if lithography is possible. Please do not draw because it takes hell of time and these figures are available, just to explain you what is going on maybe I will put it on the web if you wish.

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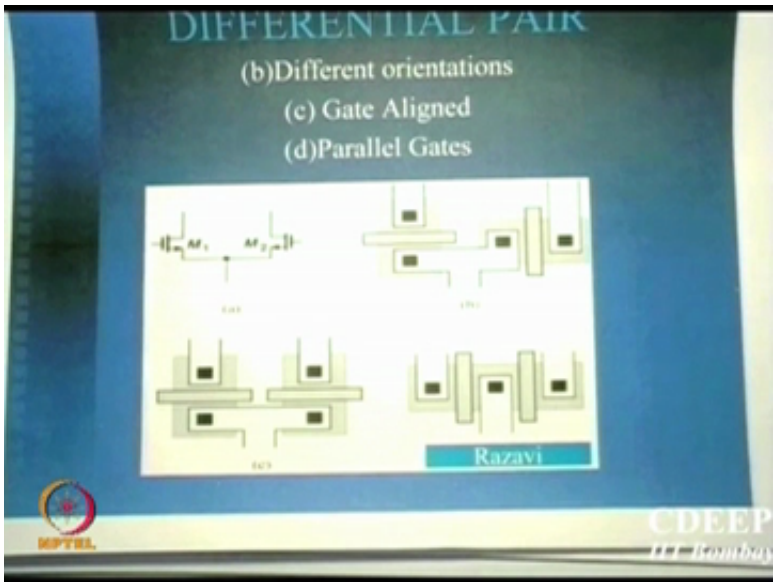

The differential pair which is the most common circuit you will use, you can see from here one method is you have one device here, you are another device here. Now, you can see I have one poly that is one input gate is like this, but the other is I made like this now it is not symmetry. The source I have made common, one drain is going, but the other drain is away from each other like this, these lengths are different than this length for the contacts. So, what should I do then I should either do this or I should do this, now you can see our identical drains, identical source. So, if you take symmetry across this, diff amp has a symmetry that is what we have been all time telling if you no doubt only then that diff amp has its symmetry requirements.

So, if lay it out only then the diff amp easily accessible to you. In these you can break more devices if you wish, but fold it now this one folded symmetry do like this, you can make devices and I it will do these, but again it is symmetric. Symmetry is all that I am looking for any lithography process. And therefore, any layout I make has much more worry in symmetry points is that ok, there are rather nobody which analog people gets problems into.

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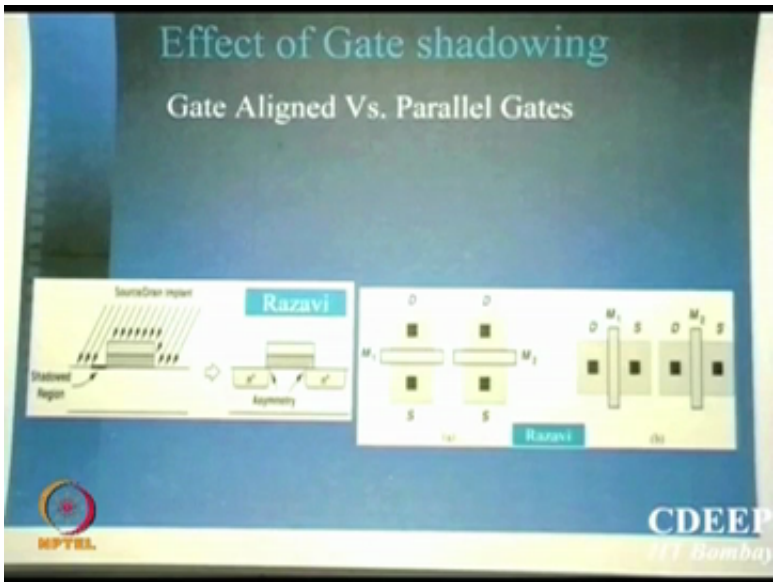

Here is another problem which we observe it is called like when I was making where n channel device I had this offside and gate delineate at first and then implant source-drain. But that is a the way implantation process goes many of you might not be aware those we are doing technology course in our other they might have seen already implants. There is a columnar tube may be of any size of 8 or 12 inch electron beams sorry ion beams a particular dopant or what whatever implant you are doing is actually getting focused by electromagnetic fields. When it comes as a focused beam, the wafer is orthogonal to it , but the distance and the focusing is done by lens electromagnetic lenses, the wafer does not have exact angle of 90 degree. You have to keep it at least 3 to 5 degree off some other day it is a part of requirement for good implants.

Now, if I had an angle this will get lesser this will get higher because focusing here will not be there this is going to happen. So, I will click the beam anywhere. So, 3 degree beam at least I will shift maybe 5. So, I will not actually have 90 degree orthogonal beams further I have to scan them. So, when I scan them, it is a like a normally last stress are came, but some people do vector also. So, when I flash back, residual implant comes. When you come back to original position, there is a residual system. So, on the left and the right you do not get identical implants.

The reason is you can now see this n plus and this n plus are look at say here it is very internally very small, here internal it is larger, larger the inside part essentially means

capacitance is increasing. So, it is called drain capacitance. What is the problem in drain capacitance increase, your pole actually will move it may become dominant which was in there.

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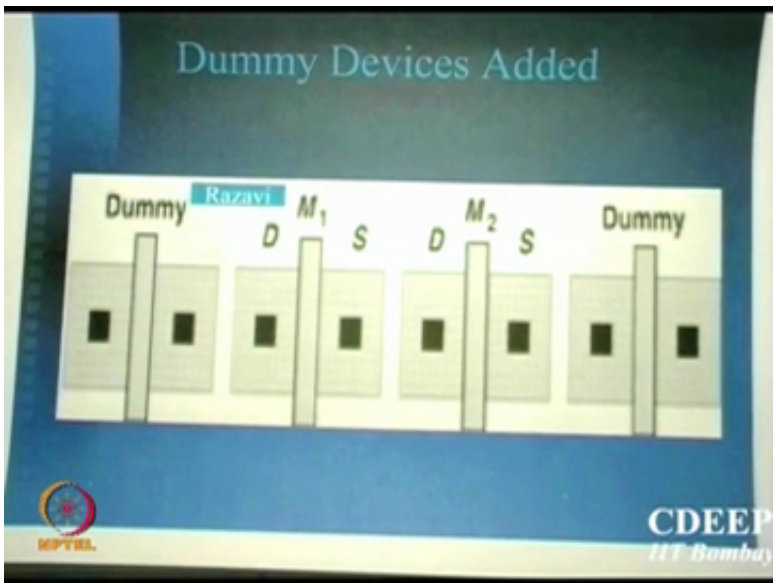

So, what we do now in this, this is two possible structures which are there. So, we do something very interesting. You have these two transistors to make, you actually put another two transistors. So, now this transistor on its left sees another transistor; this transistor already sees another transistor; this also sees another transistor. If I take it away this side is different from this side in between. So, what I say is to clear a symmetry, I actually create dummy transistors on the left side or right side. So, this is called bias. So, whatever bias IC on the one side, IC exactly identical on the other side these are called dummy transistor at least if not put transistors, at least put poly lines this poly to this poly because there were the implant edge comes. So, the minimum requirement in analog is every transistors if they are not together, they must be surrounded by parallel poly lines to create symmetry for implants. Is that correct? Yes.

Student: (Refer Time: 39:24)

You can see from here if I have a large beam coming if I do not have this there is a energy going other side. If I have back here, I have energy only equivalently on both sides. So, to keep energy distribution of the implant same all source drain side, I must have walls as a both sides. These are essentially walls for that dummies as they. And they

are not being connected anywhere these are dummies, if you put transistor you are area put transistor itself, if you do not have area at least put poly lines everywhere to protect your internal parts is that clear. So, if you see analog, this is what is needed. In digital why we are not interested so much because noise margins are sufficiently high any such things goes there it will probably take care at the end of the day there is no margin here anything goes wrong amplified, so that is where you can analog.

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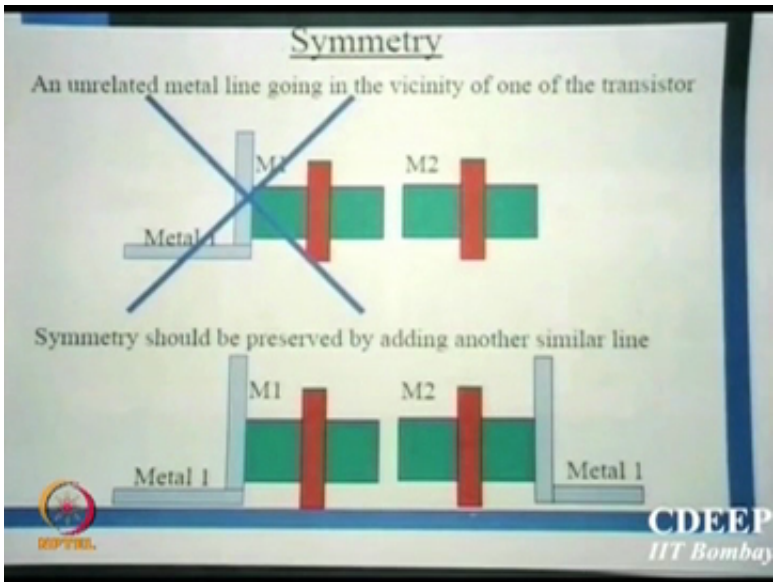

This word symmetry you can see from here the two transistors, and I am connecting a metal something like this, but no connection on this side. So, do not do this. You do metal one and metal two on if you think this is not needed then connect it anywhere is that clear? If M 2s are not needed, do not run it anywhere, but near transistors keep them. So, anytime you do on the left useful; even if it is not required put same thing on the right to be have symmetry structures. Now, I must tell you what is my worry with this, with the next one which I will do as a circuit to this, may be you will get this figure.

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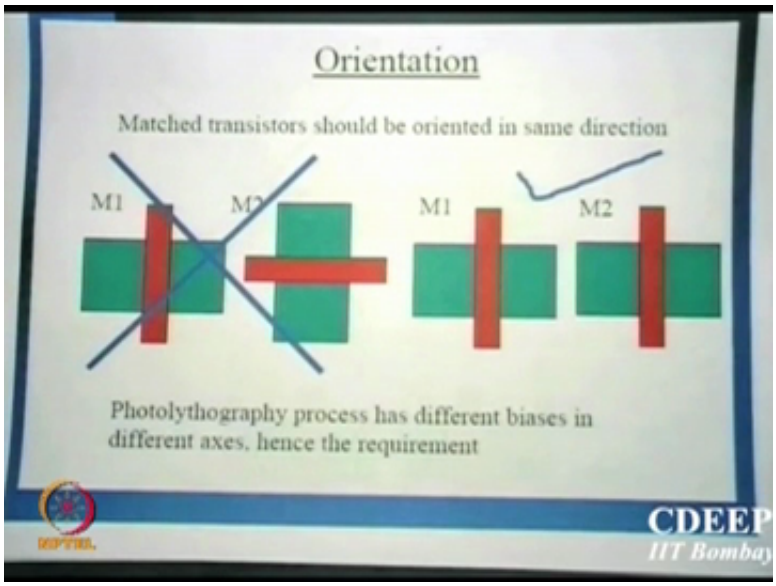

This is also one matching problem. If one is vertical poly, here is horizontal for a never do the same, run always same direction. If you have this, all of them should be horizontal or all of them should be vertical. Of course, preferably do everywhere the same, but other than same you may be change also, if you need connections the other side. So, the small area whichever cell area you are creating symmetry has to be hundred percent maintained. This is called orientation effect. There is something which Razavi thoughts, but then I will do some maths behind.

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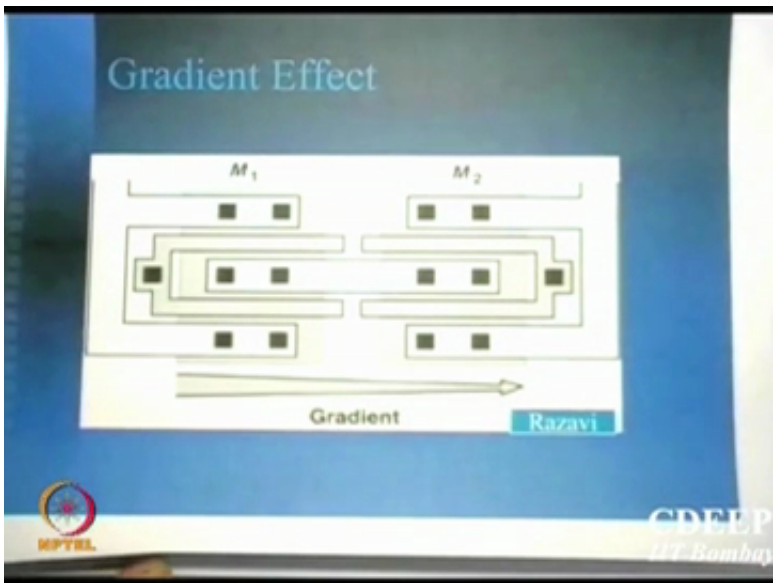

What we say from left to right, there is some variation called gradient of the sizing for example, because of the process whatever I do actually there is a gradient in the process. Now, what it can create here is an example which I will show you. Assuming right now linear gradient linear gradient means it is much easier in real life it may not even linear gradient.

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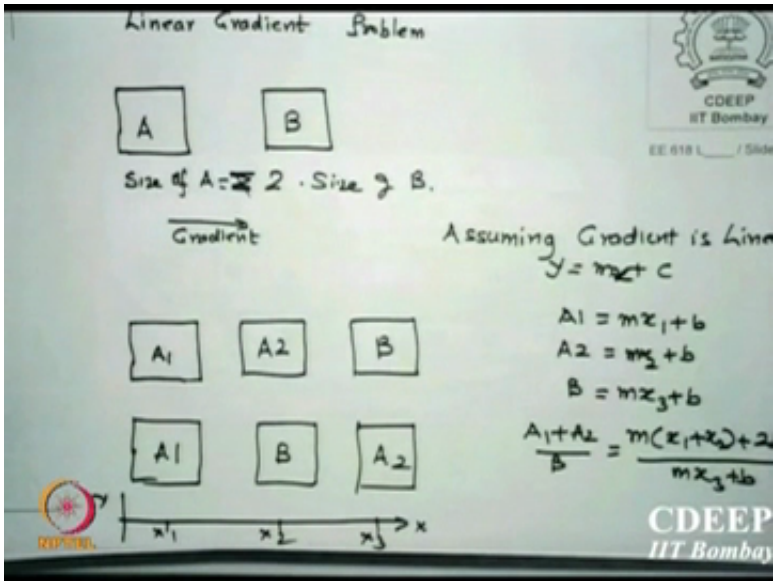

Let us say the size of A pattern is this is equalled you know so slightly equal to twice the size of B and let us say maybe the gradient on the left to right linear gradient. So, then actually I have print this, this will not remain double that of B, is that correct, this is essentially worrying us most. Because then we decided to areas to be double out of this, but in gradient this will not allow this to happen. So, what we did is some interesting feature of course, these are many other transistor should have the area should have been shown, but I just chose for one. Let us say the gradient is y is equal to m x plus c linear gradient.

For A 1 let us say A is broken into two areas A 1 and A 2. So, I write A 1 is m x 1 this is for A 1 m x 1 plus B, B is the intercept. A 2 is m x 2 plus B; and B is m x 3 for this plus B. Now, if I write A 1 plus A 2 by B, I get m x 1 plus x 2 plus 2 B by this; however, this does not become twice unless this becomes 2. Now, this can only become 2, when the x 3 is equal to x 1 plus x 2 by 2. Now this is an issue, this is an issue x 3 plus x 1 plus x 2 must be average on that must be equal to x 3.

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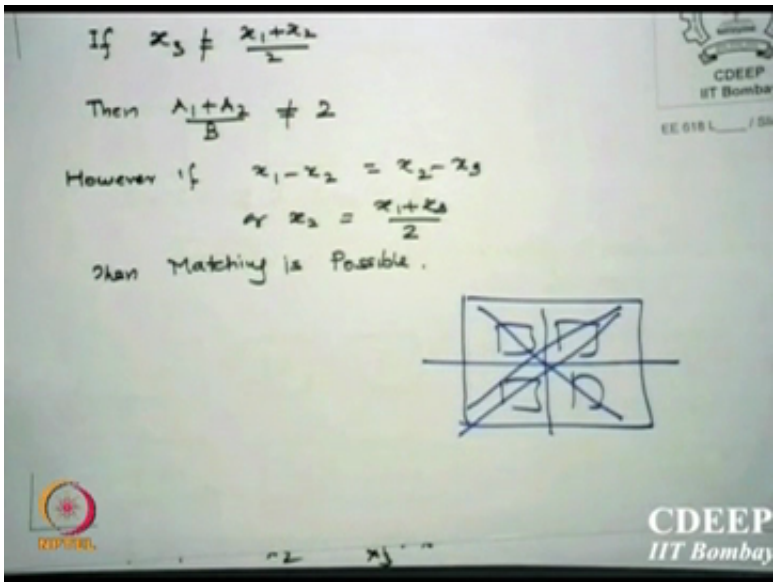

Now, this problem which we see if x 3 is not x 1 plus x 2 by 2 A 1 plus A 2 by B 2 is not equal to 2 either. So, what we now do we say ok, put x 1 minus x 2 and x 2 minus x 3 same or essentially saying x 2 should be x 1 plus x 3 by 2. If I do this x 1 plus x 3 by 2 and put B here. A 1, A 2 is across this; similarly A 2 should come on the other side and A again. So, this is called common centroid, this is called common centroid. So, if you have a circuit broken into a parts I do not know where I have a figure, but I will show you what it shows there may be blocks here along this axis sorry along this axis along this axis, along this axis, it is identical.

So, let us say where a variation from this is A 1, for example, variation here opposite will appear here. If I connect them then variation in the two is getting cancelled, is that clear. So, I do always common centroid breaking into blocks, so that the effectiveness of variation can be cancelled or at least minimize. So, all analog designers should make their layout common centroid. So, for a W by L [FL], so that. So, in diff amp also you have two transistors M 1, M 2, M 2, M 1 by 2, M 2 by 2, M 2 by 2, M 1 by 2.

Now, you can see it is common to all four sides and therefore, it will show minimum gradient effects this is an issue which is called layout issue which if you do not take care then the problem will be the sizes of what you actually we are creating are not getting transferred is that clear. So, one difference from digital hardware the analog is every layout in analog is common centroid that gives the maximum symmetry. At least if not

that do some symmetry at least preferably use common centroid, but at least symmetry you create minimum that is what is expected. Now, here is something very interesting data which is given by not data calculations given by Razavi.

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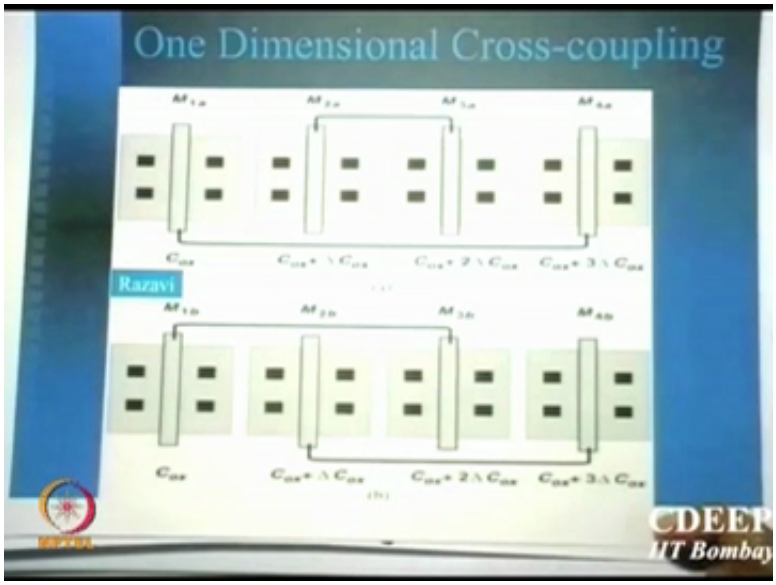

Same thing can be explained from here you have four resistors M 1, M 2, M 3, M 4. Let us say due to the gradient it has a oxide capacitance of C ox, it is C ox plus delta C ox, C ox plus 2 delta C ox, this is C ox plus 3 delta C ox. So, one possible technique is you connect these two and you connect these two. So, what is the capacitance you are going to get ox one plus there is no 3. So, 2 C ox plus 3 C ox delta C ox, here 2 C ox plus 3 delta you do this way. You connect this and this, and you connect this, and this then C ox 2 C ox plus 2 there 2 C ox plus this, so as say this become four.

So, depending on how much symmetry your gradient you are expecting you must decide which transistor should get gate connections, which transistor should not we should be closer by. So, do not put connection at least this, this is the worst connection this is 2 C ox level this is 5 delta C ox it will come. So, either try this or try at least this, so that you get symmetry as close as possible which is created due to gradient in the process, is that clear.

So, now, the all that I am going to show you that why an analog layouts it is different from, so virtue source which is the famous layout editor in the case of guidance. If you see analog designer, there is a separate shell in which you work. If you have a digital

designer you work in a different shell, the reason is this layout build it both a virtue so, but there are different virtue source. So, it is actually designed for analog the other is designed only for digital hardware. So, please use it do not use the magic, because magic is it has no connection with anything neither analog nor digital, it is only a graphic editor. So, there you can do anything you like physically by forcing it. In real life, we are not allowed to force ourselves, system will actually tell you, you are going wrong, but you are always possible to over use it, this is allowed and, but if you do that you are taking a big risk on yourself.

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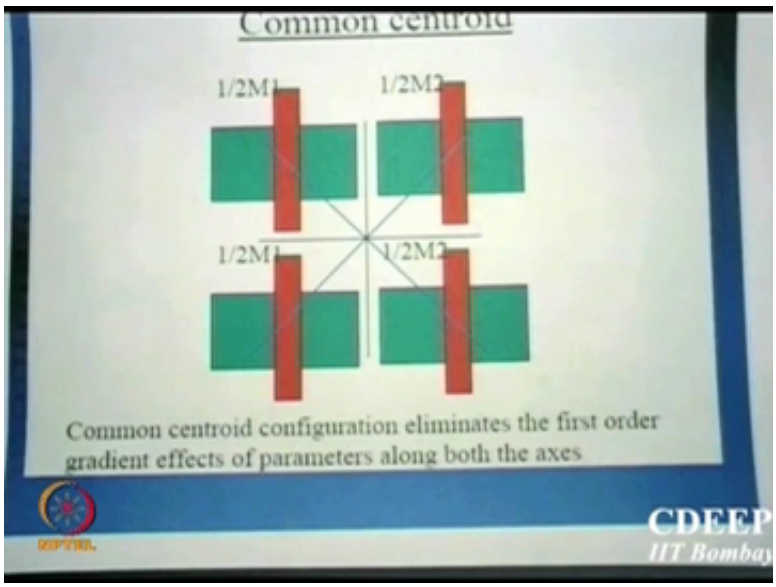

The circuit which I showed you earlier I should I have showed now this is called common centroid, is it clear? Half M 1 half M 2 half M 1 you can even flip this even better. [FL] symmetry [FL]. So, this is called common centroid, [FL] centroid [FL] similar [FL] symmetry [FL] [FL] break [FL]. The last part of this we have only seen transistor so far in analog what else you need resistors and capacitor of course, we also need inductors, but this course we may not talk about them.

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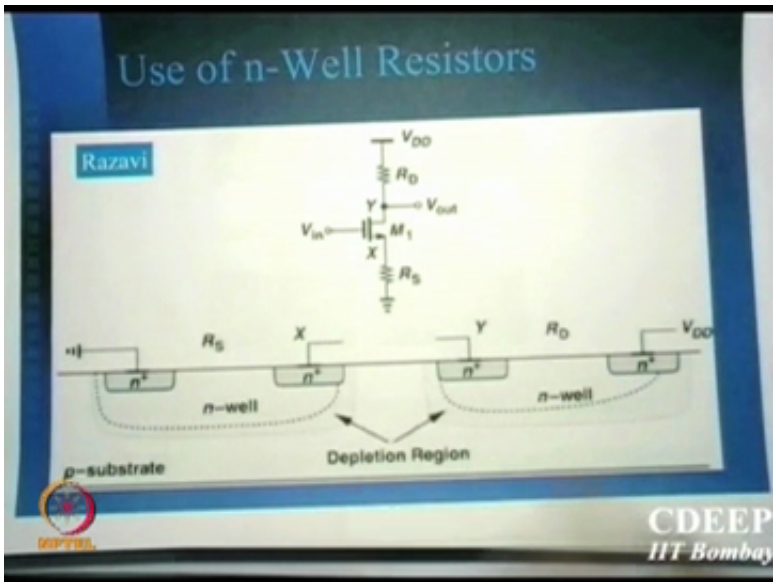

Here is the resistor, this you can write this is not a very big circuit you can see from here these R S and R D are not the transistor registers are put these are essentially the resistors which is sources drain area resistors actually I show also put R D in case if you need. So, how do I do this? If I have a n-well device area there I yesterday said you start with the p substrate and create a deep area which is called n-well, well means five micron down or three micron down that is why called well. Please remember in circuit only first half a micron or even layer is the actual surface area you will use, surface depth you will use, all devices are within 5000 Armstrong's then you do not need further then why do you need so much thickness of silicon.

Because extremely fragile and to handle it at least you should have some stability. So, for 12 inch wafer you can now understand why it should be relatively much thicker, because twelve inch wafer will huge mask and if may just break by seeing. So, you must actually put some this, so that it hold. So, so typically one and half millimeter to two millimeter thickness wafers are used for 12 inch for 3 inch wafers 250 microns are sufficient thickness, but the device is going to be within less than a micron. But the wells are normally slightly below this is that correct, because device has to have substrate kind of effect for source and drain. So, the wells are typically 2 to 3 microns over time it we used to make it 5 microns. So, if in a n-well, if I make n plus contacts n-well would have some resisitive sheet resistance rho by T.

So, R S is known, this is my length, there is a width in the inside this. So, L by W into R S is the resistor value. So, adjusting this and adjusting the second parameter width of that I can decide how much is the resistance I want. This since it is a p substrate this is the np junction. So, there is a depletion layer going on is that clear, this depletion layer should not connect, this called punch through the two register will get connected. So, there is a rule up to which two resistors could be brought together. Normally registers are created due to the implant areas available to you, so which are the area available substrate N plus implant, p plus implant the on wells. So, there are 4 R S is available to you depending on this substitute at the highest lowest concentration highest sensitivity. So, if you just taken a substrate to a gardening you create and put the contact there you can play large registers, but normally not used. Whenever you need large register which way you use you actually create transistors in saturation region. And you have large amount of R can be created.

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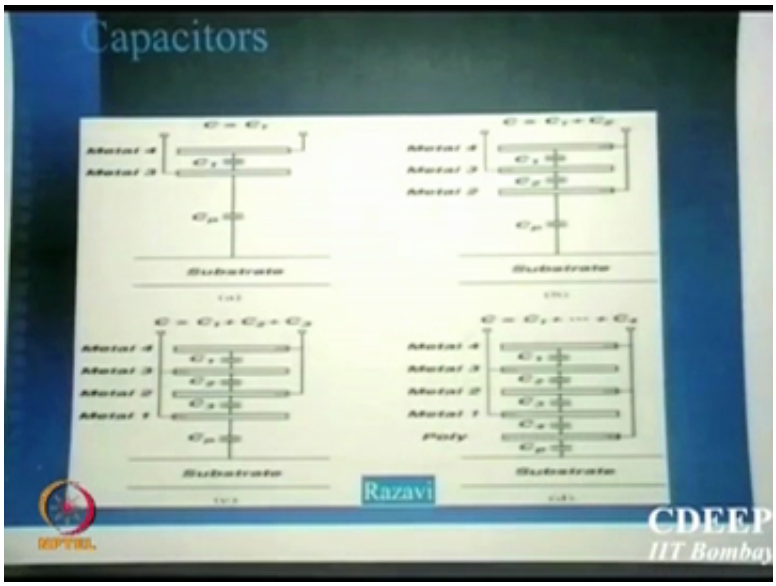

The last part of this circuit is capacitances. You can see from here a capacitance, I just told you last time maybe before I go, there are number of maybe we should use a fresh sheet.

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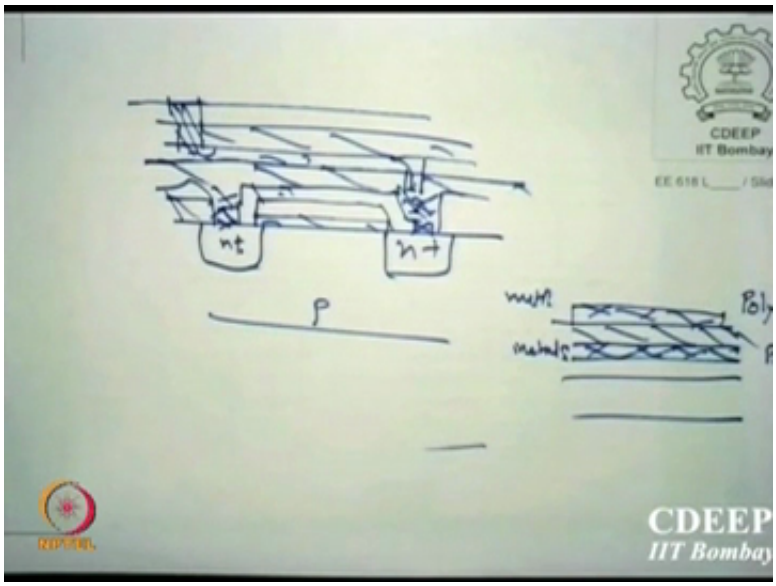

Let us say this is my first layer, I am making an n channel device. I open a contact, there is a gate here, there is a poly here, these are all oxides these are contacts, this is the first metal I took for source drain and gate of course, is in the vertically outside. So, I put another oxide on the top. Then if I want a contact with this, I open a window in this oxide, and run the metal from the top which then we will get contact to the low range. If I want the contact to this metal, I put another oxide on that and open a window here, sorry open a window here, where this next metal actually gets connected to the next metal. At no time this can directly be connected to the lower down, you must connect to the next nearest metal layer.

The cache is whenever you open a window here, there should not be another window below because the processes will done maybe inter merging somewhere. So, if you open a contact here open somewhere here the next contact on the next layer. All contacts should never match each other they should be at separated positions, but you still go down and connect is that, threes are called metal one, metal two, metal three, metal four, metal five, metal six, metal seven, and we are now going up to metal nine. Why we need large numbers because many of the processors are DSP in particular you need huge interconnect lines going from one place to the other.

So, our metal lines are similar we can go as many metals of course, there is an issue why not beyond nine, why not 100? So, the problems start that the total resistance for the

length of interconnect you go through his is. So, high that the voltage will drop there it said nothing will go down. So, there is a length minimum you can here have to make restrictive. So, in capacitors normally between two metal layers there is an insulator. So, there is a capacitor wherever you make two contact there will be a capacitance associated, but the where we actually do the capacitances in other ways is the following you have this process I have transistor but let say in the top first poly line has been created for the gate poly one. Of course all poly will be protected below by oxides then sorry this poly I should use this then there is another oxide layer on this poly I created and I put another poly here.

This is called poly two, it is called double poly process not all processes are double poly all flash processes flash roms are they all are double polys, but not all CMOS process are double poly, but analog CMOS processes are always double poly. So, extra money for that, so this is m sorry poly oxide poly. So, that is the most common capacitor used in analog designs or created in analog. If you do not have one there is another way of doing the same thing which I will show you instead of power it is poly this is called metal one and this is metal 2 or 3 or 4. So, restrict the idea of metal. So, you have a capacitor down which is called mi m capacitors, which are called mi m capacitors please remember once I use this line I must break it somewhere because otherwise there will be one line everywhere.

So, the area of a each has to be restricted to make a standard area of capacitance is that clear. So, restricted area will make standard epsilon a by d kind of thing. So, either mi m capacitors are used or poly if you have two poly process poly two to poly one is what is used often in our accessory most people have poly two. If they do not have then you use only mi m digital process will I have mi m because there are seven layers available or nine layers available. Now, there also it is you say that the capacitor should be closest to the point where the node capacitance is to be created; otherwise for us parasitic capacitance will actually shift our poles or zeros. So, in analog the position of capacitance to choose has to be which node you are actually looking at. So, closest to that you actually bring your capacitances.

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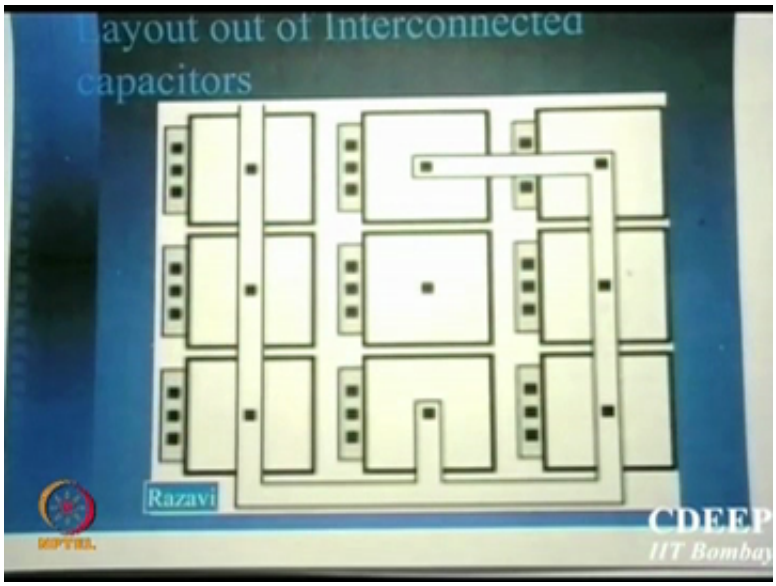

Instead of having a large capacitors you can actually create small capacitors of C 1, C 2 or C 1 and then connect in a fashion well do you see this capacitance is not connected to anywhere these are connected 6, 6, 2, so 8 capacitances if are connected to give 8. Let us say this has the capacitance of 1 or C this is 8 C is that clear. This is c and this all are in parallel made, so they are 8 C.

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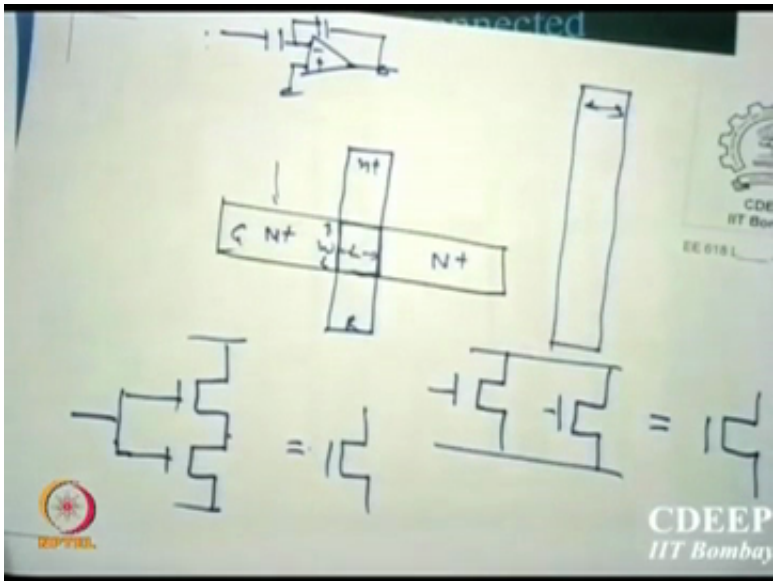

Where you such things are needed, in a switch cap circuits, you actually will use two such capacitances this will be eight times this. So, if you want to do this circuit use this

kind you make around. Now, all that I have not shown and even Razavi as not shown you need dummy everywhere all areas must be put dummies all around. So, eight of them and further eight of them around which as to keep them identical to each other, is that clear to you. So, this is something not shown, but please remember every this has I should have equal and dummies top bottom side everywhere. So, this is left, but then you should have here, here, at least poly as I said here, here in everywhere. This is essentially is called eight-to-one capacitance ratio, this circuit is creating eight-to-one capacitance ratio; eight from this, one from here. Change this combination and you can create any other ratio as well.

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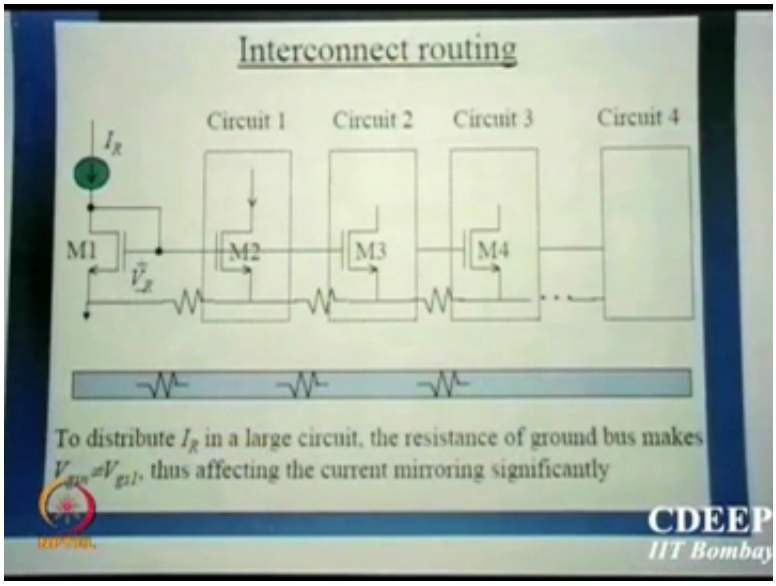

The last slide for the day as well as for this layout part is this interconnect routing. Now, this is an issue which is available it is equally troublesome in digital, but shown only for analog here. Let us say you have a current layer which is mirroring so many of them like you have know M 6, M 6, M 5 and so much even in op amps. Now, whatever way I use this line which is called the ground line or V ss line, one can see from here between here to here there has to be some metal line running and it does not have geo resistivity, it has a finite resistivity. So, equivalently saying from here to here, there is a resister; from here to here, there is a register. And if this is taken little longer, so if this potential will be different from this potential when the current is sinking through is that correct, these all sinks.

So, when all of them are sinking because of the mirrors, this sink will be different from this sink is that correct, because the available current to you is now the voltage drop is actually created across, this is called ground based resistance problem. In the case of digital, even if there is no mirror because of this we see what we call ground bounds the actual zero shifts to a higher potential. So, here noise margin on zero become worse sometimes even not there. So, it is called ground bounce. Similarly it comes from the power supply sides called power drop, so it comes down and you are upper noise margin also can go. So, these are issues which layout people.

So, what should I do for R to be minimized?

Student: (Refer Time: 62:50)

Increase the area. So, thickness of this metal analog grounds are there for at least eight times that of digital grounds, thickness wise at least eight times. So, if you see analog ground huge plates kind of grounds are provided, so that the R s are as small as possible is that clear, that is the trick, but what is the penalty area you lose, but at least survive otherwise you do not survive. So, that is the issue in the case of layouts.

Also now I will say you do not use single references, even if it does not matter if we run through as well as circuits things, but run another circuit ahead, another mirror and one ahead. So, break into number of references in case you feel too many such things you are running from one point. So, do not run from one point this is also done in digital keep buffering are actually putting V DD lines on four places. If you see if normal width chip there will be at least four V DD contact and four V SS contact then we need only one V DD and one V SS, but the distance now each of them may be different. So, at least four corners you create four V DDs same way four V SS this is done even in. So, [FL] you think you can tolerate keep as many and then repeat again that is extra area, but saving your life further.

So, these are you now clear to you that why I spend time in analog layout is the issue is that things can fail at the end just because you are not aware or you will lacks in layouts things where finally we will may show you zero. So, all analog designers must spend their fifty percent time after so called the simulation results have come in actually getting the best layout. Try any number of times extract and put it everywhere values for them and see layouts still works for you. Increase the ICMRS decrease the ICMRS, swing

their power supply 5 percent to 10 percent where keep seeing that everywhere circuit is all bounds it actually well. Increase temperature from minus 25 degree centigrade to 125 degree centigrade on whether all corners, it works then keep modifying as layouts till you find most of the corners are not, so that requires hell of an effort. Most of our student copy from the last year thesis because he must have seen somewhere and more than seen in the first. So, the worst things are going on last 10 years.

So this finishes much of the issues on layout there are many more things I can tell, but forget this. We will start with next Wednesday the last topic of this which is called oscillators. We are done lot of amplifiers at least see oscillators. Actually oscillators are not just the issue of which we are interested in we must do something called clearelse face look, face look locks , but I think in next three hours, four hours, I do not think I will be able to catch up with PLLS , but I at least tell you how PLLS works on Friday. So, on Wednesday, I may show you a V CH; on Friday, I may show you how PLL picks up why PLLS are essential with PCOs.