CMOS Analog VLSI Design
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Lecture - 25
Noise

This is what we did last time.

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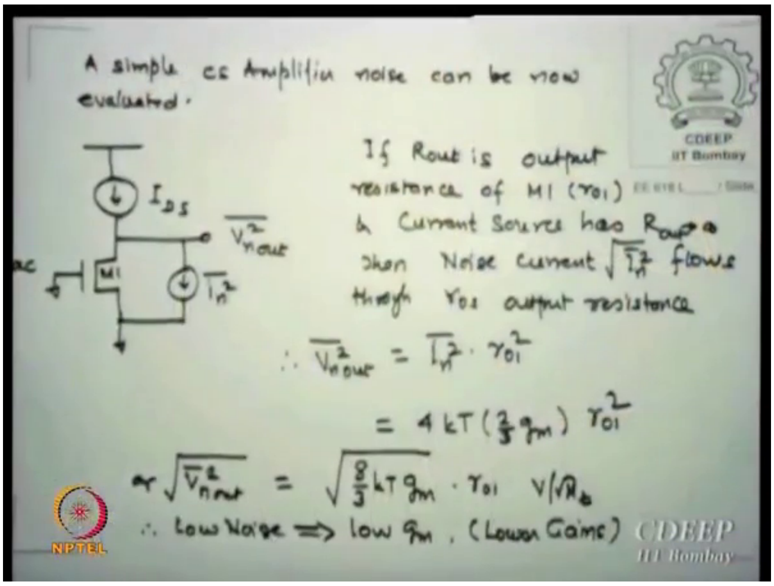

We were looking for a common source amplifier and we say if it is driven by a fixed current source biasing then for each transistor, there is a equivalent noise current source I n square and since this is I n square, the impedance seen at this node is the ro of this parallel of ro of this, but since I is the good current source with ro infinite. So, this only ro of this will appear.

So, we said is I n square time ro 1 square is the V out noise square term appear and we know this term we already figured it out this is for kt 2 third gm into r 1 square, this is what we calculated last time. Please remember, it has a unit of volt square per hertz or if you take under root of that as a noise voltage, then it is root volt per root hertz and many a time, this number may come in minus 9 or minus kind of things. So, it is normally expressed in nano volt per root hertz.

It is not necessarily values may be differing and so do not say; oh, it came in pico or it came in milli; it may come in even ohms; I mean in the volts. So, please do not take it, but generally noises of the order of nano volt per root hertz.

So, this is what we did last time. So, the noise here we assumed everywhere was essentially because of the randomness of the nature and we say it is thermal noise. So, we say it is, but as we discuss in the few first few slides there are other noise factors.

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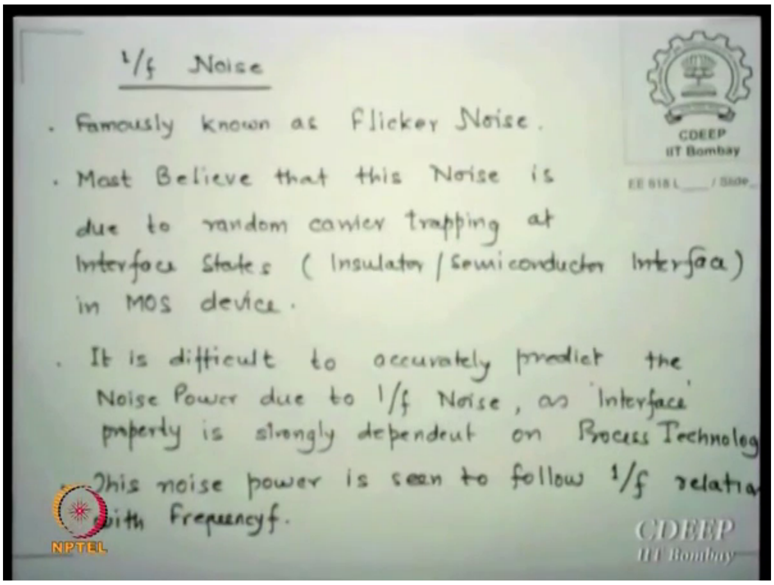

This was done last time, this is just to recapitulate where we were the; another noise of interest which you have to worry about is called 1 upon f noise; popularly known as flicker noise. Most believe that this noise is due to random carrier trapping at interface states this most word is very important because some others do not so; obviously, I had to say most many of them feel that this is good enough explanation to get whatever value one monitors ok.

So, this is one not a very absurd thinking, but there are many other devices where there are no interface states. So, then how do you say that if there are no interface states? So, why there is one upon f noise so; obviously, it is not the only reason, but in mos transistors probably interface is. So, strong between silicon and silicon dioxide or any insulator and substrate and the interface states are large numbers impact those who know something about devices. Now at least mos device course or mos technology could the typical order maybe order of 4 or 5 10 to the power 10 per centimeter square. This is the lowest one gets to at best; normally it may even go to 11 10 to power 11 per centimeter square. So, it is a very large numbers are seen actually and they may actually carrier trapping can occur because carriers are moving at the surface channel is at the interface in the silicon. So, tapping is very strong children.

Now, this noise because of this randomness in trapping one say there is a noise associated and this noise was said to be called I has shown a nature that it decreases with frequency and un linearly goes down. So, we said is one upon f noise.

Now, if you if you are noted down maybe I will move, this as usual we can model this as either voltage source or a current source whichever way you feel like you know V ir. So, whichever you wish you can always this or V into g is I either way is that move in general as I say we can.

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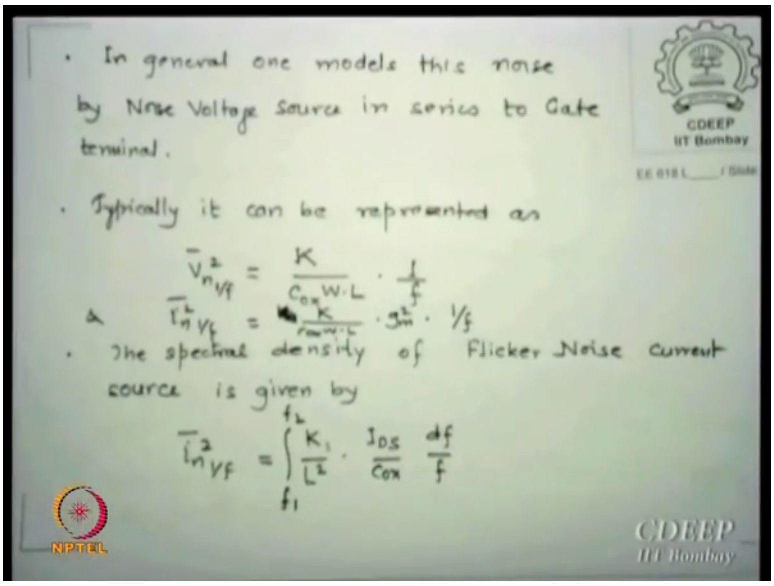

Noise voltage or noise currents; it can be monitored as 1 upon f noise voltage is k upon c off W by L into 1 by f and if you look at currents then k upon cox W into gm square by into 1 upon f. Kow k some kind of a technology constant related to a mos technology work with and therefore, different in different technology nodes cox is the oxide capacitance per unit area W is the width of the channel L is the length of the channel and one upon f is the f is the frequency.

And since for a given current biasing everything rest remains constant you can see the current noise source is proportional to one upon f; however, if you are looking for spectral density you must integrate it because that is always used for something. So, now, integrate on f 1 to f 2 df by f and since this gives you some df by. So, here is another way of expressing this which is I intentionally brought you can also represent it in a diff different form that was a voltage recover gm form this can be written in IDS form you know due to beta IDS is equal to gm square is that here.

So, adjust the terms then this k will not be same take some term in the k and then new constant can be given because that W will then cancel and L square will appear. So, this is how new expression can be derived why I am deriving, it will soon will be obvious to you.

So, now for a given IDS biasing one then can immediately evaluate instead of finding gm one more this is the current. So, we know what is the noise associated from this this is the method one uses often in actual designs. So, I just wanted to tell you that some books or some papers if you see they may be using this expression rather than these expression they are identical remember this case are not saying there some constants have been picked up there in k plus some into something new name has been given.

Now, if I integrate this term which is df by f term is only frequency term there.

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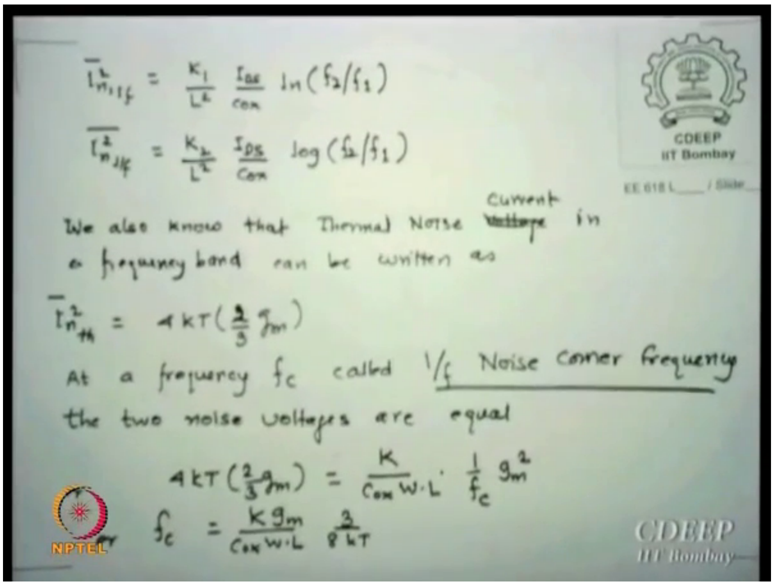

So, it is log f and therefore I can say it can be k 1 by L square IDS by Cos ln f 2 by f 1, if you look at take some more constant out of that what is the constant I am taking 2.303 also; if I took out, then k 2 by L square IDS by Cox log f 2 by f 1.

So, what are they trying to tell why; why this expression has been shown if you see the spectral density for this it shows essentially telling that the larger the bandwidth larger is the noise is that clear. So, that is something you have to understand that there is some relationship we are looking at noise with the bandwidth; is that clear?

So, when I am defining bandwidth for my amplifiers or my circuit please remember it also influences your noise voltages or at then we say signal to noise ratio may deteriorate this is something which; obviously, not known earlier, but now you can see that there is a dependency coming from here.

You will also know there is a thermal noise. So, if you really want to say that 2 noises are simultaneously occurring you can see this is constant there is no frequency term here. So, if you see this noise volt currents somewhere this value will become equal to the noise voltage due to current noise due to one upon f noise is that point clear one upon f noise is decreasing and let us say thermal noise is much it may be I will show a figure first and then come back.

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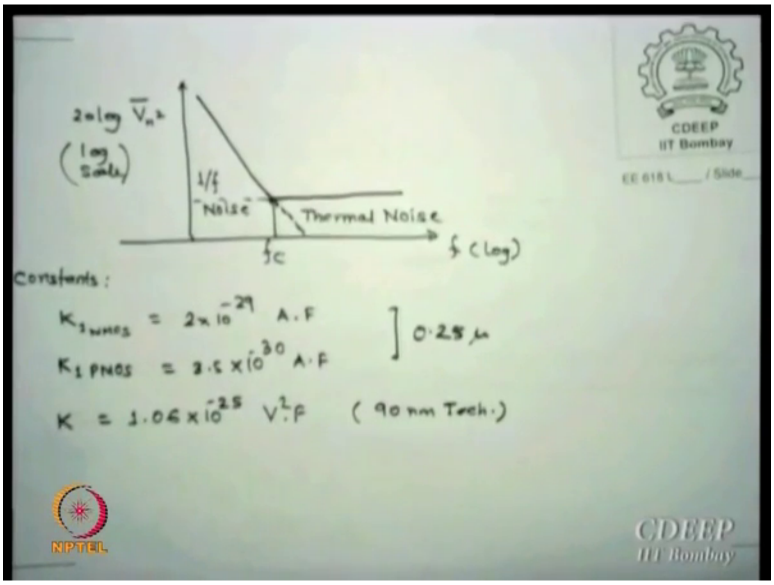

The one upon f noise starts decreasing as frequency increases thermal noise is you can always tell that this is essentially not here only it is like this, but it is constant.

So, above this value where the one upon f noise has same value as thermal noise with one upon f noise will continue to decrease and therefore, thermal noise will start dominating beyond this called corner frequency of noise which is I have seen at that frequency onward thermal noise will dominate below that 1 upon f noise may dominant is that clear to you.

So, this frequency is very relevant for us at what frequency we are operating will decide whether to use one of them somewhere here; both are equivalent terms and therefore, normally you may put 2 terms all the time if one is smaller the; it will take care the second term will mask the other anyway in numerical numbers.

So, for us we need not worry too much, but if you know jolly well you are working at these frequencies I mean one need not worry too much about one upon f noises, but that a priori; you should know for given technology node what is the fc for you to know fcs you need some constants to be known that is case. So, it has been found; for example, this is essentially for point 2 5 micron technology where are the k value which I got from the Razavi's book is essentially for 90 nanometer process.

So; obviously, one can see why this is different in different cases why I said because as technologies case interface properties are getting difficult or in some cases even better either way there are different technologies like if I put high k, I will be worst in that silicon dioxide I will be much better now actually, but as we scale down we may have to shift of nimoxide of nim oxynitride or zirconium oxide or as we are working lanthanum oxide or europium oxide very large numbers.

So, there as you scale down the case becoming you can see larger and larger what does that mean; that means, noise will become higher and higher as you scale down is that point clear. So, we worried started now as we went down below point one three or point one eight micron technologies, we figured out the first hit was over noise itself because it was just increasing and increasing as the frequent notes start going down.

You can also see the term L square in the denominator there is that clear. So, smaller the channel length you use larger is the noise you create is that clear to you. So, some issue has to be understood that why; now I am talking so much about it because you are already gone to twenty 2 nanometer process maybe soon sixteen will come and 11 may come and zero will come, but the point is that the noise will start then such a dominance that signal is not their only noise is there may happen.

So, let us see; what is the situation where this may occur or may not occur. So, elevation is one way of trying to reduce as long as we get signal to noise ratio higher its fair enough only noise increased then you have a worry is that correct or somehow you must try you some filtering has to be done such that somewhere this number can be controlled that is something we will do later.

So, is this constant values are varying you understood why they are different because at different nodes the interface states are not same and therefore, and the channel lengths are different so; obviously, the constants are and the total lines also is different and different notes.

So, as we now move towards this fc calculations we equate these 2 currents or noise voltages as per whatever it is this is noise voltage; I am now taking 4 kt to third gm is equal to this is square current only and then.

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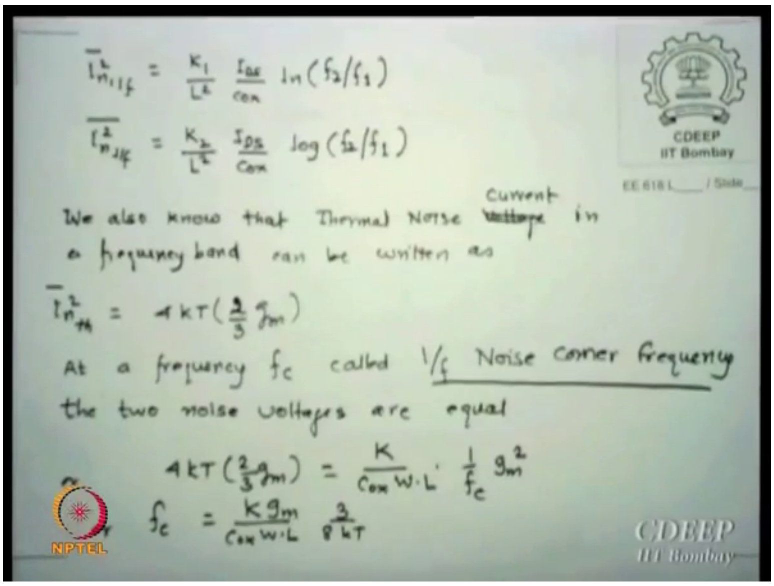

We get a term which gives me kgm fc put f is equal to fc and solve this equation what is it trying to say and again you can see it is function of W and L or the L square as the if you take IDS terms k. So, larger the k larger is fc is that clear. So, then one upon f noise will start dominating if your k is larger you can see smaller the channel length again the fcs are higher and higher.

So, now one upon f noise is now seeing even in rf circuits is that fine clear everyone asked us oh we are talking on gigahertz. So, what is the problem of one upon f you can see numbers is now going towards as many as gigahertz in some cases normally it will be order of hundred kilohertz to few megahertz fc is typically on the order of few kilohertz also it will be different for p channel and n channel device p channel will have lower fc n channel will have higher fcs this also an issue which you must appreciate.

The gm square term is coming because of the resistance which is coming resistance of a transistor is seen from the lower side is only one upon gm. So, resistance, but current is something by one upon gm is gm goes above 4 kt by r is the current source r is one upon gm and r square if you do it is gm square is that clear to you [FL] same method.

So, in nutshell about this one upon f or whatever it is i said already i repeat k one values are larger for nmos compared to pmos.

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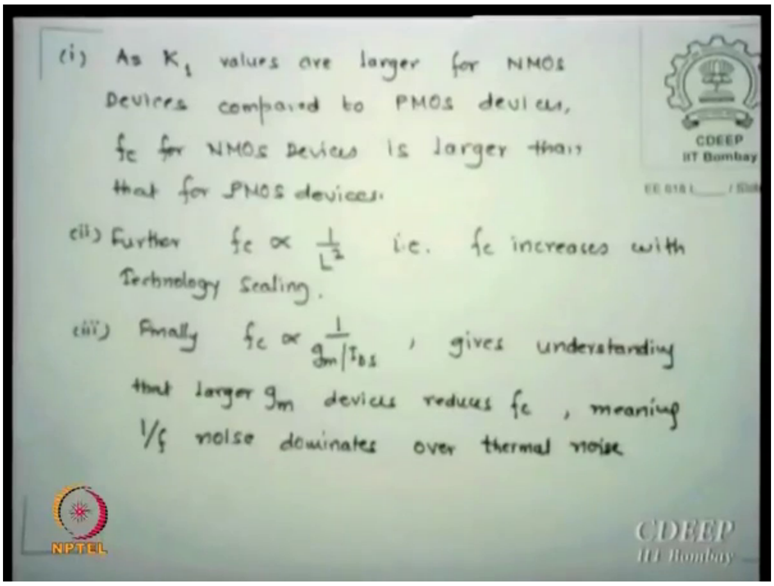

Fc further going to see larger than that of pmos; fc is a proportional to one upon L square fc increases with technology scaling finally, fc is also proportional to one upon gm by

IDS which gives some understanding that if you have a larger gm your fc goes down larger gm, but larger gm has other problem what is larger gm problem

Let us say I have hold gm larger then i proportional to will increase IDS because i will maintain gm by IDS larger IDS means what

Student: power dissipation

Power dissipation. So, the first hit I got is I; here I saw that; oh, I reduced power, but I hit on my power dissipation which was decided only by earlier by slew rate.

Student: Net current.

Net current available to you at the is for diff amps and it is also decided to some extent by the heat sinking possibility in the device. So, the power if somewhere was not connected to noise and now we realize that yeah power has some relationship with noise lower noise can be obtained if you have a larger power dissipation is that clear to you.

So, this is another feature which has now been added in analog design that the current you cannot just do something you like if you do something better for x, you can see you on to maintain bandwidth; let us see one upon rc if you increase see to keep this you will have to increase or decrease r by same amount or in our case is one upon gm. So, in some way you always find that you will hurt to the power immediately as soon as you go to the real device is that point clear to you. This is an issue which normally many books are not telling earlier because this was in 5 micron to one micron or point eight or even point one eight people thought this everything is manageable.

Now, this manageable is now becoming unmanageable. So, please remember the issues in 2010 or 12 are different from what 2000 we had. So, in my earlier first course in 98, I would not have told you anything this because I myself might not be aware of this, but as I started teaching ahead, I realized things are happening now much more stronger worries are started then what was happening in many years ago.

So, please you have a more problems than what we had when i started my master thesis work on ttl; ttl was a that time very interesting logic and it was very nice to work on ttls if I now say ttl, some may ask what is ttl. So, I hopefully it may not, but so, things are changed over the years.

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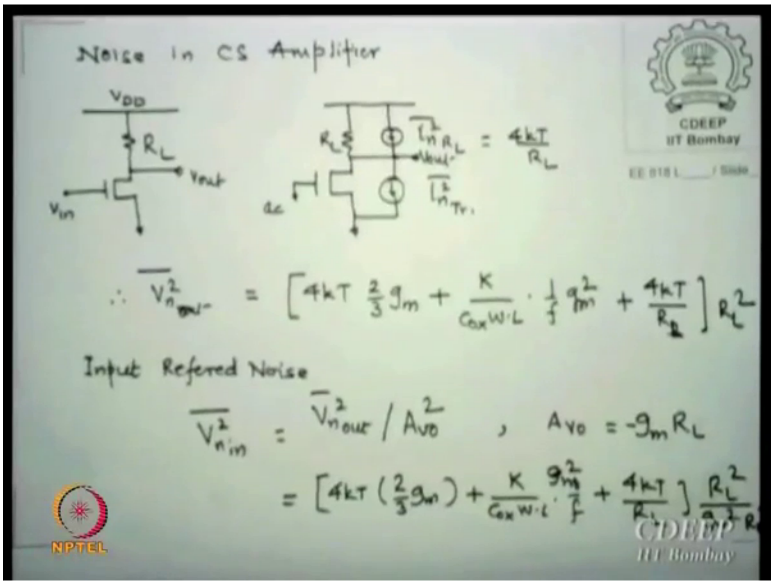

Coming back to quickly on this noise in amplifier, I will do quickly few cases. Let us say if I have a resistive RL as the load biasing is otherwise done then there will be 2 thermal, noise sources 2 sources across the 2 component one is due to the RL, the other is due to the transistor itself. So, to calculate the output voltage that is the noise output voltage what is the method we apply use super positions take one noise source find output take second noise source find output or to say sum them out and then actually figure it out.

So, for this we all know that this transistor has 4 kt 2 third gm this is what is this this is one upon f noise term and this term 4 kt by RL is RL term and multiplied by what is the load here RL; RL parallel ro is RL. So, r assuming RL is much smaller than ro. So, R L square this is i; i square please remember this is i squared multiplied by RL square. So, you can say i 1 square R 1 this i 2 square RL square is the net output voltage at the noise you will get substitute this.