CMOS Analog VLSI Design
Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture – 21
Operational Transconductance Amplifier

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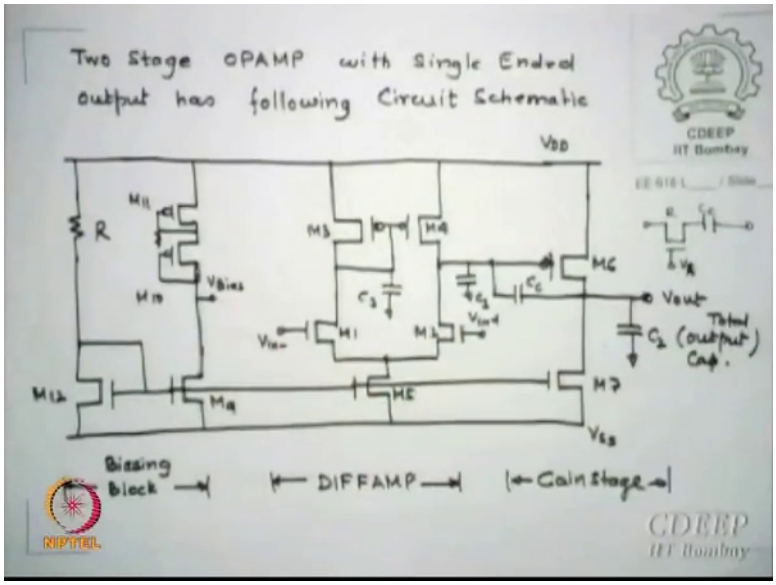

Last time this was the circuit which we designed, and there was a quick query last time that, when I will said Vgs 3 is equal to Vgs 4 is equal Vgs 6, and some people objected to that, actually it is not object I thought that now should know what I said here is one you can.

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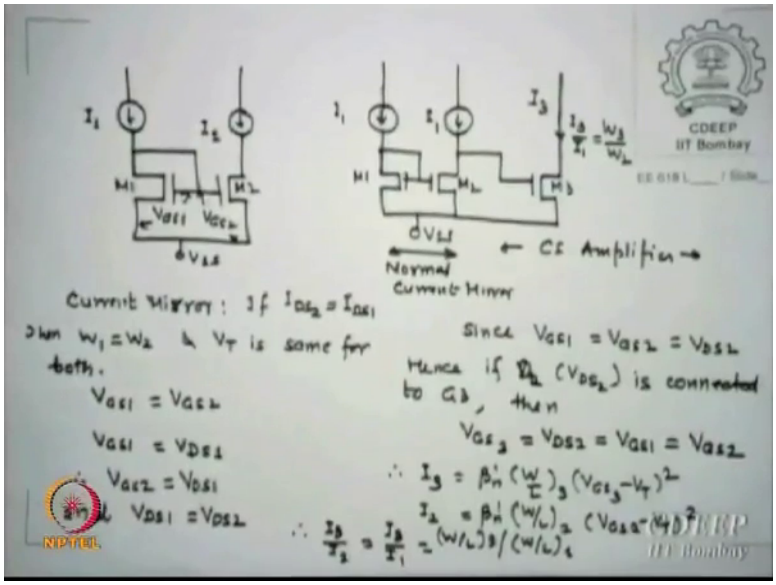

Now, look at it the way it is done this is specifically ready for you to show how it is done, just take a normal mirror, both W by L equal to each then Vgs one is Vgs 2, but since it is mirrored Vgs one is also Vds one therefore, this Vds 2 is also Vgs 2.

Now, having done so, we now look at this the structure which is same (Refer Time: 01:06) this is your M 6 or whatever number what is that transistor there, this is that M 6 this is the mirror, and it is drive driven from the output to the input of that common source amplifier. Just look at it if the currents are same Vgs is same, there is no other a Vds still will be different, but the currents are also same Ids is equal to beta by 2 Vds R square. So, that has to be same if the currents are same sizes, are same there is no other way it can be different.

So, since we say so, all this normal current mirror which is you can see there these transistor are also identical there as well as here, and the output of that is actually paid to the this is for M channel, but you can wait for P channel, now one can see from here this is Vgs one this is Vgs 2, and that is also equal to Vds 2 and this Vds 2 is nothing but Vgs 3 for this, is that correct? Since I 3 is the current which is beta dash by W by 3 Vgs 3 minus Vt square, and I 2 or I one which is same here is beta and W by 2 Vgs 2 minus, but these are equal, if these are equal then I 3 by I 2 is W by L 3 by the W by L this.

So, the way show this is also essentially one of the method of biasing a common source amplifier from the mirror, this is the very standard technique you should know it

[laugher], but I thought since we that they raise Issue. So, I thought I will prove myself that I am right. So, this you try yourself in case till it is not clear, but this is very in my opinion very simple, the OPAMP which will we looked into.

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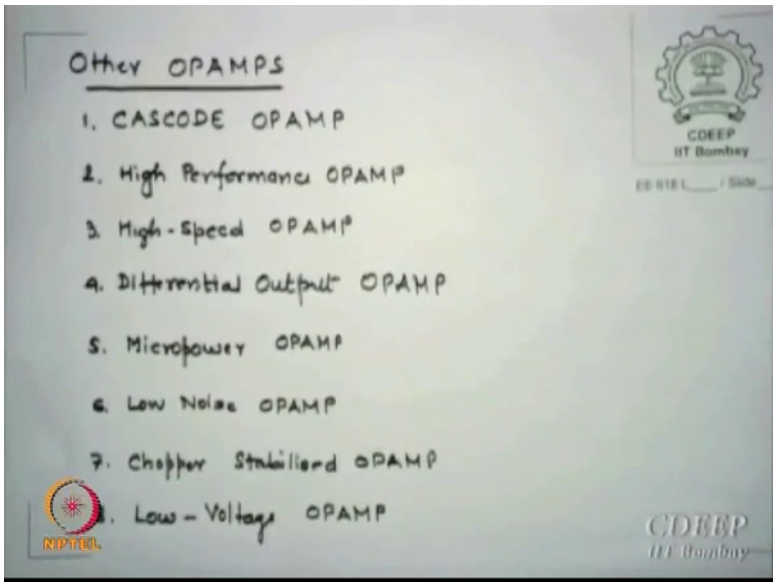

All these days what essentially a normal single ended 2 stage amplifier which we called OPAMPs.

There are other OPAMPs possible in the hardware implementations, one is cascode amplifier OPAMP, the other is called high performance this is essentially related to slew rates.

High speed OPAMP is related to the bandwidths, a differential output OPAMP 2 outputs which are differentiate to that is also a differential OPAMP, which probably we may do, not all of them, then there are amplifier OPAMPs which are called micropower very low power OPAMPs, then there are OPAMPs which are low noise OPAMPs very, very low noise we are trying to use very large signal to noise ratio there and maintaining low noise, and there are OPAMPs in power electronics particularly we use which are called chopper stabilized that low frequencies, and of course, there are OPAMPs which are at low voltage supply itself, may be 1.8 volt or point 6 volts.

So, there are number of OPAMPs in the literature, basic idea does not change, though for each case we will have to do something to achieve that specification is that clear. So,

look into books, there are all kinds of such OPAMPs are available, I have done the basic OPAMP to stay single ended amplifier, but they can be need not be single ended as we see earlier, it can be double ended as well, if first thing which probably may like to quickly do is the cascode, one of the major worry of the 2 stay single ended OPAMP was, you are worried about it is stability, because there was the second stage, and there was already a capacitor at the output of the first stage, and then we put cc mirror capacitor. So, that you can compensate to some extent, or put rzcc to actually compensate the non-dominant pole or null that.

But; that means, you are actually limiting something because once you start increasing cc, for your good compensation you have more worries, if you put rz higher then the 0 which is coming has to be very close to the non-dominant pole. So, adjusting the W by L for the transistor is not very straightforward as it looks. So, why after all your ultimate aim was to see large bandwidth and large gain and stability. So, if the second stage is removed them [laugher], it defined as a larger gain it has only one pole dominant pole, you can adjust the bandwidth and gain accordingly you can do that, and to improve the gain of an any diff amp stage or any amplifier stage, when technique who is know is to do cascoding.

G in Rout. So, increase Rout. So, let see if you look at this single stage cascode OPAMP, to improve stability Issues one possibility that we have a single stage OPAMP.

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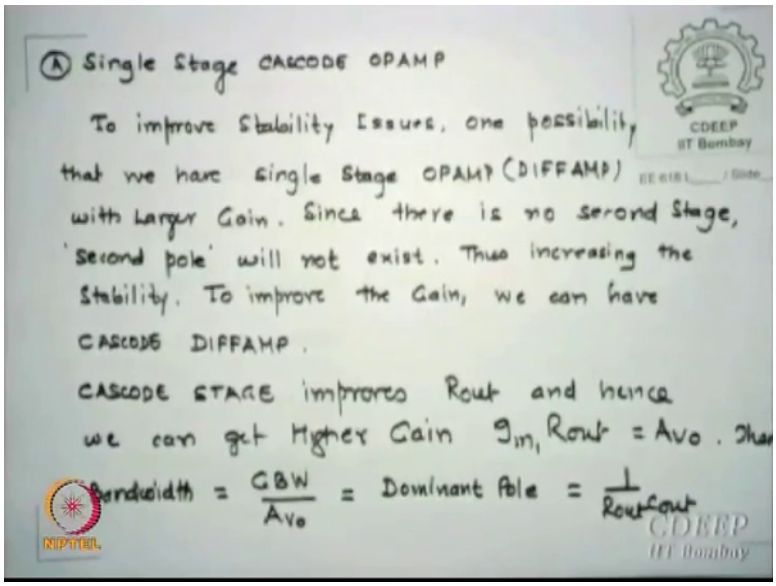

With larger gain, since there is no second stage second pole will not occurred, thus increasing stability to improve a gain, we can have cascode diff amp, and if you are look at it if Rout is larger GBW by Av 0 only dominant pole which is Rout by C out.

So, you have only 2 things to control, the W by ls of the 3 and 4 transistors, and W by ls of M 1 and M 2 transistors, and you can still increase of course, the bandwidth will not be very high, simply because if you are larger gain then you will use the bandwidth to some extent, but at least there is no Issue on stability, there is no second pole going on of course, there is one pole on 0 from the C 3, but that we are already evaluated because of cgs is far away. So, we do not careful that.

So, this was once not that we did, this we I am trying read which what we did finally, So, one possibility was we cascode the diff amp itself, is that everyone this statements I write is simply because I thought that if I say little fast, or something you can read at least you need not like every bit word by word, you should only think what I wrote in general, what I am trying to say that the method is that you can cascode a diff amp is that okay?

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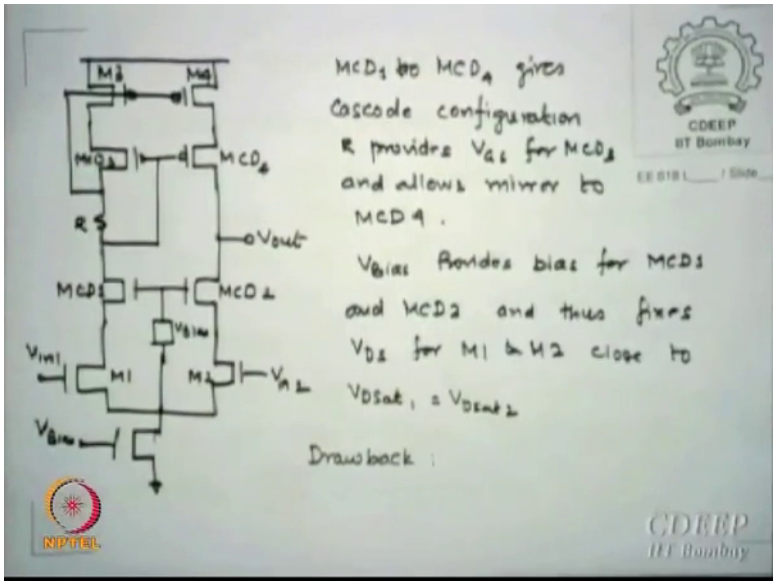

So, how do we do that, is it, here in a circuit which is cascode OPAMP or diff amp, I introduced MCD 1, MCD 2, MCD 3, MCD 4, 4 transistors, from the normal M 3 M 4 M 1 M 2 combination to make it cascode looking structure.

Now, there are few things you should know, actually I put I have connected something like this, but since you know it would have emerge with something I put it inside, this is still like mirroring, it from the gain I am going through the drain of this transistor b 3, now you can see from here what further I did there is a small resistor r, and from this MCD 320 I have put output here, we think why us this was done anyone. So, I want to bias these 2 transistors, I must provide a drop across it. So, essentially it is a v bias which I am going to create there, or and in current will be decided by M 1 M 3 any way. So, whatever rr draw there will actually decides the bias for it.

So, a trick of the trick just put small r, and this R value will decide when the transistor will be at least at the saturation or little better, the similar logic to cascode this I have put to un channel devices which is MCD one, and they are given a separate bias the bias. So, that these 2 transistor can recollect your OPAMP or cascode stage, we need a dc bias at the series transistor that bias I am creating.

Now, question is, from where this v bias will come? Externally how do I generate these v biases? So, that I can force these transistors in saturation, and still act as a series transistor 2 M 1 M 2, is that clear, this is what we are looking for, I will show you how we do we all draw the circuit, I am not going to design this these are circuits, we know the circuit analysis now well, you should be able to design yourself in case such a circuit is required, and basically you need not design manually right now once you know how to design OPAMP, basic design you can continue and put in cascode in in between.

Student: So, you can prefer second R 2 (Refer Time: 10:08).

it can be, but then 2 resistors are very bad to operate, because they will created RC time constant. So, avoid as much larger number of rs in your circuits, instead of R in one R mistake keep the other I will create out of what we are asking to a transistor. Which is what we are going to do you are not really wrong. What is the drawback of this circuit? As soon as I do cascode something goes wrong for me Vo swing.

But even input icm are goes down, because 2 Vgs drops is that clear. So, are icm are goes down and small, and smaller the ICMR means your linearity is very restricted, now which essentially means is for very low signals only you can probably employ this amplifiers. So, what you said we out is Vo max Vo min will also will be reduced, because of drops across 2 transistors, is that correct and that is one reason why you can actually

there is some other version of this look into the books, which is called folded cascode, which slightly improves ICMR compared to this, but essential still will be worse than the normal single ended OPAMPs.

So, this is the drawback. So, maybe I will write, reduced ICMR and Vo swing. So, this is the drawback, now I want to create this bias this where I chose it, because anywhere you need this the circuit which is shown in the book, is be enough to actually create any kind of such biases, which is given in not exactly this way, but bias go or to some extent even in Rezavis book, also there is some bipolar version of this is available in grain mayers book.

Actually, you can also try something, you can have bi CMOS you can one or few transistors can be converted to bipolars, and may have advantages and some disadvantages of course, with that. So, there are versions, I am just showing with the basic idea of cascodes, if I see you know this is creating a problem, bandwidth if I increase the gain bandwidth goes down drastically, they it will give gain higher because Rout is very high now, now the problem what I see is can I done use the 2 stage what we did earlier, but actually cascode the output stage, instead of the first stage the source common source amplifier I will cascode that amplifier.

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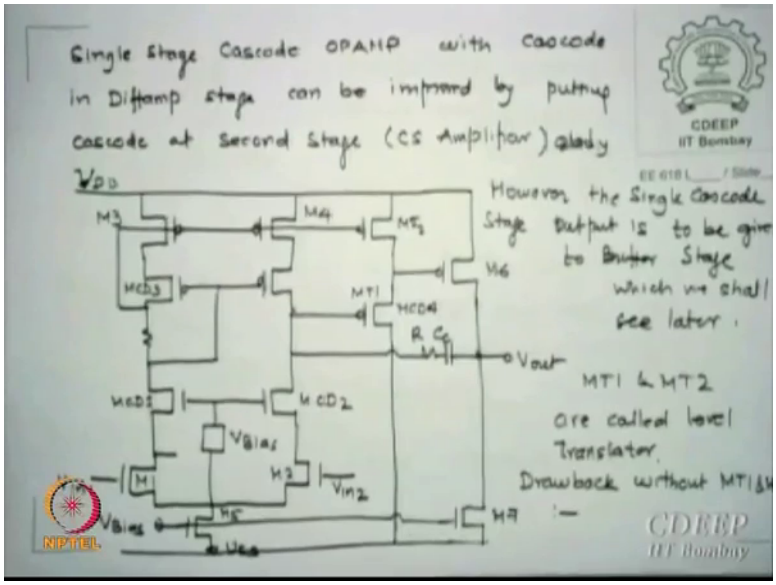

So, the second version of this which actually appeared is base cascode OPAMP, with cascode in diff amp stage can be improved by putting cascode at the second stage, but

now see the first one in which you can see from where this is your normal M 6 M 7 output stage, this is your cascode which we did, and to do this I have introduced 2 transistors Mt mc, what is called Mt 2 and MCD 4, these are names given in the books on a thing rate about, this is Mt 1 and Mt 2, sorry they should not have been change the name Mt 1 and Mt 2, please remember I can use this the advantage of can anything.

What is the purpose of Mt 1 and Mt 2? Because these M 6 and M 7 are going to decide your gain as well as the slew rates; so, I said okay they should not be connected to the output of the first stage, because they connect directly then they actually limited there.

So, we said if that is. So, I can have a lower translators from this voltage and this voltage, whose outputs then I can give it to M 6 and M 7, and if I do this I can have better this way, what is the problem with Mt 1 and Mt 2? If I put it there again the voltage swings will be now limited because actually we are reducing this values. So, actually reducing the how could seems, but slew rate could be slightly better which is independent of gm 1 Gm 2 currents coming from here. So, this additional drive capability, which you create separately can do wonders wherever you are ready to have lower output swings.

These are tricks what people do alternatively to this as well, it just take output stage and cascode it, here is that circuit this is given in the bias book please.

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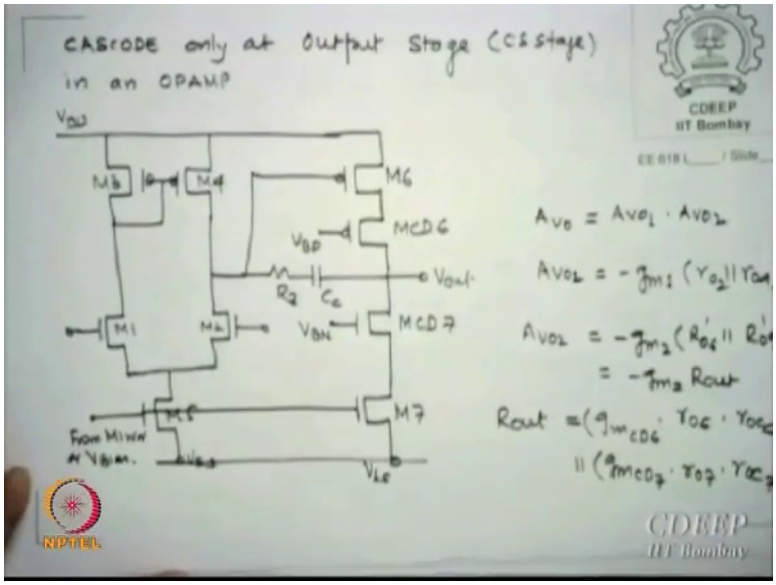

Look at it again

Student: (Refer Time: 15:07).

This is essentially required for your slew rate requirement then these currents which are coming from M 6 and M 7 are not connected from this output, these are driven by Mt 1 and Mt one. So, I am changing the bias for this independently. So, the currents which otherwise will I have got limited because of the gain which come from the first stage, is now broken by me, I said I will always separate voltage requirement M 6, and shrinkage of course, base RC has to be because the charge has to be from this side. So, the output has to be RC from there.

I whenever M 6 current is calculated, the output of this stage goes to input of the M 6, forget about this part this output would have gone to M 6; that means, the whatever it is currents coming here, will I am gain I want this current will be decided from this side, what is the input to Vgs is coming from there they are putting the translator, I have grouped that change I growth the change I have independent controller bias to this, now that Vgs 6 is not equal to the earlier one, I am now controlling through these 2 devices my bias for the M 6 so; that means, I can change the current here to require output load current requirements I can change without changing anything here is that clear.

Otherwise that will decide what current I can push to the output, the alternate way as I said, is to put a buffer at the output that is the common sense amplifier, this is your normal this all that I did is put one P channel and one in channel device in series to M 6 and M 7, and now I know once I do this Ro of this, and Ro of this could be boosted. So, Ro parallel is even boosted and therefore, one can see the gain will be larger, because Rout it will be Gm times Rout of the first stage. So now, it is cascode stage, the gain is now boosted by me is that correct gain is boosted by me.

But what is the problem I will create, the bandwidth will proportionately go down, because now the second pole has to be re; that means, null in as well as this method has to be found. So, that the bandwidth is not that much reduced, should then increase cc too much also do not increase rz so much, because if rz is together 0 will go, too much on the laptop it will not nullify the non-dominant pole, say when has to adjust rz cc value. So, that reasonable bandwidth and higher gains are, please take the point what did we say in

the case of gain bandwidth if broke that change we broke in cascodes. So, that word we have trying to use here by putting cascode at the last stage.

However, all these statements I am making I am telling as a 2-stable circuit which I am keep showing you is an OPAMP. In fact, OPAMP is this is not a real OPAMP, any OPAMP you used need to have an final output to be driven by something else, because this is not able to draw larger currents.

So, the load which Vout is going to see, may not be very small it may be very, very large comparatively, very large means it may not be larger than Rout or something, but at least it will be sufficiently large, for a large output loads what do I mean, b should provide larger currents, but these currents are provided by this stage as well as the rz cc combination I am going to Gms are decided from there ratios, which means I am not able to really drive a larger load using 2 stage OPAMPs.

then this word OPAMP therefore, should be slightly with a use with a pinch of soil, because this is how we started with either probably we keep telling it, but we said actually this does not drive the external group, it me ay give a good slew rate here, but at the output you need larger currents, their sizes how much we call 40,50,60 I want larger current means 100 200 W bias, if I put I can use larger currents, is that correct; that means, followed by this, there has to be a another stage which is called the buffer stage, and unless there is a buffer stage we should not really call that as a OPAMP.

Why I am insisting on this, because if there will be a OPAMP without a buffer stage and little modifications I will do that, that block is essential called OTA operational transconductance amplifier, OTA with a buffer is essentially a OPAMP, will come to a did soon is that point clear. So, 2 stage OPAMP is essentially claim out to be a OTA whereas, when I put a buffer out there, I actually called it as operational amplifier. So, is that point clear. So, the output stage could be what kind, it can be a class of amplifier, can be a class ab amplifier, or it can be class b amplifier, that is called push pull, which one you will prefer what is the problem in push pull anyone remembers second year.

Student: (Refer Time: 20:49).

Crossover distortion or dead zones, the 2 device may not switch over at the same points. So, there is the dead zone appearing at the inputs.

now this Issues so, we will avoid b classily as a limited gain. So, you do not know class a. So, I want class ab operation. So, what we say for a while it operates in b, and for a short time it operates in a. So, we call that as class ab amplifier, is that point clear of my worries are that I want to next stage, which should be able to provide huge currents for the output capacitances, but huge currents I can only get if there are large W by ls for these transistors.

But large W by ls means they are decided by the gains from this side, you all know control on that the W by ls you shown you remember, Gm 6 and Gm 1 by related because of the stability Issue which I create should be greater than 10 or something.

So, that ratio which I could not d1 play too much forces with the thing, I must have another stage out and that is called the buffer stage, and buffers are normally ab are in some cases even beta e, is that the Issue is I clear to you.

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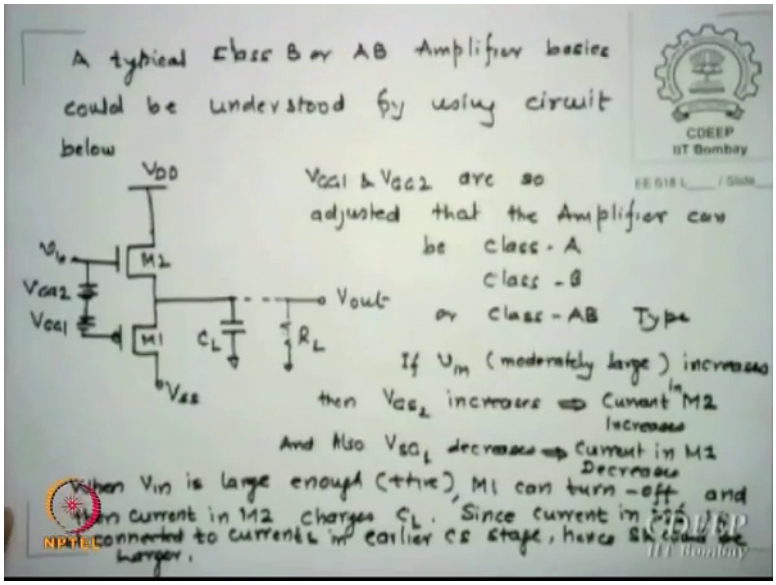

Just for those who have for gotten their second years this is something slide I think I should show quickly, a class b or ab amplifier basics could be understood by using a circuit shown below, you are a M 1 M 2 transistor amplifier and M 2 receives of course, this is the N channel driven it could be other way, it is nothing very serious you can have P drives and load and right P load.

what we do in principle is to bias M 1 M 2 by 2 bias power supplies, which is called Vgg 1 Vgg 2 and they actual circuit will say how do we create this Vgg 1 and Vgg 2, now you can see from here the way it is operates, depending on these 2 values I can make M 1 M 2 either in working in such a way, both working a class a both then plus N v in minus goes through, I can have a class b in which Vn positive either goes to or negative goes through, that is class b and in one third case partly M 1 and M 2 independent operates and somewhere both together operates, this was required for output of the second stage will be a higher voltage swing, Vout max you have created Vout my max minus Vout in, you have output swing large enough is that clear.

Please remember the gain stage you are going through, Vout is sufficiently high, now when this Vout or for this transistor which is going to be my Vinif that is moderately large, one can see from here if this increases positive this Vgs increases is that clear, but since the bias is kept like this, equivalently saying this decreases, total bias is same if you increase that one the other one proportionally goes down. So, current in M 2 will increase and current in M 1 will actually decrease.

Now this if I keep increasing the vn, there may be possibility that this voltage may not be as much as Vt requirement. So, M 1 may shut off and all the current may only pass through M 2, we increase these larger and larger this may switch off and this may become only driving, the converse is true if Vn is minus at certain weightage this M 2 may shut off, and fully M 1 will operate, the in between these 2 values with M 1 and M 2 will operate and therefore, this and the those cases when both operates will say devices is an in or say amplifier is an ab class amplifier of ab class is that clear.

Now, please remember, says the current in M 2 or current in M those this charges the capaci this is of this charges the capacitor, when this is of this discharges the capacitor essentially this is like an inverter driven system, and this essentially meaning that if I want this capacitor to be charged fast, I must put larger sizes of M 1 and M 2, except for a short time and both along then the huge power will actually consumed, otherwise only dynamic power will be (Refer Time: 25:54) is that clear to you. This is equivalent taken from inverter side that is like an a inverter system, in which I can decide dynamic loading dynamic charging discharging rather than static charging.

Now, this please remember Sr should not be used correctly here, because you say actually I am saying the output capacitor charging is also slew rate we have dv 0 by dt at that point, this Vm is about 2 stage amplifiers output, which is going to be the input for the buffer stage, a how much will be voltage swings for this, when this is of Vdd minus 1 Vt, a Vdd said will be as close to at that point is Vt. So, Vdd minus Vt and how much is there Vss plus Vtp. So, one can see the swings this is now very Vts are much smaller values. So, the output swing is also large enough in this kind of class a ab or b amplifiers.

So, one of the requirement was faster charging, and larger why larger because you are putting larger inputs, and you want all of it to possibly go out, otherwise what is it will start going, the distortions and more major destruction you will see later is the third harmonic distortion, because non-linearity starts a 0 plus a 1 x with a 1 x square into x cube, you expand this series and then find which ones omega 1 plus minus 3, is going which means going to hurt the most for us. So, if then point clear.

So, all that now I have to go in real life is, to generate Vgg 1 and Vgg 2 by they shows in the principally shown, that if I generate this depending on the v in values which I am going to get, I must choose this values this properly. So, that either this or this is all most times or for a short time both will be on for you, that is not a good area because then the gain actually is falling currents are actually partly taken here and partly taken here, is that clear which we do not want because; that means, all of it is not made available to the capacitor, that case should be for a shorter time this happens even in a CMOS inverter, this call short circuit currents by which force you P channel N channel turns on both simult for a while.

When input changes from input output I mean the 0 to one, when transit it does change the output like that same gain was played only difference between this and next is, what I like to create this Vgg 1 Vgg 2 such that this transistor amplifier can become class ab.

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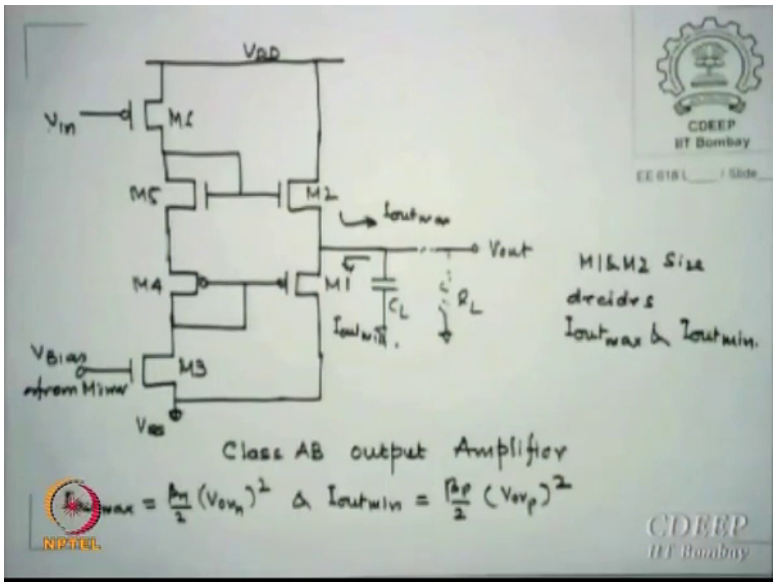

Here is a very simple circuit which can do this job for you, these M 1 M 2 they are not same as in the diff amp, I mean 2 stage amplifier these are just put M 1 M 2 M 3 M 4 M 6 here.

So, what is actually an amplifier M 1 M 2 is actually forming your class b amplifier, is that clear, the one which I just now showed these are the 2 transistors which are actually at this output is the capacitance, whatever this circuit is going to do is provide, Vgg 1 and Vgg 2 it is called floating biases it is called floating biases, this there is a transistor M 6 M 5 M 4 M 3 in series, and they are mirror formations here, this M 3 is receiving current or biasing from the mirror side, which side the M 5 M 8 whatever the large diff amp there is an extended that, or you can also put ab bias from this circuit which I have created v bias also in my bias circuit. So, I can either pick up that, or mirror the current from whichever current mirror I have to push this. So, I can decide current in N 3 or videos of this transistor.

So, what does it do this is my input. So, this is whatever this is the amplifier kind of situation, you should driven by this transistor this acts like a load for this. So, this is my output, which is going to be the input for M 2, from the lower side when this when is opposite, this is the maximum weightage than appears here in the negative this minus this. So, this actually drives M one.

Now, the trick here is the maximum current which is decided by M 1 M 2, whatever we want is b time Vn square and beta P Vop square. So, if I have adjust my W by ls of these 2, I can decide and if I know my Vop and Von, then I will be able to decide how much maximum current I can provide cl to charge and how much I can create, generally I will have I just one same because the time taken to charge should be time taken to discharge, but it need not be every time, because many a times once the capacitor charge the next stage requires some time for at further, is that point clear this this output will go to some other stage, that has some response time.

So, in between discharge if input goes down, I have sufficient time for discharge it please remember there are tricks in the game because once charged the output is now taking time for the next stage to operate, when it is switch on this it does not matter because still can be delayed, because that a still has not completed operation is that correct so many a times sizing is done.

So, that this time may not be same as this time, but as I designed you always try to keep equals. So, that this Issue need not coming to mind, how much is that clear. So, that is the method of creation of an output stage of a which is class ab amplifier, and this class ab amplifier is always the last stage of any OPAMP is that clear, last stage of any OPAMP, first stage is single ended diff amp, second is gain stage, and third is a buffer stage, is that please remember buffer gains are not important, what is important is currents it can give you as much of this.

So, what should be sizes this betas, should be large enough. So, that Iout match and Iout mean in R sufficiently large for this capacitor to charge and discharge in a given time what you want is that clear. So, that is something and now since it is not connected with the last 2 stages, this is independently driven by me to any external load I am in connected to, is that clear this is how OPAMP normally works, to all this time when I was saying OPAMP the real OPAMP will have additional circuitry at this kind.

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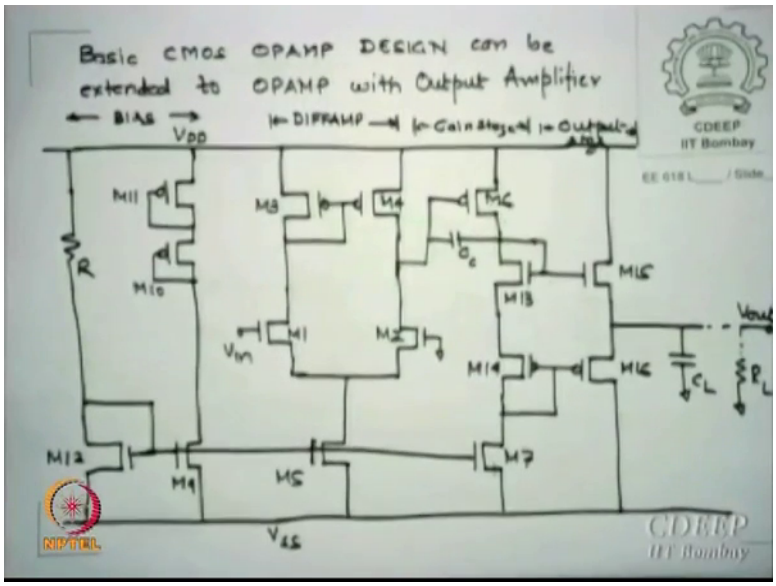

And if I put this here, this is what essentially an OPAMP will look like. So, you can draw this this is our final OPAMP which almost every circuit in the chip you have is this kind.

I forgot maybe I can now put r, R will be a of course, replaced a transistor whose bias can be picked up from any of these, even this R can be replaced by what, a few channel diode connected is that correct, the R can be replaced by P channel diode connected device, what why we do not want to put R everywhere, because the area it takes is very high this will be around 350 k 200 k 4000k; that means, mega ohms sometimes, and that takes huge area on chip.

However normally R has one advantage which this has a positive temperature coefficient this has a negative. So, net Tcf could be minimize, if I put actual rbi. So, for that purposes is sometimes instead of diode you actually put a r, is that clear this fact has to be remember normal resistance have positive temperature the other say. So, we want to reduce to less than thousand parts per million per degree centigrade, and that is the way people probably perforates at times, is that clear to you this is my final output stage, now this last you know something I have to draw just check the last part cl parallel to something I put.

This is our diff amp this is the first part is bias, this part is a diff amp stage, this part is essentially a signal gains cascode relatively cascode kind this stage, but essentially it is screen Vgg 1 Vgg 2 if I has this M 15 and M 16 which is your output amplifier or buffer

stage. So, how do we design that refers design diff amp, based on that we designed gain stage based on that we designed what is the buffer stage, please do not go the other way and this of course, can be independently designed and can actually we kept ready for every one of you, which may be a common because this line can push anywhere, and you can observe W by L ratios to get what the new currents you want, this why I intentionally put a rl there since M 5 for M m 15 and M 16 are being too dry with a large currents available.

So, even if you have a resistive load there, it can still create Vout, by ir drops is that clear, in the case of you do not have these and you have dying from there and the currents available to you are. So, small that ir may not reach larger v 0 values, that point clear this is an Issue which is submitting this the OPAMP from and oti which I am going to come, now is that clear is that point clear if this currents are not large enough, rl cannot reach to go match a main values, and thereforr OPAMPs can drive with resistive loads and capacitive loads, is that correct that is the major thing which we are trying to say here, a OPAMP with a buffer stage which is always called OPAMP, then can drive any kind of loads is that clear that is the strength of an OPAMP.

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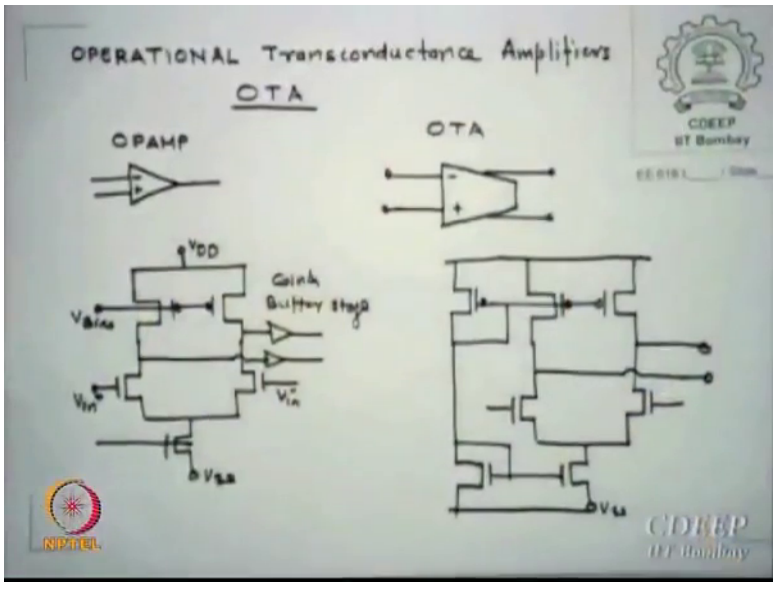

So now, we after all this OPAMP word we slightly modify OPAMP word with a new device or new amplifier, which we call operational transconductance amplifier OTA, in naturally what I say is if you buffer it a diff amp then it is called OPAMP, and if you do

not then it is called OTA. Is that correct the actual OTA is not that simply, or not that clear I shows the actual circuit which we use.

But this is essentially difference between OTA and OPAMP, is an OPAMP without a buffer stage is like a OTA, please take it the actual OTA symbols with therefore, separated from OPAMP, you can see we cut it partly here make a this quadrilateral kind of thing, and it can have both outputs normally OPAMPs are generally single ended outputs, is that clear OPAMPs are generally single ended outputs.

There are separate OPAMPs which are called differential OPAMPs. So, there will be 2 outputs, but then I will create those OPAMPs out off an OTA itself, because they anyway I have 2 such outputs possible there, is that clear it is not necessarily to use both, but I have access to both possibility this, but in real OTA I will do is I will have only one output, and I have that is what the major OTA chips are available, is the difference clear this is same diff amp same diff amp if it is buffer stage gain stage buffer stage then you say it is intentionally I did not put signal ended, you can have separate bias and can use source current source the instead of diode connected loads.

The loads could be either of them, even here I can have bias or have a mirror, please remember these are all your think you can decide any time. So, had not shown you that, there are 2 symbols and there are 2 possibilities let me give a table which actually separates OTA from OPAMP, is that everyone note down shown this figure is trivial, but still diff amp square plus minus plus minus terminal. So, do you get the where do you think therefore, OTAs can be used because there are no buffer stages there, it can only drive capacity loads, it can not drive resistive loads that is the major difference between OPAMP and an OTA.

But you can always convert an OTA into a OPAMP will do an example, I will make an amplifier using an OTA, and I will also make an amplifier like normal triangle basically resistance that I will show you with OTA also I can get the gain, same as what I did from OPAMP provided something happens that provided is what it differs between OPAMP and OTA.

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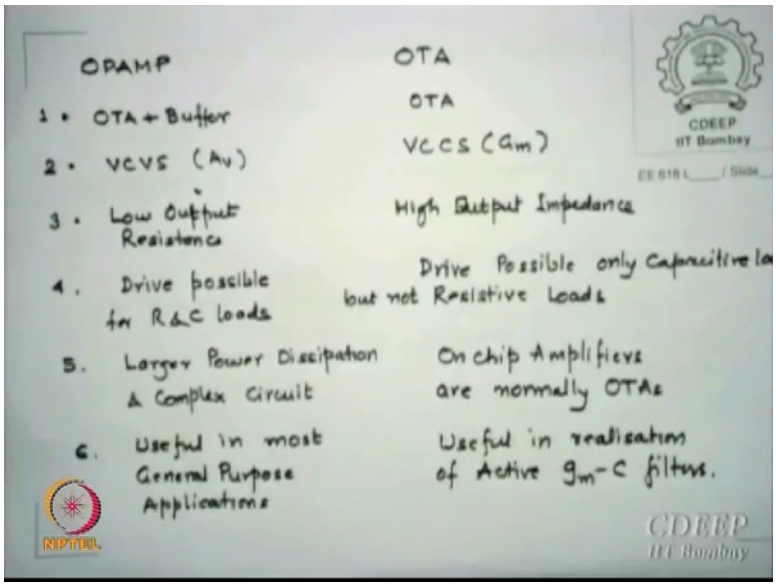

Table which is relevant for you OPAMP versus OTA are OPAMP an OTA whichever you look at it, a typical OPAMP is OTA plus buffer therefore, OTA does not have a buffer the second most important point all OPAMPs are voltage-controlled voltage source VCVS, all OTA the voltage controlled current source, VCCS. So, what will be the output of a OPAMP.

V 0 by v in. So, a v voltage gain, what will be the output of a OTA current is the output and input is the voltage. So, it is transconductance therefore, it is called transconductance amplifier, is that clear, another thing which is which is very different between OTA and this, for a diff amp stage what all the loads are used, diode connected is that clear. So, what is then output node resistance at the diff amp, Vo one of Vo 2 very small Gm 1 upon Gm is that correct, since these are 1 upon Gm kinds of outputs come, these are called low impedance or low resistive nodes. So, in OPAMP most nodes are low resistive nodes.

Is that correct, where as we shall see later OTA is the output nodes are actually very high resistive loads or very high impedance nodes, and therefore, are easy to charge a capacitor, is that clear that is the reason can drive all loads, OPAMPs can drive all loads, both are C and RC the only possible capacitive load and certainly not possible to drive resistive loads for OTA, OTA does not drive resistive loads because their currents are smaller comparatively, they are no large sized transistors there at the output. So, can not

drive larger currents and therefore, R is very you got the point why ir is a v 0, if I is small that ir will never reach the reo max value which you are looking for the next is.

So, the all OPAMPs generally I complex we are seen how much hardware I did, and they required large power dissipations it maintain your Gms and there are so many vertical paths. So, they are large power dissipation circuits, comparatively the OTA s are low power comparatively, and almost on chip. So, called amplifiers which you use on chip any how chip you see, it in a OTA and not in OPAMP, this is an interesting part there since OPAMP can have any load it can have larger gains, it can have any bandwidth bias cascode, you can do many tricks there high performance high speed they are used in all kinds of applications. So, they are called general purpose applications, right from instrumentation to communication, everywhere a power electron you can drive everywhere.

Whereas these are only generally used in filters which is gnc continuous active filters, these are the major diff amp, not there they cannot be amplifications voltage amplification is also possible, but this is much higher than what I can get through this is that clear. So, I would prefer to use OTAs, whenever I need to create larger Gms larger Gms and not larger Av 0s is that clear that Issue clear.

So, OTAs are of it is own class, they all most say OTA plus buffer is not that trivial as I make it better show a circuit later, the actual OTA is slightly modified version of what this statement as if gives.

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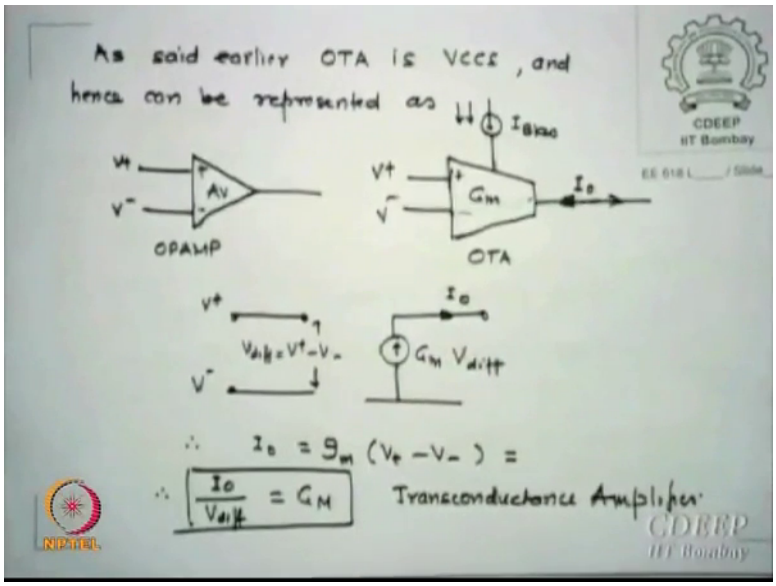

I said earlier OTAs is a VCCS device as shown here. So, what does that mean the symbol which I showed you here.

It actually receives a bias current I bias for input signals of v plus v minus or v in one v in 2 whichever we look at it, and it gives me an output current of I 0, and then I am interested to know I 0 upon v plus minus v in, or we delta vid or vid whatever you write, and that is called the transconductance capital Gm. Why it is called capital Gm? Because it is from the output to the input where in the small Gms as the part of this circuit, if I see equivalence circuit of this, you can see from here this is my v difference, this is Gm time v difference is what does the p, this is equivalent circuit of this. So, I 0 is Gm times v plus minus Vm capital Gm you can make. So, I 0 it make a capital Gm.

So, I 0 upon v difference is transconductace and since it is a higher. So, if I make I 0 higher than the v difference for which and finding that, then Gms are higher and we say it is a good transconductance amplifier. So, what should I do therefore, Gm should be improved is that correct, a good transconductance amplifier make large Gms. So, of course, there will be we are we will not calculate, but maybe you think for it or someone lastly maybe I will put it on the web, they are bandwidth tissues there are nicce Issues with OTA and OPAMPs, either v or maybe I put some words on that on my webpage. So, there you can see, why OTAs are not all that great as people think, but in some cases, they are the best speech device to operate is that okay.

This is only equivalent part of that. So, let us draw a actual OTA and see how much it differs, that is the real-life op OTA implemented on a chip the circuit diagram is taken from that. So, you can and this is taken from boys and bakers book, you can I have keep telling you day one if you really want to learn the real life analog designs, do look at boys and baker because, baker being the chief scientist in all over world he has been actually fabricating the newer step of analog blocks.

And because of that the data of course, he gave a old to you that is, but the numbers which he is giving is essentially tested chip, Rezavi extraordinary and good theory, but it never gives this numbers which problem we get actually on chip, he may put a many thing ideally, baker does not do that he knows exactly.

What is the real chip will give you. So, his values of sometimes very hard looks to you, but they are essentially what he has obtained during designs during realizations. So, please stop looking though that book, because it gives the real life. So, it is old technologies since not modified it is new book they are modified the old book has still 5 microns, does not matter theory equally important.

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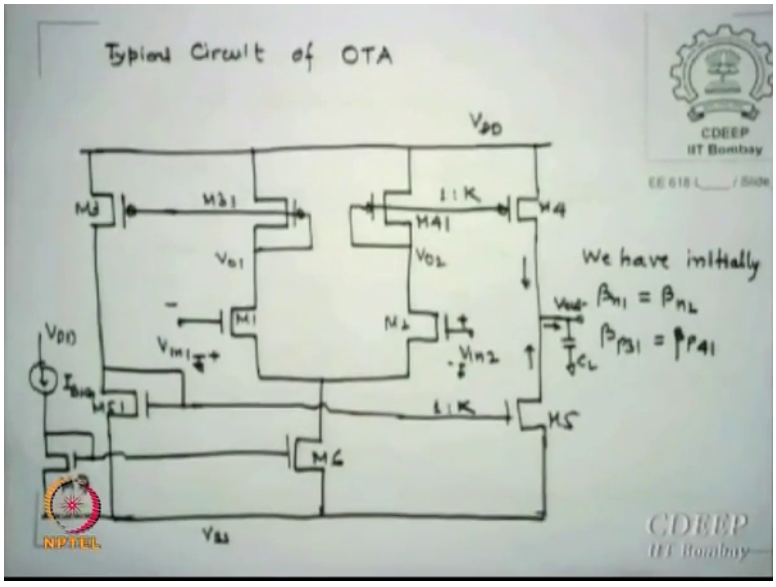

So, typical OTAs deadline is shown here this is a diff amp this is double ended it is that correct.

Student: Yes.

It is double ended book output connected. So, we have normally show from here, we have shown from here, this is same point. So, that is the way people are you know differ in right we showing figures, okay these are 2 diode connected, but not measured is that correct, they may be measured some other reasons, but they are right now not connected like this to create a single ended output, it is a 2 different diode connected loads, on your right if you see the output of this stage diff amp, which is taken from here or here they are same is given to M 4, which is like your M 6 in the OPAMP stage gain stage please remember we are not looking for what in the case of OTA voltage get we are not interested in voltage gain what are we interested in.

Gm means currents. So, we will see what currents M 4 volt drive, on your this side of load they have a transistor which is M 3 another P channel transistor, which is receiving output from Vo one, be a one is giving input to the M 3, these numbers are also taken from boys book, I mean you can put any names, but this is what I said, diff amp has the input plus minus v in 2 minus plus v in one, this M 4 is connected to a M 5, in series down and this gate is connected to M 5 1 on the other side.

In which M 5 1 is connected in series to M 3. So, what is this known has the impedance higher or lower Vo one and Vo 2 nodes 1 upon Gm smaller loads, but at this output which is like a buffer stage or equivalently in this, there is no Gm kind. So, Ro power Ro huge output resistors are created. We are asking know Ros output is higher yes Ros output is higher actually.

Now, the gain is from M 4 one, to M 4, size changes k times, M 5, M 3 one and M 3 are the same size M 3 and M 5 1 are also of same size, but M 5 1.

Or M 3 to M 5 or M 3 one M 3 M 5 equal, but this is again k times larger size, this is also larger time, but larger of M 4 one, k times that k is more than one, the minimum value of k will be one, we can start the same N channel devices are similar P channel devices are similar. So, that beta N 1 is equal to beta N 2, beta P 3 e one is equal to beta P 4 one, this I can assume W bias are same new C ox is same. So, these are identical they are identical, now we can see from here last stage very carefully you see it, the way I have shown the current, this current is going coming down and this current is going up.

Ac current do not say dc current. So, what will be the current here, the sum of the 2 are subtraction this is mine 1 minus of minus means add up this the current will be very high

here, is that clear we will see how, but is that point clear of this current this currents add at the capacitor end and therefore, the currents are larger the current, output current lager is Gm, this is what we are saying while making it k I have actually listed the current is that clear, by making it k times I have actually are boosted the current, now the way it operates if these voltage ac signal change since these are 180 out of phase.

So, if one changes one direction the other will change the other directions, if this decreases this decreases this also will correspondingly again one it goes up like this, this way this goes down again. So, the idea that choice a such circuit is that between these 2 M 4 M 5 currents, ac currents are always opposite, ac current are always opposite because of the phase I am creating out, now this idea that I can change the phase out is very interesting because then I out is sum of these 2 currents, subtraction means I actually magnitude where they add these 2 currents will be functions of something like this, and something like this. So, I can have control on this.

I can have control on this, and then I will say I can get higher for given v in 1 minus v in 2 or v in 2 minus v in one, such that I can have larger output current for same difference is that clear input signal. This is what we essentially do is that figure is that Issue clear positive negative signal, will push the up and opposite signs, M 4 M 5 says with the output stage of this way the capacity load is been keep this is my output stage, is that clear this is my output.

Student: (Refer Time: 54:17).

Otherwise some where the currents will up to drive the capacitance, the way I have done it that this current will come through M 4, and since larger size I will boost this current. So, this is k times this is going opposite file boost this current also, and this minus this will be more current at the output. So, that I can charge the capacitor faster, is that clear haven't shows all this there is some you keep that figure where in front of you, I will keep in here I am first trying to calculate the current in this P channel device.

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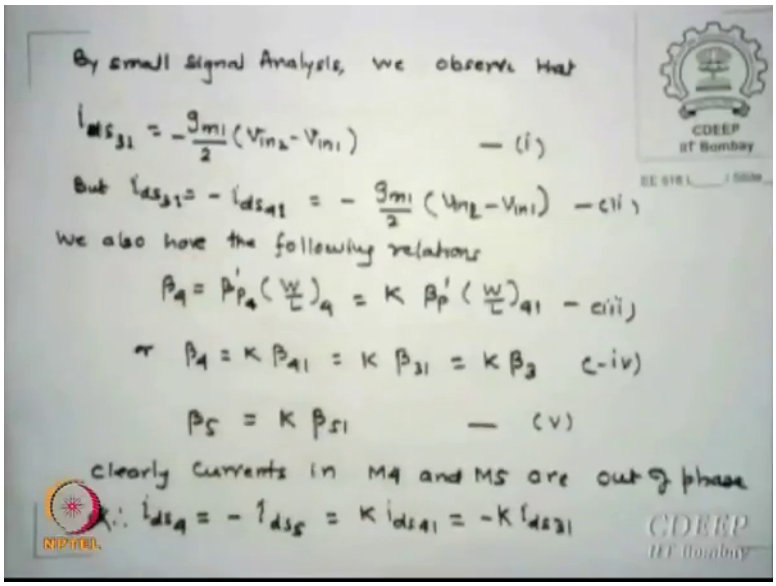

So, Ids 3 is nothing but minus Gm 1 by 2 v in 2 minus v in one, but if you see Ids 3, 3 one and Ids 4 one they are in.

Opposite because one will increase the other will correspondingly decrease. So, Ids 3 one is minus Ids 4 one, is equal to minus Gm 1 by 2 v in 2 minus v in one, now the way we did it please remember this is something trick we are paying, beta 4 this should not be 4 here you beta 4 which is this beta 4, for this is beta dash P into W by L by 4 , but we also know this W by L by 4 to 4 one the size is k times. So, k times P dot W by L by into 4 one is beta 4 is that correct beta 4 one is k times that are beta 4, is that or beta 4 is k times beta 4 one, but you can also see beta 3 one and beta 3 is same, these are not k ratio they are same since they are same and we also since same currents are flowing here and here for the bias betas here or actually, same as both sides.

So, essentially say beta 3 one is same as beta 4 1 please take it size at this is same. So, beta 4 one is replaced by beta 3 one. So, k in to beta 3 one is same as k in to beta 4 one. So, we know beta 3 one is same as beta 3. So, k times beta 3 size, I am just using my sizes and finally, before we come last this size is also k times. So, this beta 5 if it is k time beta 5 1, we already said since the 2 currents are in out of phase, Ids 4 is Ids 4 is out of phase of Ids 5, and then I can write Ids 4 is nothing but k times Ids 4 one only W by L as change from this, and minus since this is minus of this.

So, k times minus Ids 3 one opposite, then what I say once I declare this, is that expression you wrote down I know Ids 4 which is related to Ids 5 by opposite phases and each is related to why 4 one 3 one I use, because these are the currents and the diff amp stage. So, I am trying to equate those currents with that, why I am interested in these currents, because Gms will come from diff amp stage. So, I must know what is Ids one and Ids 3 one and 4 one, what is the output impedance of this has any one noted down, what is the output impedance here see that is the fun.

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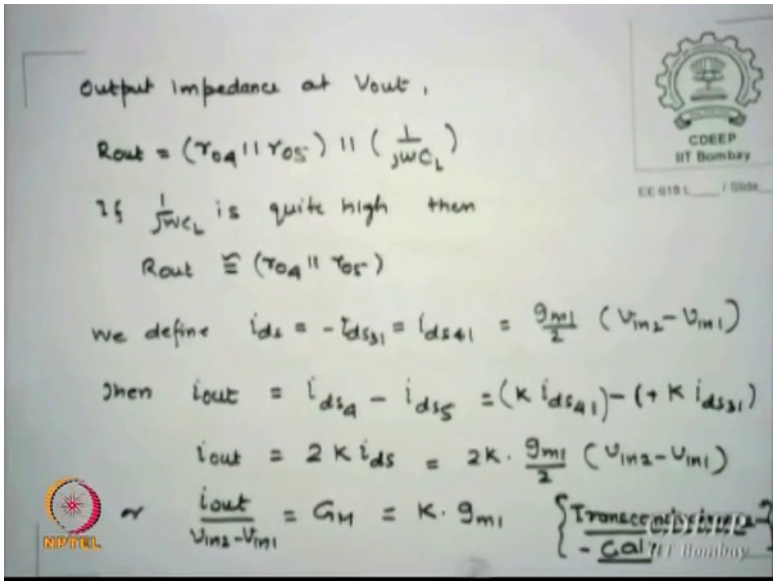

So, if we look at the output impedance at v out, is Ro 4 parallel Ro 5 parallel 1 upon j omega C L impedance of that, is that correct, now generally I mean I am not saying every time you may have to figure it out at a given frequency range, you may find these values this is much higher than these values because normally OTAs have lower bandwidths. So, generally this may be true, but in real life figure it out and then use my statement, but as I say if you normally unless I do intentionally a mistake, things will be correct on this. So, R out is normally equal to Ro 4 parallel Ro 5, now we define current common current Ids which is equal to Ids 4 one equal to minus Ids 3 one, just one same these are same know.

So, I put Ids which is nothing but equal to Gm 1 by 2 Vin 2 minus that is what I derive that way. So, what is Iout current, please look at it what is Iout current, this current minus this current. So, Ids 4 minus Ids 5, which is k times Ids 4 minus k times Ids 3 one, and

since these are opposite signs they will add. So, I get 2 k times Ids is that correct, but what is Ids, Gm 1 by 2 v in 2 minus v one. So, I get 2 k Gm 1 by 2 v in 2 minus v one. So now, I get a ratio of I out by difference voltage, which I call it transconductance of the amplifier which is k times gm 1, that clear k times gm 1. So, ks in my hand how much size I put, ratio wise Gm I can decide that from there where the size of M 1 M 2 or.

The M 5 current I push in, is that correct, bias current I push inside is that correct I can decide my Gm.

Now, here is the interesting part please everyone has seen I out by v in 2 minus v in one is transconductance, which is nothing but k times gm 1 or Gm 2 because they are seen for the sake of brevity.

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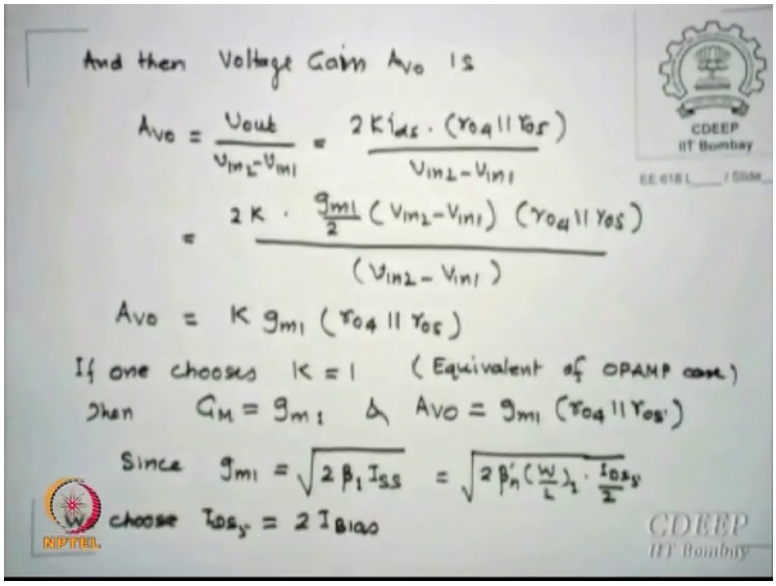

I may even calculate the voltage given rather current, this transcoonductance. So, v out upon v in 2 minus v one is output voltage by this, output voltage can be written all Ids into this this, which is equal to than substitute correctly all these values. So, I get k times gm 1 into Ro 4 parallel Ro 5.

What is k gm 1? Capital Gm. So, Av 0 is capital Gm multiplied that they output resistance again a voltage amplifier. So, it is not that is not being voltage amplification. So, the 2 style OPAMP is also doing this job, the first part there is essentially OTA base, now for the sake of brevity I choose k is one, which is like an OPAMP that there is no

increase. So, we say one. So, Gm is gm 1, Av 0 is this which is what we are what in a diff amp stage anyway.

Since gm 1 now look at the way I did, gm 1 is to beta 1 into Iss which is in this case Ids 5 by 2, now I choose my Ids 5 such that it is twice the bias current I 3, that is double the size I think I bias twice at that.

I pass through my 5 fifth M 5 transistor. So, that you know this half there is nothing the 2 W if I substitute this here 2 I bias, have you please note down and then I will put the last few slides for that transconductance via is OTA. So, please remember OTAs are why they are. So, important is this, now this fact which I am showing you is important and noted down everyone.

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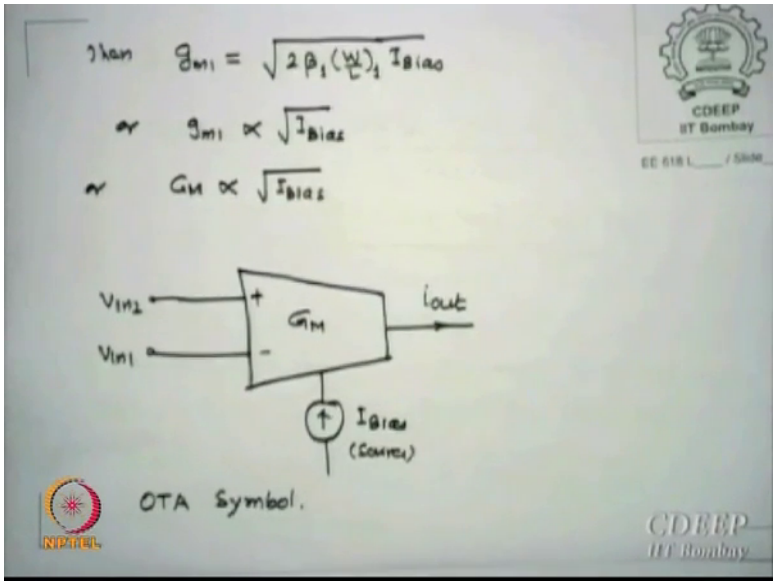

Now, you can look at it if I put that I id 5 is 2 I bias, this become 2 beta 1 W by L I bias. So, Gm is proportion to Root of I bias, and capital Gm k times Gm is also proportional to Root of I bias, what is the advantage of this? If I chase the bias current.

I will chase the transconductance that break as proportion Root of course, but is that clear. So now, I must figure it out, if I want a particular Gm and Gm 1 upon Gm is what resistor. So, if I want to create a 1 upon Gm as large when a R smaller, I should boost larger Gm, why should I need small R what is the time constant associated with the 1 upon R c, is that correct at frequency, if R is smaller the frequency is larger filter cut off

point. So, Gm decides the cut off for the filter, but Gm is decided by bias current I choose. So, I have a OTA which I can nicely configure.

To create a low pass filter, a high pass filter, band pass filter, and it is active device, why because Gm is active element is that correct it is not a passive filter it is a active filter, which is connected from the dc bias current, now the question is dc bias current externally how will I you will have a voltage current source.

So, something I must create a voltage control here, the pin should have variable voltage control, if I do that and if I change I bias for that control voltage then I will be able to from that v control I will change the Gm value is that correct. So, here is the circuit which is very simple this is what we have; I added this additional mirror side from this side P channel.

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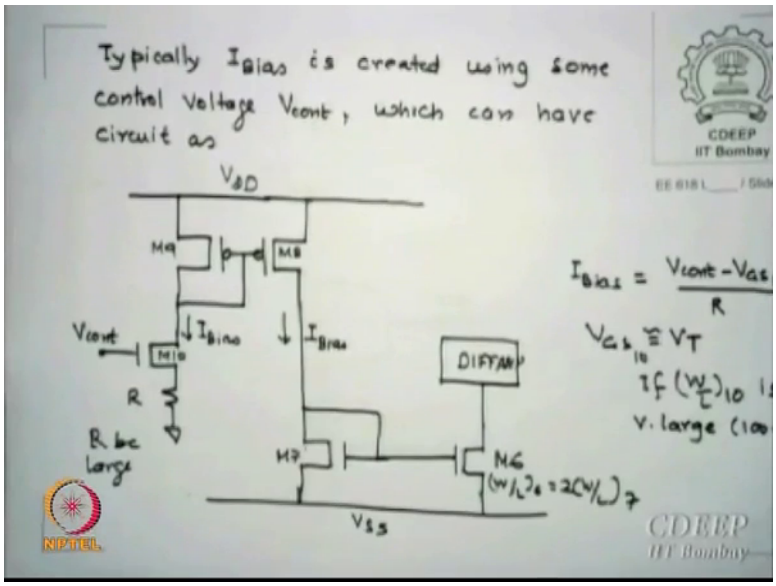

We are looking for there is a resister here isnt it instead of that I measure it to another P channel, and put a series transistor M tan whose M pole is.

Student: payable.

Payable control as we call and the resistor r. Now we can see from here if you are drawn the figure, they are same sized M 9 and M 8 are size. So, the current here is same as this mirror. So, if this is my I bias current, and for the diff amp I made the double size. So, it is 2 I will bias current. So, that the earlier expression is valid and if I bias is to be

created from this the current across this must change, is that correct. So, that the voltage here should be such that it create this I bias current, what current R can recieve what M 10 can provide, now I bias you can see from here, this voltage minus this voltage divided by R what is this voltage Vgs of this is that correct.

Student: (Refer Time: 66:04).

. So, v control minus Vgs 10, is this voltage the minus 0 of course, if you wish, divided by R is the bias current, now here in the catch they nominally for if I keep this W by L as then very, very large. So, Vgs will be very close to Vt, for the sake of this who do not agree I will just solve for them if the size of this is 100, 200 or 500, then the vov will be less than 10 millivolt or 20 millivolts. So, Vgs will be almost close to.

Student: Vt.

Vt. So, I now know this Vt, I know my control voltage which I am varying if I fix R then I know my bias current.

Student: Bias.

Once I know bias current I know my 2 by I bias current which I bias each can give me my Gms, and if I have k factors known to me I all my transconductance k times gm 1, and I also know my I out. So, I know what is the transconductance essentially at the gain transconducting gain as well as the voltage gains are possible is that Issue clear to you.

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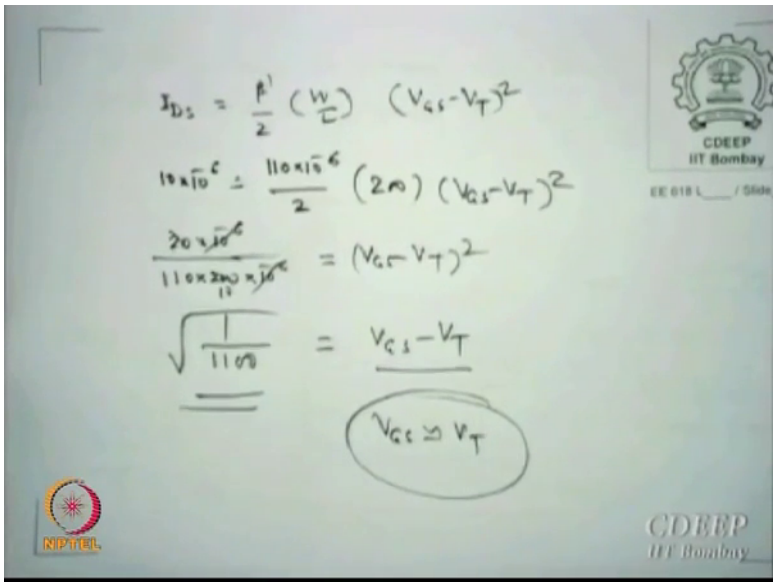

Student: (Refer Time: 67:49).

yes, Ids is beta dash by 2 W by L into Vgs minus Vt, let us said I want 10 10 micron current, for the sake of it this is 110 into 10 to power minus it for N channel device by 2 let us say I make it 200 large size, Vgs minus Vt if I do it 20 into 10 to power minus 6 upon 110 into 200 into 10 to the power minus 6 is Vgs minus Vt.

Student: (Refer Time: 68:06).

Minus 6.

Student: (Refer Time: 68:13).

Oh yes is fine that is not very Issue important. So, 20 this is 10. So, it is 1100 under Root is Vgs minus Vt, this will be Roughly point 02 or point 05 less than point 02 10 millivolts of some layer. So, one can say Vgs is close to Vt yes is that clear. So, one of the techniques of forcing a transistor to remain in saturation is, increase the W by L it will force itself to these 2 saturation is that clear.

This is a trick which we follow often, wherever we forcible is increase the size, is that this will be clear this things we sometimes I said it is equal to Vt only this Vt comes from because of large W by l, if W by L is smaller this is not valid, but if W by L is large enough. So, this M 10 which as I show you here must be of the order of 100 or 200 or

more. So, that it guaranties this voltage as Vgs v in minus Vt, and that Vt is known to me. So, Roughly I can control my current here, and then I can control current here. So, Gms controlled k times Gm is my. So, bias current instead of bias current.

What is done the output will be Gm v proportional to v control. So, I have that when I change the voltage, and I actually get different output currents, is that correct the external thing has only v out v controls pin, it does not because I is very difficult to push we will have to create source of yours bias is always available. So, pin has a control voltage pin, which changes the Gm of the OTA is that clear, that is how next time we will do quickly some filters out of this, and then start on a new area which is not connected to OPAMP analog per say which is noise, let us say how much noise you can make