CMOS Analog VLSI Design
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Lecture - 20
OPAMP Design

A particularly for gain, gain bandwidth product, power dissipations, and the stabilities one major issue, we have done most of the analysis, and also evaluated last time from the given data for a phase margin of 60; that Cl Cc should be related to C 2, and we say that C 2 is essentially encompasses the load capacitance, and total load given to a system pf to the minimum value of Cc which you can use is 2.2 pf, or it can be greater than 2.2 pf. So, based on this we continue now.

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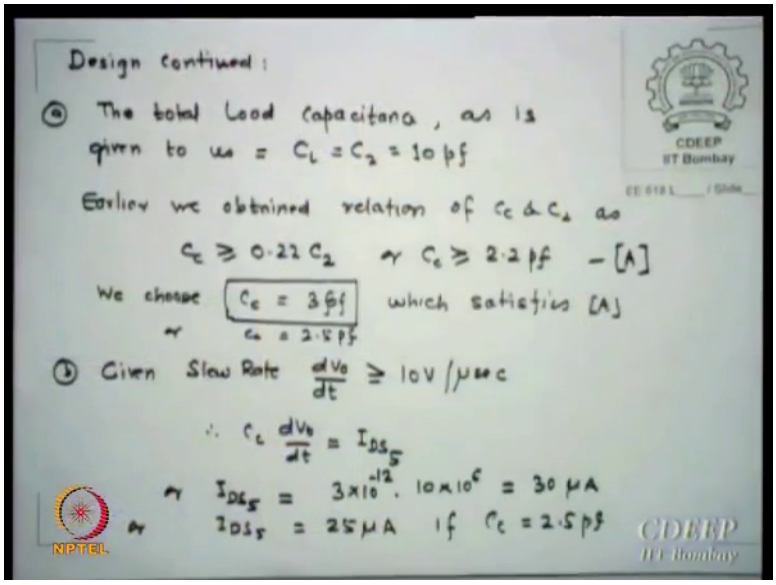

So, if I have a choice of making Cc, I can either choose 2.53 3.5 or even 2.2 itself, because that satisfies the condition of A. I kept saying you earlier larger the Cc value I choose better stability I will get, but then there is a problem of bandwidth. So, I do not want to go too far from 2.2. At the same time I do not want to be very closer 2.2 either

So, there are two possibilities as looked into, but may be finally, I decide I will choose one; either I will choose 3 pf or 2.5 pf. So, the further calculations we are perform with 2.5 pf as Cc, you can choose 3 and do same analysis again, or you can choose 3.2 and start doing everything

The values will keep on changing the method, may not the only problem. You must remember any value I choose here will have implication of all W by Ls, and also the gain. And at that time you should see that gain should not below 4000. So, the issues are little tricky. So, I believe that if you close to 2.2, you choose things will happen, because all This phase margin we have taken care of a V 4000 or something. So, some way this value is good enough in my opinion

But this, my opinion does not count, we should check it if necessary. So, whenever slew rate is given to us is dv 0 by dt greater than 10 to the power 12 microsecond. And since our last time I said the current which Cc can receive is the maximum IDS 5. So, based on this, I can, I have two possibilities, where choose Cc are 3 pf, this may be 30 micro amps. If I choose 2.5 pf, this will be 25 micro amps

So, I am going to use IDS 5, or what is our iss for diff amp as 25 micro amps is that. So, choice of iss and what we now call IDS 5 is now chosen from choice of Cc. So, it will be different if you have a different Cc for example, three, it show a 32.5 25. So, difference is proportional. So, 10. So, you can even choose higher than the, because say you are asking higher than dv 0 by dt, there is 10 volt, but I am choosing 10

Why this numbers are given. So, that let us say in the first round you do not meet specks you are looking for. So, you come back and replayed right. From here you say loop come back and redo again. So, since I met their was specks, I am not going to do second time, but in case I would not have probably I will have to do second time.

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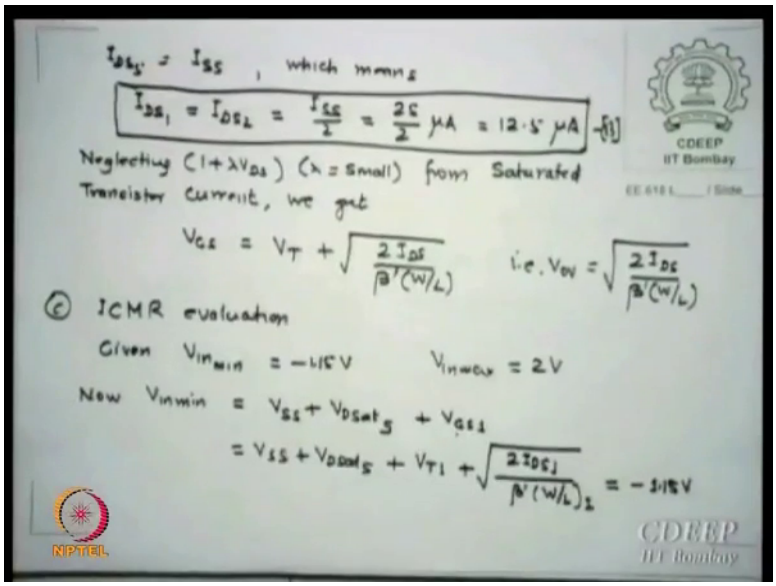

So, an individual arm of a diff amp the IDS 1 and IDS 2 will be the half of this current, which is 12.5 micro amps

So, why these values are needed, because Gms are calculated for these currents, we will now, we also. Please remember that whenever I write VGS, I will be leaving 1 by lambda VDS term, lambda being smaller and then I can always write VGS is equal to VT plus under root of 2 be IDS of a beta dash W by L by this relation, because if I know this, all are know something here, and able to hit W by L through this relation. So, one way of reaching W by L is this expression. So, I will like to use this expression once a while, when I think I can, I have other things known. So, I may evaluate W by L for given transistor, and in this case; obviously, the over voltage or xs voltages under root 2 IDS upon beta dash W by L

The second third parameter given to us, third or fourth what are number is input common mode range. Its not real evaluation form as ICMR evaluation I should say. We have been given Vin minimum and Vin maximum. Please remember this word minimum and maximum are slightly what I would say, they are not very correct what I essentially means. The main word is taken from the Vss, and max word is taken from VDD whenever we calculate.

But the actual value this Vin min is the max value of that which you required, and this max should be the minimum, what I want is that clear to you. So, anything greater than 2

V is fair enough, anything less than this also is good enough, because using a larger fair enough. So, please this slight statement making is very some. So, please what I am saying, the value given to us is the. This is the minimum value of maximum which is two words. I forget 2.2 I am fair enough

This is the at least I should have minus, if I am below that I am still fair enough via larger swings, is that clear. So, these maximum words are not really the actual max. They have taken max word was given from calculation from the uppermost values VDD value down and Vss value up

So, this confusion should not happen, then you are. I am not meeting space actually, we have improving the specks that what is common mode range. We are saying, we are trying to say that in this input swing the transistor remains in saturations, is that clear that is the range I have given you.

So, that is if at even more value it will be still beside is, if you go below VGS minus VT may not be smaller than or equal to VDS, then it will come out of saturation. So, these are the values. So, something going beyond is fair enough, its still if I will increase VDS fair enough. Now what does it hurts me, is that clear

So, this values are essentially taken as min max, but actually the max mins. So, there is some catch word, there is which I use. I thought mainly in the end, I may show you something different value; say oh it has not met. In fact, it might have done better than what was expected from you

So, from this V in min if you see the figure, I may have to check the figure, I should keep it separate now. So, that every now and then I need that. We are done this expression earlier in, when we divide those expressions you can see from here.

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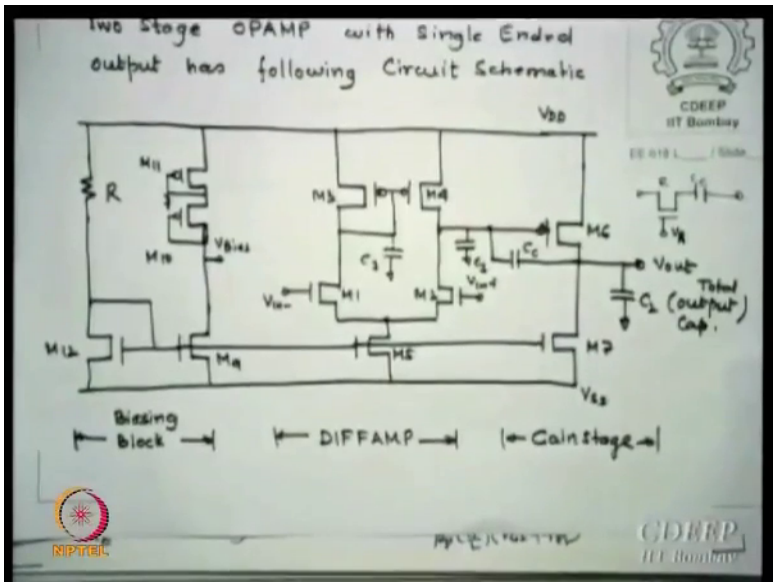

The Vm essentially is, if I calculate from here it is Vss plus VDS sat 5, this voltage plus this voltage plus VGS of 1 is that clear

Reduce this point, I start from here this voltage plus this voltage plus this voltage is V in is that clear. So, again V in min is essentially Vss plus VDS sat plus VGS 1. So, and this value has been given to us is minus 1.125. You can see that 1 was added by me, because when I did some calculation 1.5, I went out of the way, because device came out of saturation. So, I suddenly came out of say I put ones extra there ok

So, this expression and VGS 1 can be writen as VT 1 plus under root of 2 IDS 1 upon beta dash W by L 1 is that clear. Just now I wrote VGS expressions. So, I reuse that expression in writing V minimum. I may not use immediately this value, which I am saying, but the same expressions I am going to tell you this I have finished

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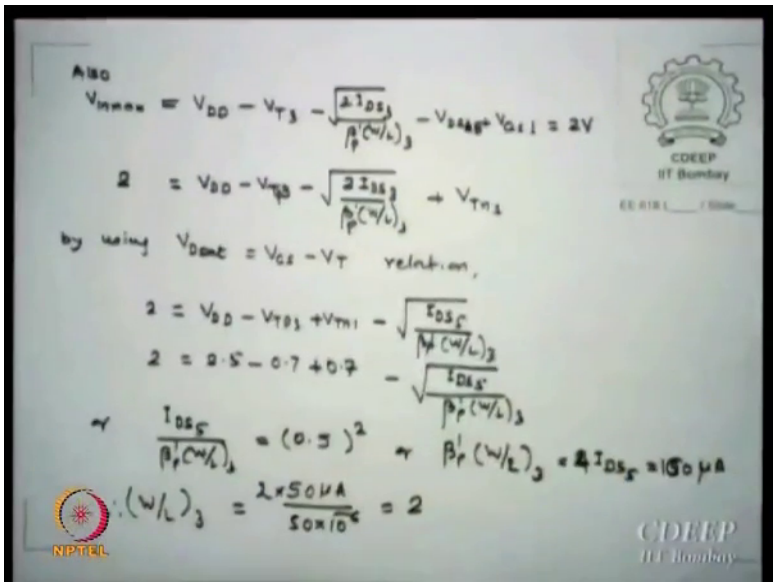

We also see V in V in max max is taken from where

Student: From the VDD.

From the VDD side. So, you come from here, you come here, then you come here, then you come here, and then you come here is that clear. I repeat you come from here, then you come here, then you come here, then you come here. So, this is the V in max which as the minimum value I want really. So, that the device remains in saturation

Now, in this function I will repeat, then it will be VDD minus VT 3 or VT P 3, you should write if your wish. So, that is the P channel device minus this is VGS 3. I am writing, what is this

Student: VGS.

VGS 3 minus VDS sat for 1 plus. Please remember VDS sat, please just this is VDS sat plus VGS 1 is that clear

So, VDS sat 1 plus VGS 1 is given to be us too old. So, if I write 2 is equal to VDD minus VTP 3, and this is n channel device. So, please write VTN 1 . So, and what is VGS 1 minus V T

Student: V (Refer Time: 10:06).

We those. So, we actually rewrite in that expression. So, I will get 2 is equal to VDD minus VTp 3 minus this number, but this essentially is VGS minus VT is VDS. So, that value are substitute as VTn 1. I keep doing this and finally, from this, because I now know this I know this, I know this. Now the only catch I said by last time I did say that here I has used it 0.7 as the typical value of VTs, and I say you know that normally max min values you should choose the worst cases are having 1. So, that max min values of those, you should choose which will give you that bar better than the normal

In this calculation I figured it out W by L 3 is just 2, which essentially is, what is the problem if W by L of P channel device is smaller the resistance is higher. So, nothing wrong, but they are the resistance is 1 upon Gm 3, which may not be done higher lower actually. I mean I want that to be higher. So, I feel this two slightly smaller value. So, I did some tricks you write down this, yes

Student: Sir.

Yes

Student: VTp 3 is (Refer Time: 11:25) minus 0.4 (Refer Time: 11:27).

Actually if you see that signs have been taken, this is 0.7 minus, no this, that in writing may already taken care of the sign VGS minus VT. So, VGS has to the negative, and VT has to the negative, then only is always may need to subtraction, because you cannot exceed the value given to the supply

So, using this, these are standard expression how much W by L I got for the transistor 3 is 2. We also said that in all our designs m 1 is same as m 2 by size, as well as V T and m 3 same as m 4 by both V T as well as sizes. So, once I know W by L 3 as well no W by L 4

So, I in my opinion, since my I choice a typical values of VT, I got into a small value of the heavy written down. I keep say these are only three ways, just write this expression and maybe this which I, and this is also sometimes rounded by me. So, check it, because this is I always hand calculated at times, not using calculators is it.

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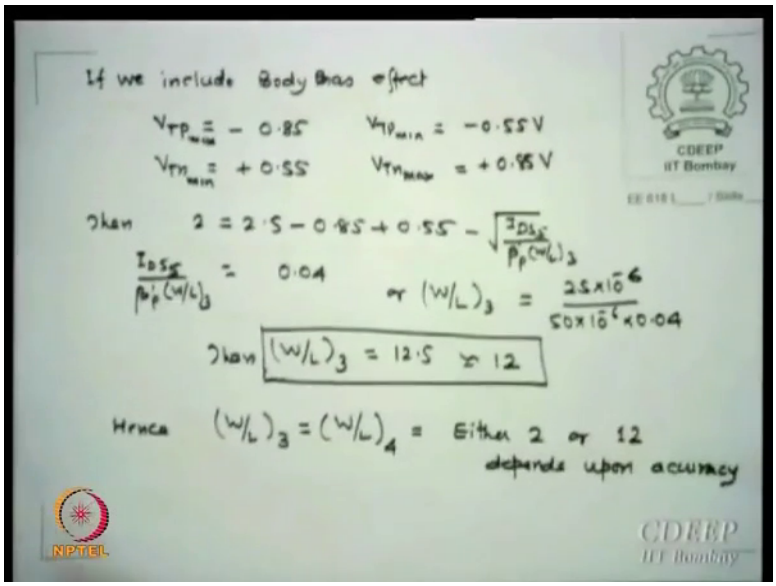

So, if I use now VT p max as minus 0.85 VT p minus 0.85 that is I say [FL] of 0.15 is what I expect max min values to shift from the typical same way VTn minimize 0.5, and this is 0.85

So, now if I say to get the value of V max, I subst that has to be too old, I must subtract highest value of VTp, because then the, then it should satisfy two, then I should also satisfy the most value of VTn, because then it will the max worst case, and therefore, twist is should satisfy my two requirements. If I now substitute with this, I can recalculate W by L 3, and it turns out to be 12.5 which is 12

So, just think of it, if there is a bar on VT, the W by Ls can changed by 5 to 6 times. This is an issue, which you, I wanted to bring to a notice that for me as a calculation, I may say 2 is good enough, what is bad big about it, but in real life the value may change as much as 5 to 6 times, if your VT bars are such high values is that clear

So, this the designer should keep in mind that there will be a max min values, always associated with the data given to you, even they will specify a 0.7 plus minus 0.15. So, there is specified that delta. And therefore, right now I have used it same VT and same delta VT, but for p channel and n channel VT will be different, and their delta will also be different. So, maybe we have to do little more calculations correctly for the real life situation for simplicity I have made equal everywhere. So, that at least I will get the numbers of my kind of numbers I am looking for ok

Coming back to your Vin, what is the Vin max value, you can see from here, from here. If I want to reach Vin 1 method is VGS 3 plus drop across m 1 VDS 1 plus VGS 1

Now, if this value has to be say minimum maximum for the worst case. So, whatever I subtract that still should reach to, that is the value given to me. So, what do I say. So, I will VGS 1 I know is VT plus under 2 under root 2 current flowing through this. So, I choose the maximum of VTp, because that is the worst case available to me

When I calculate this drop, this drop is nothing, but VGS minus VT. So, I actually my C 2 at the, that drop is the maximum available to you. So, I also you a corner you put VTn. So, that the, because it will be subtracted out of these. Please remember VGS minus VT is VDS. So, if I have to subtract out of it, I should choose minimum value of VT. So, that is the highest drop across which it will come. So, that the, still it will satisfy your 2 volt requirement, this is what I say Vin minimum or maximum

But whatever that mean, if something is lower than this, fair enough. Sorry higher than this is fair enough, because these values are chosen worst cases. In fact, they will not be that bad. So, this value will actually exceed to word, and that is nothing wrong with us, because devices are saturated even with this values is that clear

So, anything beyond is still satisfy able is that clear. So, the way value we chose, is called worst case situations, if that satisfies the saturation condition, then the other conditions are always going to satisfy. So, we say, we are well within our limits to actually see terms and immersion, whatever what you mean always, no transistor should come out of saturation.

If this is the case; that is VDS must be equal to VGS minus VT or greater than VGS minus. As long as that condition are satisfied I am always. So, edge is equal. So, if that is satisfied by anything higher will VDS higher will be better. So, I am safer when I say I take the worst cases, and then I say it does not reach that; fine, thank you; that is the way we actually assume the values.

Student: (Refer Time: 17:01) VDD is 2.5.

Fine, because the, I am asking more swings. See my worries are that how much Vin I am allowed in. So, larger input swing is better you, and with that also devices define worst fantastic.

Student: So, (Refer Time: 17:17) I am asking to be a calculate 2 volts.

Two volts if it becomes 2.2 volts I am fair enough.

Student: V means 2.2 this will work.

It will still work how much, because; that means, still try to satisfied as long as this condition is satisfied, I am least bothered about it. Saturation condition should not be actually defeated by me; that is that minus value become plus. So, Vin max, Vin min cannot be plus, it should be minus as such call then higher end of the vid

What is, we are looking for minus vid by 2 be plus vid 2, in this range device remains in saturation. I am trying to see if it is, it does not go to minus sign, it remains positive, then I do not have a swing is that clear. So, with the minus 1.5 if I put I will find (Refer Time: 18:03) or in the other way subtraction. So, I will say, I will reduce that value. So, at that still remains negative value. You do calculations, I did not bring those, but I do then. Therefore, I will removed them actually ok.

So, either now is that I got W by L 3 equal to W by L 4 equal to 12. You can also for the sake, where that you can say 2, its and nothing wrong if 2 put, you put it and everything else is satisfied. I have no objection, I am using two. Better if it is too why, because it will reduce capacitances, it will reduce, also it will increase resistances. So, everything is fine, area will reduce. So, I should not really boost w, but I am now worries that, I mean I may lose something else, and because I know typically it is around 10. So, I thought I will see that, what is the worst case situation I use, and I will increase it; that is a trick

This will not know, because you are not seen actual chip. So, because you are seen it, we know at least boost it little bit and; however, boost it, I figure out this is the easiest way of looking at it, and we can, it will be higher than 2 anyway ok

So, once I declare. So, how many things I have now calculated. I have calculate W by L 1 and W by L 2 W by L 3 and W by L 4. So, diff amp case sizes are now fixed by me. One, we are not yet reached one. We will calculate, we will calculate from some gm 1

requirements, when you, which will come from the other area, we will calculate we are. I am sorry, only we are calculated 3 and 4 you are right very good

Now, I, last time I said before we proceed further our assumption is stabilitive was that.

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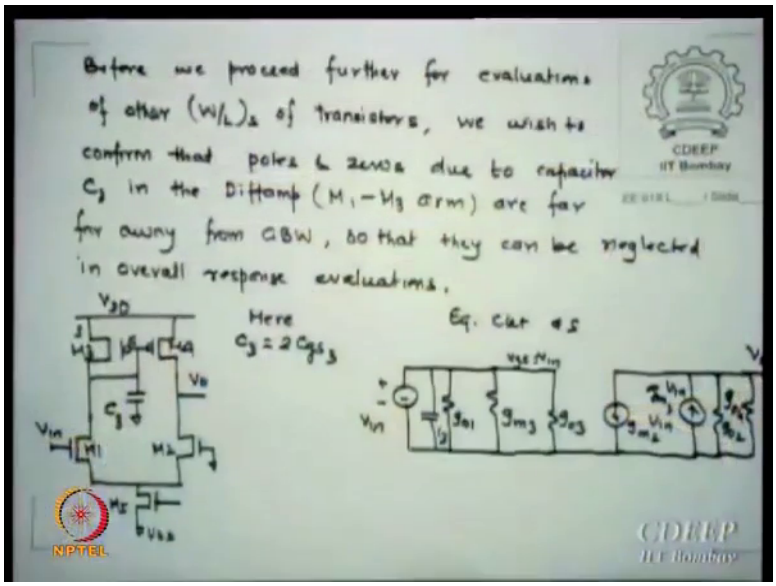

The pole at pole 0 at c, because of C 3 in the diff amp, does not contribute to any stabilative issue, because these poles and zeros are far away from the large way. Also the, we are assume z 1, even it is higher than that, and if that happens I will say it is. So, far away, and fortunately both are on the left half plans. So, actually it is not going to effective in any sense, as well as you have this

But this statement cannot be taken on a phase values. So, I have, did evaluate and check it whether those values are available in real life. If you do not calculate 99.9, nothing goes wrong, but for the brevities I must say I will calculate. So, this is your diff amp, this is your equivalent circuit, this is your input, then C 3 is the capacitance go 1 g 1 go 1 go 3 by this gm 3, because this is diode connected.

So, 1 gm 3 and this is my VGS on the other side from this arm gm 2 Vin gm 2 Vin plus gm 3 Vin. now this current which I am current, I am showing, is the current flowing in this actually getting mirrored is that correct, its getting mirrored. So, that mirrored currents are shown here. So, this gm 3 Vin go 2 go 4 in parallel, and if I solve this circuit which you should be able to, how we are solve. These are resistance; these are currents,

which I calculate. We solve this. This is a standard diff amp theory. I do not ask me to redo the diff amp again ok.

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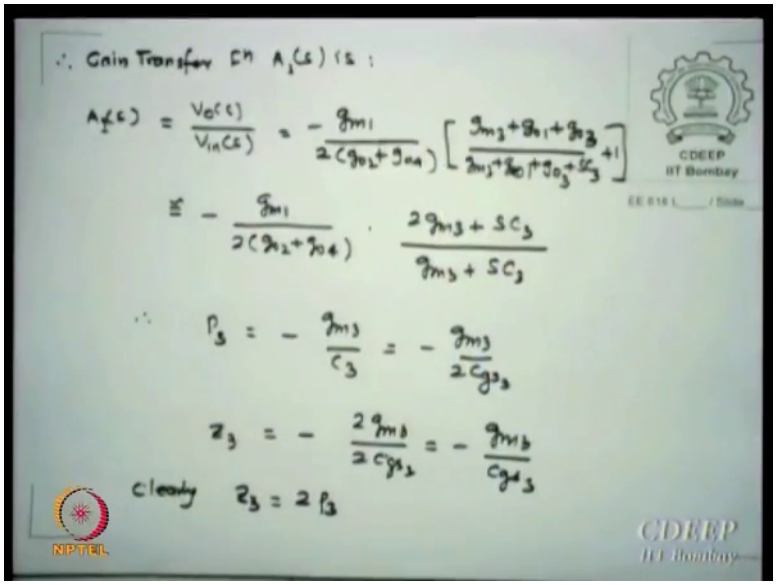

So, I calculated the current gain, transfer gain for this diff amp, which is V 0 s by Vin s, and it turns out to be, why are you use gm trans gos. Now suddenly, because I say 1 upon ro 1 upon ro become difficult. So, if I write gs, I just add g. So, sometimes i. So, gs sometimes I do rs, you can make your choices as much ok

This is a, if you know myself and Professor Sharma has been teaching, this courses lop many industries, this g (Refer Time: 22:10). He always like to like gv is this i. So, that is why sometimes when I am teaching with him, I also follow his way. So, these expressions we have picked up from my others old slides. So, I have got this big expression gm 1 upon 2 go 2 go 4 gm 3 plus go 1 plus go 3 upon gm 3 go 1 go 3 plus sc 3; that is the impedance due to this Sir Kirchoffs Law and get this expressions plus 1

Now, I can say gm 3 is much larger than go 1 and go 3, and then we start doing some interesting calculations, I get minus gm 1 upon this. This can be expressed as 2 gm 3 plus this one [FL] gm 3 plus 1 [FL]. So, that becomes 2 gm 3 plus sc 3 upon gm 3 plus sc 3. Then we say gms are larger than gos. Further if we keep doing the same ways, we can say the third pole you can say from here, third pole is ,because of this, which is minus gm 3 by 6 3 this 0. Means this is dc, dc gain. This is whole, this is 0. So, p 3 is minus gm

3 by C 3 which is gm 3 upon 2 cgs 3. Why 2 cgs at that point cgs of 4 and cgs of 3 rn parallel. So, I just made 2 cgs

Now, what is z 3 2 gm 3 is a sc 3 is coming, said gets 2 gm 3 upon 2 cgs 3, which is gm 3 by cgs 3. So, which is higher the 0, is still at higher frequency than the pole 3 a 2 [FL] denominator is smaller. So, the value is larger denominator is higher, means value is smaller is that clear, is that. Therefore, z 3 is twice of p 3; that means, there is still ahead of p 3, but both are of this sign

Student: Minus.

Minus left are plan fantastic. No issues, they are far away from p 2, they are far away from gbw. So, we say if values which I calculate for this, comes out to be in gigahertz. I say thank you very much

So, now to these have you, everyone noted down as I said this. I am only showing you further, sake of this, we should not say why are lease that. So, I actually taken a data and substitute it this, what is typical cgs. Should be two third cox, is in saturation, typical value which cgs can be given is. Of course, there is a (Refer Time:25:06) of capacitance. So, you may add something additionally, but typical value as, this we can chooses two third cox

But that cox is per unit area. So, what is the area of this transistor W 3 into L 3 .

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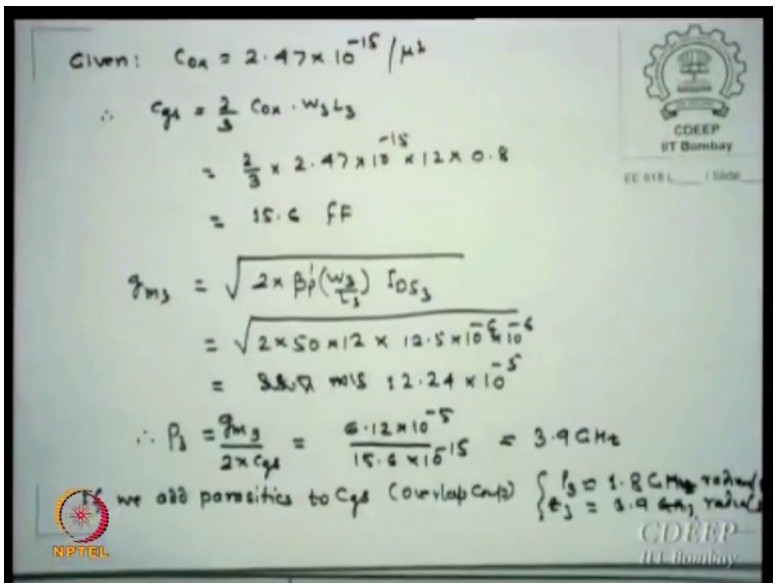

What is the technology I am using 0.8 micron. So, I will choose limp as 0.8. Its not compulsion I am choosing. It you can choose some other values of length and still do everything

Cox from the data sheet is 2.47 femtofarad per centi microns square 2.47 10 to the power minus 15. femtofarad are not 15, then 2.47 femtofarad per micro amps. Square is the value of cox. I multiply it by 12 micron by 0.8 mincrons W 3 by L 3 into L 3. This is an micron square. Now is that clear. So, I do not have to write 10 to the power something, because this itself is now taken in microns square. So, I just multiply it. So, I get the capacitance cgs has 15.6 femtofarad is that clear, cgs

I want to calculate gm 3, because the pole and zeros are related to gm 3. So, I substitute gm 3 is 2 beta p dash W 3 by L 3 IDS 3. What is the IDS 3 half of IDS 5, which is 12.5 micro amps. So, if I substitute beta p as 50 into 10 to the power minus 6 IDS 3 is 12.5 into 10 to the power minus 6 W by 3 W by L 3 is 12, and solve, I get 12.24 into 10 to the power minus 5 3 mums

Student: Sir this W by L is 12 or W is (Refer Time: 26:57).

W if L is 0.8 it cannot be 12

Student: Sir here we could W 3 is 12 (Refer Time: 27:03) W by L is (Refer Time: 27:04).

So some small number you will change. You are right. I am sorry, I have probably a assume one and get that, but you just calculate from there, you are very good

Student: (Refer Time: 27:17).

No. So, it does not matter. So, that is why this is a, I am not changing. You are right, but he is right for a 0.8 micron W by L 3. It will be more than 12 may be 10 by 0.8. So, around 13.0 something instead of 12 [FL]

So, if I got. So, what is the pole. Now gm 3 by 2 cgs. So, I got the pole of 3.9 gigahertz. If I add cgs more, it may slightly go down, because then it will be lowest, it may come to little 1.8 gigahertz or 2 gigahertz, even with additional capacitance, if I put I may, I am still in the range of gigahertz

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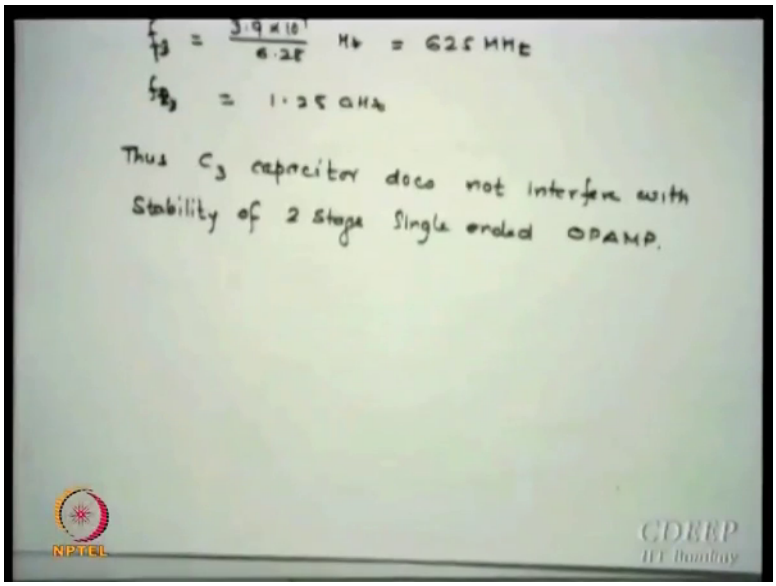

Please remember this is not gigahertz. This is in radians per seconds. So, [FL] frequency [FL] 2 by [FL] divide [FL]. So, f 3 [FL] pole [FL] fp 3 is around 625 hertz, where fz 3 is 1.25 megahertz gigahertz, how much is a gain bandwidth given to you

Student: 6.

6 megahertz, 600 [FL] temp 10 time [FL] gbw [FL] 64 [FL] double [FL]. So, we can say that C 3 p the poles and zeros due to C 3 for the case, we are solving is of inconsequence, as far as the stability issue go; otherwise you may have to even take transfer function, which is third order, and then equations will become even more complicate it is that clear

In our calculation we thought C 3 does not exist, I thought why did not take it. So, I wish you to verify myself I say, I said you, but may be for other case, because I had data which is from other technology 5 micron. So, I can, let me check with a data available for 0.8, and then I figure out that, even with this I am far away from gbw, and therefore, p 2 also. So, anyway I am not closed by. So, I say do not worry too much about C 3s. So, that is why in all analysis, in many books, they not even, they do not even show this C 3. The reason probably is, for a given technology, this will normally not affect any of your stability issues

And therefore, they do not consider, but for other say I want to now clarify that why the designers sometimes do not tell you, but do use it anyway. So, this is what they use it,

they known by experience. This will be 25 or forget it the reason why, because cgs is in what value femto to others are in picos. So, that number ratio itself is telling you that, you will be far away from this situation cgs is in order of femtofarads. This is the reason why it will always be far away from it is that to everyone ok

So, now once we said that I am not going to utilize this transfer function for 3. Do I, did this evaluation for the heck of it.

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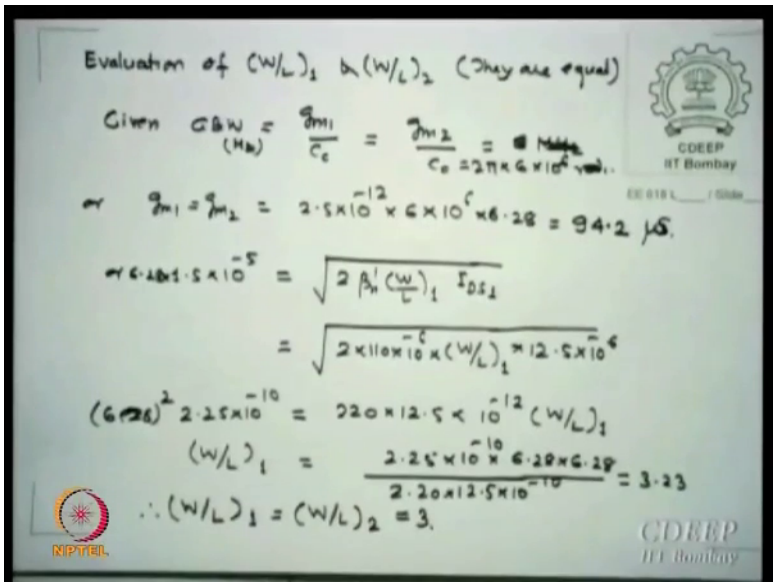

Now, you I said, I will like to calculate gm W by L 1. So, here is the calculations, we more gain bandwidth product in variance in. If it is in hertz multiplied by 2 2 pi. So, it is gm 1 by cc, or which is same as gm 2 by cc, and that is given to you as 2 pi into 6 megahertz; that just writing 6 megahertz is not correct; that is not the frequency, it should be written; that is in actually radians. We should write in radian per second, you should always multiply it by 2 pi to make it hertz

So, if this is the value which is given, then I calculate gm 1 gm 2 is 94.2 microsiemens, s is not second microsiemens to what can I calculate. The idea is, one is known beta n dash is known. So, all that is missing is W by L ok

So, I substitute these values here, and I have got a value of W by L equal 1 is equal to W by L 2, which is equal to only 3, which is correct. The reason why the lower transistors are always, because of the capacity effect they hold, that should be smaller than the loads

is that. Correct; that is how the large current. This is a p channel device, this is n channel device. So, matches to be there. So, n channel device should be smaller than p channel device for same currents to flow through

So, this value which I got, is now, you can see the value I got is 3.23 in out layout editors. There is nothing 3.23, it is only integers are allowed. So, never use very random numbers, always try to go to the nearest integer, and in most cases, I do not do it. We should actually make it in binary numbers 2 4 8 kinds. In layouts, the simplest way of doing designs are 2 4 8 with the problem is, if I use the, I have to reevaluate for all of them, and check whether I am write. So, I am not doing it. So, I am keeping 3, but in real life simulation you do not mind is not it. You will put that value and higher value also a, and check if it worst or fine

Why I am not doing it. I am telling you as such this all values are never actually used by as in designs, because there are layout a data does not give accuracy of such second decimals. So, we normally do not play too much nearest value to that, we use, and we also check right now. Of course, I do not know whether this is worst case, we always see to it that the worst case is chosen. So, that with this, is also if it is satisfy, if I choose higher value it will always satisfy this way. I do not know whether this is the worst situation, but I just round it to 3.

What should be the, what trans the, what value is, I have got now W by L 1 W by L 2 W by L 3 W by L 4. So, diff amp [FL] transistor I know now their values. So, which is the last value in this diff amp the 5, which is your source rather seems to that. So, that the next calculation should be now perform for W by L 5 is that clear. All my procedures are based on individual, how to reach each value of W by l

Student: Sir.

Yes

Student: W by L will be less than 1.

[FL]

Student: (Refer Time: 34:20) increase.

If you will increase the lambda, the lambda change, length is allowed to be change is not, then again it should be integers, let us say it is 0.8, the next value will be 1.6

Student: (Refer Time: 34:31) all calculation just change the.

No, but lambdas will vary at the different length, lambdas are different. So, we will have to from the spice, we will have to find which is lambda

Student: Suppose (Refer Time: 34:42) normally (Refer Time: 34:44) less than 1.

I agree with you, I choose to a, you exceed for that, for that, for that 12 value, you must get your r 0 correctly, for the lambda chose different. Now is that correct. If I 0 changes I gains will change, all poles will shift. So, there is a issue which is not just by putting to, you can always use it. Of course, this value will never come less than 1, the list will get 1, but in case it comes, this is doable is that

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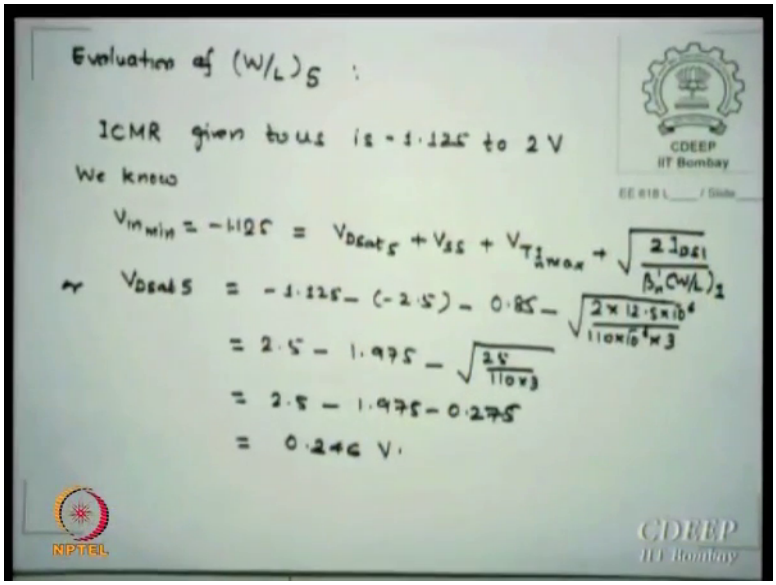

So, the next value I am interested in base values my Vin minimum value vd sat my, this is 1.125. I rewrite that expression. So, anyway I got vd sat 5 from this calculations IDS 1, I know beta n dash, I know W by L 1, I know, this I know, this I know, this I know. So, I calculated vd sat 5 as 0.246 here minus of minus is 2.5 plus [FL]. You must have observed there, you know [FL] line [FL] 1.12 [FL] 1.54 [FL], we just look at it is 5.1.5. So, [FL]

We got the point what could I, if I put 1.5 here, this would I have become negative. So, I just [FL]. So, that it becomes at least positive, this is taken other side. So, one kind of vd sat 5. So, what can I calculate IDS sat is IDS 5 is beat n dash by 2 W by L 5 into vd sat square VGS minus VT.

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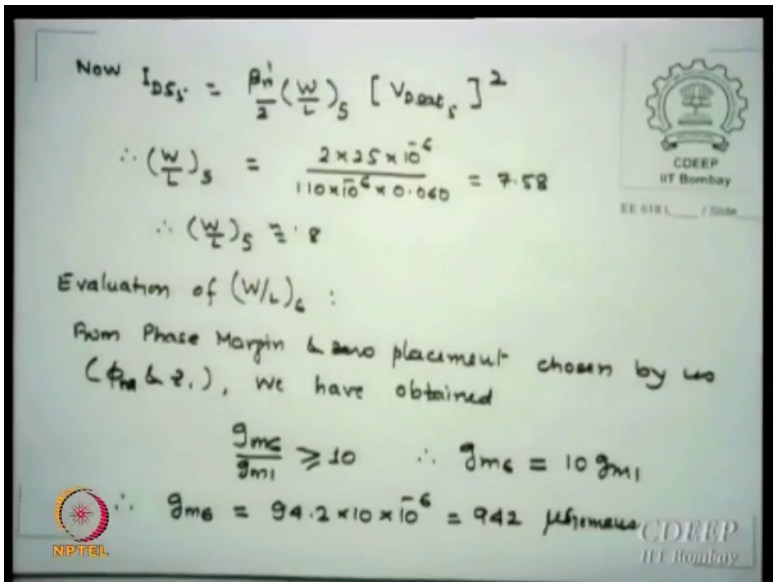

So, with it IDS 5 expression [FL] and some, there I evaluated W by L 5, which is 7.58, which is rounded to 8.

Why I am saying, I am not worried too many, because these are the specks. We will start with your design, and verify is that clear, but if you have no such value, you may choose 16, you may choose 4. So, where do you initial value that W by L has been chosen. This gives you very good guess for that.

So, in 2 or 3 times, the spice issues actually get that, all specks correct [FL]. What is the next one? Now a gain stage, you know I always as a diff amp does not get diff amp gets equal gains, but normally diff amp is not scale gain stage, the next stage of amplifier is called gain stage ok.

Now, if I say W by L sat I go back to see my phase margin relations, I figured out from there. If you check our earlier gm 6 by gm 1 should be larger or equal to 10 I shouldnt be the equal value gm 6 10 gm gm 1, I have just calculated. So, gm 6 is 9 42 microsiemens. from there what do I, what can I calculate, what is the next. Now I am interested in,

because [FL] V out max [FL] what is V out max. From here expression output per VDD minus vd sat 5 6 I must now calculate vd sat 6, if I know gm, I should be able to eva evaluate vd sat 6. To do this I do little trick.

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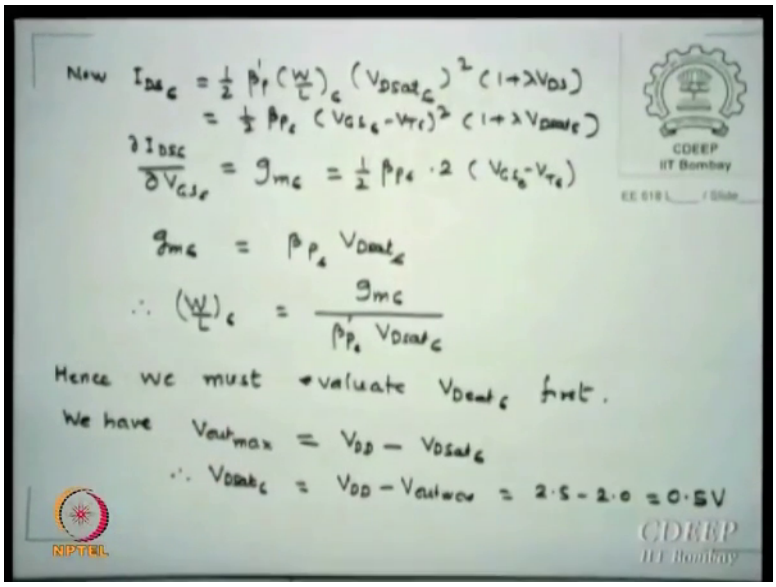

I write IDS 6 expression which is half beta p dash W by l, instead of this I write VGS 6 minus VT 6 square into this differentiate. So, I write gm 6 equal to half half cancels 2 cancels. So, beta p 6 2 of this. So, a VGS minus VT by that VGS minus VT is vd sat. So, I got VT p into vd sat 6 as my gm 6 is that ok

So, my I had W by L 6 is essentially equal to gm 6 by beta p dash 6 into vd sat 6, but vd sat 6 [FL] that I will now calculate is that to all. From here I got a relationship between gm fairy 6. Madam sorry [FL] differentiate my 0 [FL] vg [FL] allowed lambda term is small size. You can always start neglecting, whenever this gms calculation starts, whenever gm calculation start. So, W by L 6 is gm 6 upon this

What is V out maximum, we are given to you VDD minus. Please look at the figure just a minute VDD minus, this is the vo is that clear. So, I say VDD minus vd sat 6 is my V out max. So, vd sat 6 is VDD minus V out max. So, 2.5 minus 2, which is 0.5 is that correct. If I know this, if I know this, I already evaluated this or what do I calculate

Student: W by l.

W by L 6 [FL] expression [FL] data [FL] that is the trick in design image it, here once I did vd sat 6, then I know V out max is VDD minus that. So, I actually evaluate vd out max is given to me as to 2 volt. So, I will get vd sat 6 as 0.5 volt. So, W by L 6 is gm 6 upon beta p dash vd sat 6 substitute, this is 50 10 to power minus 6 this is 9 4 4 10 to the power minus 6.

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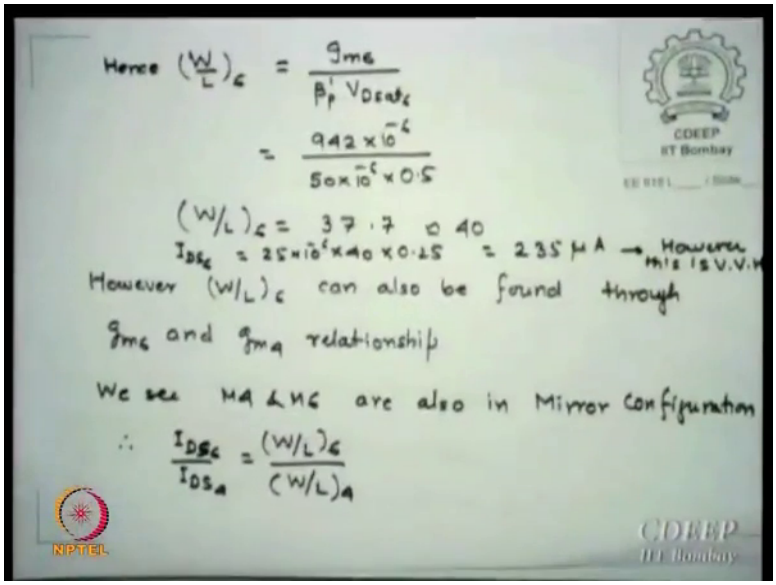

So, W by L 6 is 30 7.67 [FL] that is the most worry some part in design; that is why I am going to tell you, why I this value I am not accepting, I said fine W by L 6 if I calculate, I will get 40 value roughly, and for this the id 6 is 2 30 5 micro amps. What is that maximum IDS if I am playing 25 micro amps.

This is roughly 10 times, I am pushing in the last transistor size at W by L of 40, like a buffering; [FL] that is not very much good, because this seems to excessive power consuming device, because [FL] power [FL] limit [FL]. So, I said there is something I must have done wrong, or at least I am not getting the correct value which I should get

So, I said I, another way of calculating W by l, let us check with that. Now you can come back to this circuit. Do you see this m 4 m 6 also forms a mirror [FL] connection [FL] actually [FL] circuit [FL], but actually connection [FL] it is like this current. There is no everywhere get. So, this mirror is mirroring in this, in the ratio of m 6 to m 4. I just let you this, VGS is equal to this VGS. This VGS minus VT is this vd sat, which is same as

this VGS. If this VGS, this is very close to this value, this current will be mirrored in m 6 by some ratio of size m 6 to m 5, you tried this, this is what we did [FL] expression [FL]

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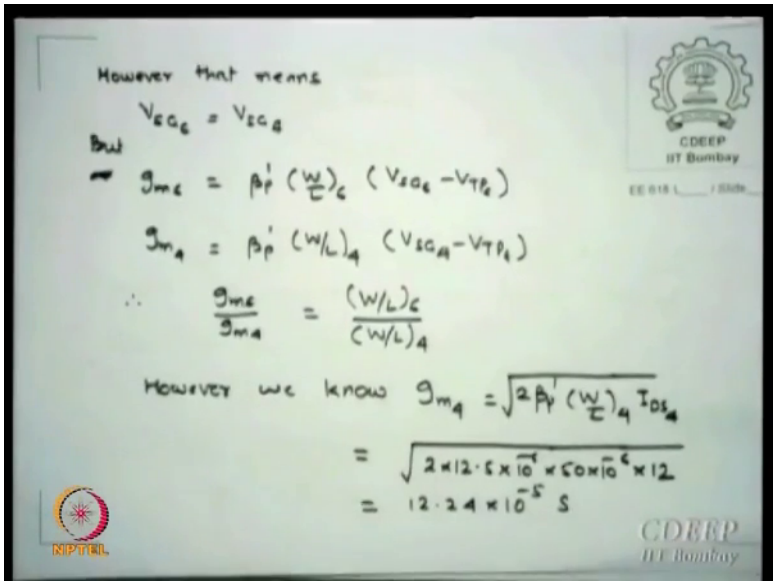

So, IDS 6 by IDS 4 is ratio at sizes; however; that means, and that is the verification what does that mean vga sc 6 equal to vga sc 4 you condition [FL] condition [FL] equate [FL] g 1 6 [FL] gm 4 [FL] yes. So, vs g 6 is equal to vsc 4. So, I will calculate g m 6, I calculate gm 4, the ratio of the two is W by L 6 by W by L 2. So, as long as I prove you that these are equal my assumption of gm 6 by gm 4 is same as W by L 6 by W by L 4 gm 4. I can calculate why, because I know this current, I know the size. So, I will calculate this as 12.24 10 to the power minus 5 microsiemens or 122 microsiemens gm 6 by gm 4 is the ratio of W by L 6 by W by L this, this I know, this I know, this I know is it everyone written down gm 4 is 122 micro siemens, I got 0.4 microsiemens

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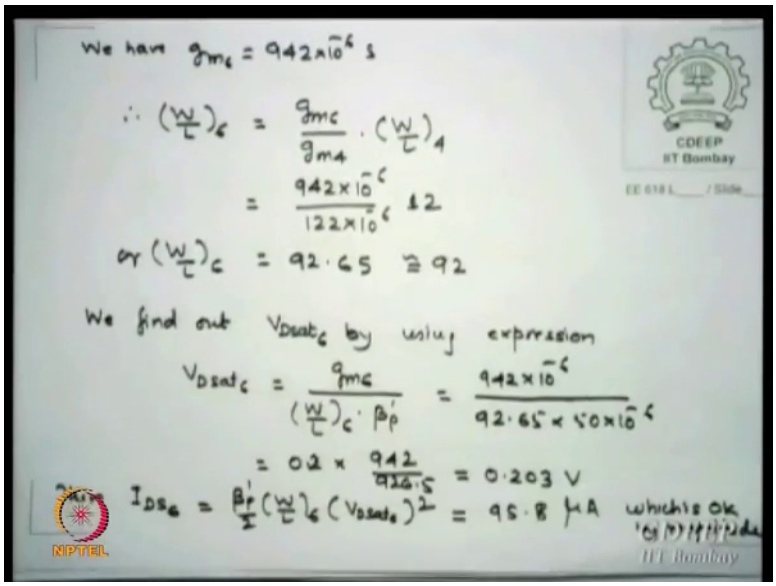

So, I get gm 6 by gm 4 into W by L 4 is W by L 6, which is now 92, how much for earlier 40. Now I increase it to 90; that is seems to it, but if I now calculate vd sat 6. For this, I get the value of 0.2 go 3, when I calculate the id sat 6 current for this, which I get how much value 95 micro amps. This is compared to 235, this is acceptable limits for me is that clear

So, I will choose my tricks [FL]. So, I found that if I now choose larger size of W by l, I can get different vd sat value, and for which then the id sat or id 6 will be 90 odd micro amps [FL] 235 [FL], at least 2 and a half times. [FL] [FL] worries are at the end power estimations. They actually seems the current chosen by me as so small, and the limit I put was too high. So, I think anything is satisfy able there 2.5 milli watts is a huge power, all that we are going to get is, less than what a anyway milli watt with all calculations.

So, this 95.8 micro amp is reasonable value power thinking. So, I say you can start using W by L of instead of 40, boost it to 90. So, that now at least I currents are now within my acceptable range. Also you can find some here, how much is V out minimum, you will get. Can anyone tell? So, 2.2 or something. So, which is 4 enough, because we are expecting.

Student: 2.

2. So, it is (Refer Time:46:08). So, 4 enough, what is the next on the side left now 7. Please remember I kept telling you earlier also, the current in.

Student: (Refer Time: 46:17) divided by 6.

Is not decided by m 5, but decided by.

Student: M 7.

M 7. So, this current is flowing here. This current is fixed by you, for gm sized. So, the ratio of this should be; such that it sustains the current of flowing from m 6 is that point clear. I will repeat the current on this are, means not decided by this. This is the load transistor, there this is the driver, current is picked up from here, which actually goes run through m 7; however, m 5 and m 7 are a mirror. So, for this point current for this current, I will then make a sized ratio. So, that this current flows through also

Student: M 7.

M 7. So, it looks if I basing to that, but actually I am not biasing randomly, same current are not passing, and biasing it correctly; such that it flows that much current in m 6 is that point correct to you. I repeatedly saying do not push same current here, because in that case this current will be different. So, come from m 6 figure out, what is the currents you are I expecting to get the W by l. Further W by l is that current for m 7, and then find the ratio of the this to this, this current I know this size, I know this current I know, if I know this size of m 7

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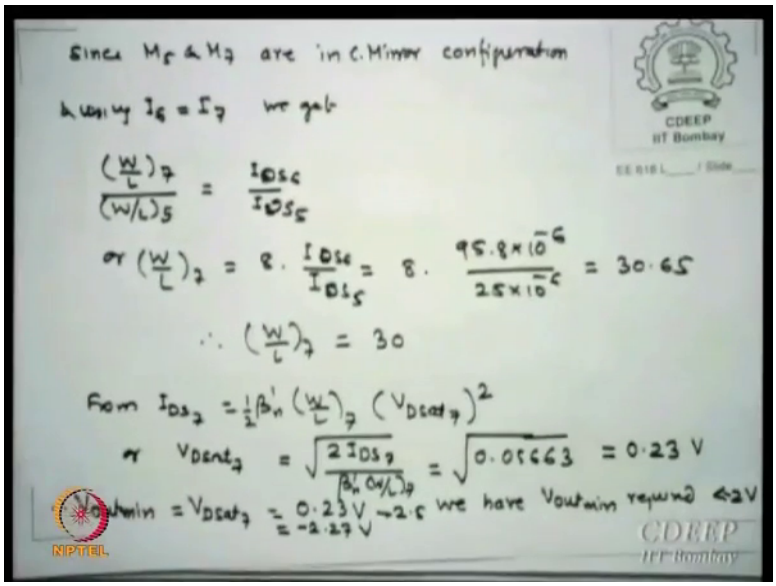

So, m 5 and m 7 are in current mirror configurations. So, I 6 is I 7 and also I 6 is I 7. So, I get W by L 7 is 8 times IDS 6 upon IDS 5 95 98 into this

Student: (Refer Time: 48:11).

So, I get a value of 30.65. So, nearest value is 30. Normally how much I should put 32, but I am not sure whether it will change vd sat how much. So, I kept 30 is that clear. m 5 and m 7 are a mirrors, but m 7 is now drawing 95 micro amps current m 5 is only drawing 25 micro amps current. So, the ratio of m 5 to m 7 should be 30. So, that it actually matches to plus into multiplied by value of the W by L a 5. So, it is 8 8 into this ratio is roughly 30.65 which is 30.

Now, I verify that whether vd sat is. So, I will substitute this value of in IDS 7, and evaluate vd sat for that that comes out to be 0.23. If I take it from vi sats, it becomes minus 2.0

Student: 2.

27, how much I respected minus 2. So, I am not worst of I am still better off. So, with this new calculation for W by L sats, I am actually improving the output swing remembers, what is the best thing you should have Vss to VDD, any amplifier output if it can swing from Vss to VDD is the ideal situation the minimum, if you can further go down to, ways is still better. So, nothing go the wrong, if I go below minus 2, because

you are actually expecting ideally full layer to layer, which probably may not happen, because saturation not, does this condition is trying to says device is still in saturation, even with this, this will still remain into saturation. So, good enough and you are improVing the layer margin or of the V out.

So, that is larger swing, there we increase beyond to, here we reduce normally sub that. So, very good. So, in some sense, we are getting better swings than what we are actually asked to do is, it the next value, what is that, what is right now sizes we have done except the biasing size.

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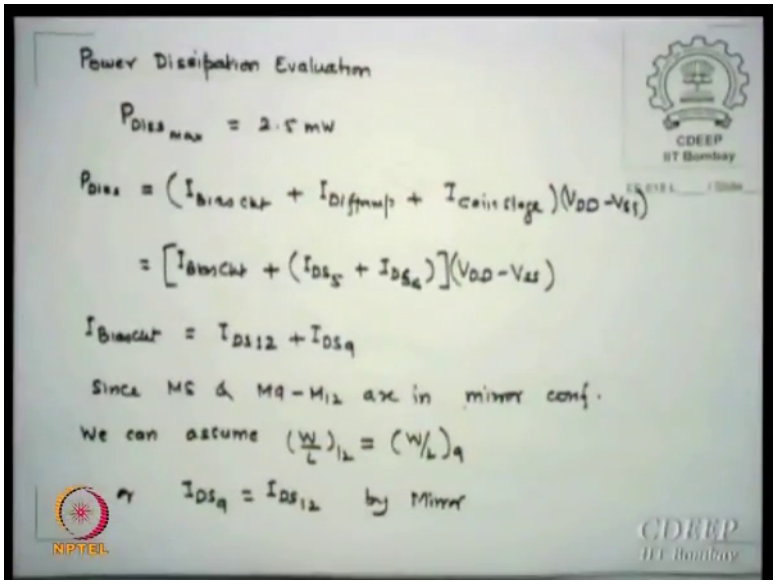

Now, what we do is, to calculate power keep now why are they are maximum. [FL] There are [FL] randomly [FL] 2.58 milli watt, does not matter what is the current flowing in this, how many arms. Please [FL] sir [FL] how much currents are fail one current in this arm, one current in this arm, and one current in this arm, and one current in this arm into VDD is the. So, I together, I will call it, because I am going to put equal, this values I says twice plus current due to I bias in to VDD plus current in this into VDD. So, that is the net power dissipation is that correct. Each arm current multiplied by VDD, some all of them; that is the net power dissipations

So, I said I bias circuit, plus I diff amp plus I gain stage into VDD minus Vss, because the swing is (Refer Time: 51:38). So, 5 volt. So, I find out I bias circuit I ds 5 plus I ds 6

into VDD minus vs I bias circuit is how much. I bias circuit is sum of this current plus sum of this current 9 and 12.

So, if I write that I 12 plus IDS 9, and now I assume the mirror is one to one, what to I shown.

Student: (Refer Time: 52:07).

M 1 m 9 m 12 are mirror one to one what is the current I, I want to. So, I said I can choose any current. So, I says is 5 is running 25, I will half it [FL]. So, I have chosen size 4 here, size 4 here, and how current each is drawing 12.5 micro amps.

So, if I do that by mirroring this, as I say these are my choice, you can choose any other value, because mirror does not matter any took, you can stand it 2 1 that ratio will change is that clear to you, where 12.5 [FL] W by L shift [FL]. So, in any value is, I have for the simplicity [FL] twice [FL] 4 [FL].

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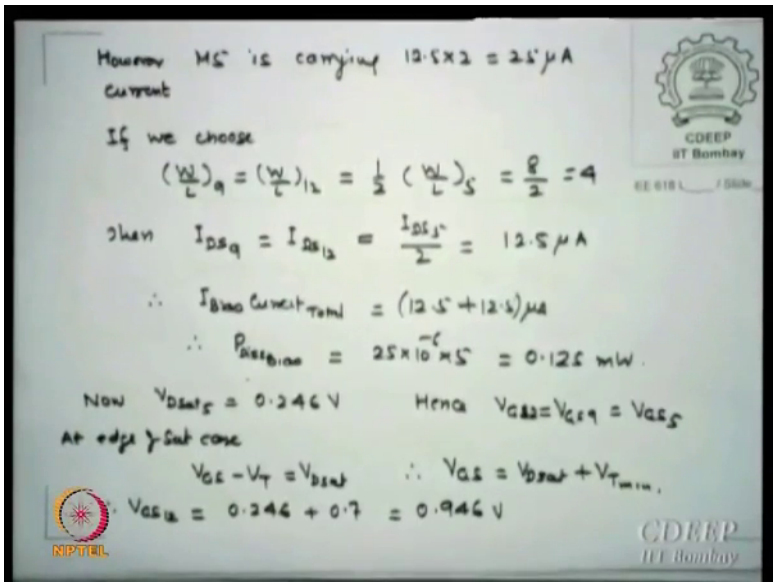

So, if I do this W by L minus same as W by L 12, because I kept them that way. So, each is drawing each is size of 4 and each is drawing half of this current, which is 12.5. So, the bias current total is 12.5 plus 12.5 into 5 which is 0.1 to 5 milliwatts, how much 125 microwatts. So, [FL]

Now, we also want to find the r value bias. [FL] Finally, find out if I know VGS for this, which is same as VGS for this. Then this value minus this voltage divided by 12.5 is r. please remember this voltage minus this voltage divided by r is 12.5. So, I did this, I have calculated resistance to be

Student: (Refer Time: 53:55).

VGS minus VT vd sat. So, for this value I calculate VGS 12 as 0.946 volt is that, this is the 0.246 which I got saturation voltage plus 0.7, which is the VT here. Also you can choose the worst cases, and figure out what should be the correct this. And for this I will calculate is that VGS. Please take it 5 9 12 are in mirror. The VGS are same that VDS also are same one of the vd sat 5 is known to me. So, I can evaluate vd sat for this current I know. So, I know this I rough, I know this voltage. If I know this voltage, this voltage minus Vss minus, this voltage divided by r is the current 12.5.

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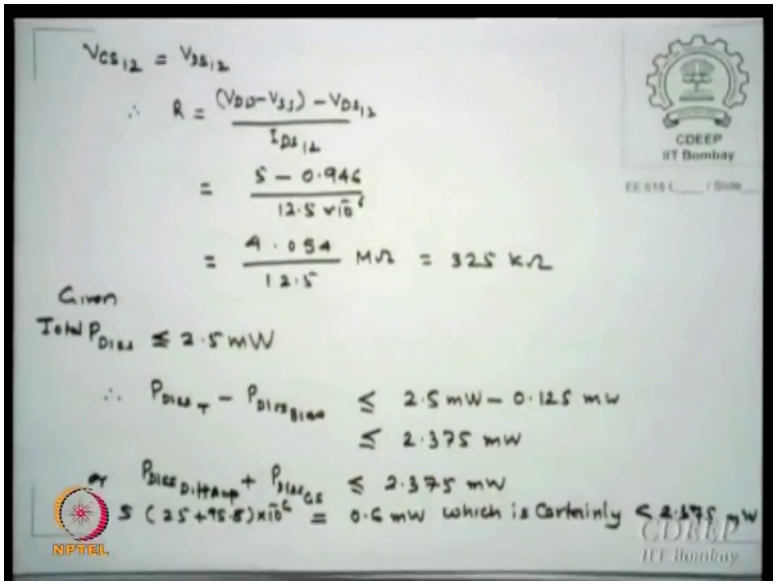

So, [FL] expression [FL] r is equal to VDD minus Vss minus VDS 12 into this, which gives me a value of 3 25 kilo ohms to get the currents are 12.5 micro amps. I need for this W by L are 4, I need a size of register of 3 25 kilo ohms bias [FL] power [FL] 0.125 available [FL] 2.5, the diff amp plus [FL] available a 2.375 milliwatts is still available for me for the limit for diff amp plus gain stage bias [FL]

Now, let us calculate the power for diff amp plus gain stage, how much is the current in diff amp.

Student: 25 micro amps.

25 micro amps how much is current in I 6 or I 795.8 micro amps multiplied by 5. You get this point 6 milliwatt [FL] 0.2125 [FL] it is 0.725 milliwatts which is one fourth of what was given to us. So, we us, given to W by Ls and currents, I chose and well within the power deception limits. So, what is the next, given we can play, you increase currents highest slew rate, you can done gain. It will calculate all values, have W by Ls and see whether still remaining saturation, but it satisfy conditions, better is that correct, because that at the end of the day, this may be sufficient, because low power is one of the major criteria. So, we are anyway achieving it.

But let us say you are, you suddenly say 20 micro ohm or a per microsecond you want, then probably you may boost the current, but recalculate everything again with this, new IDS 5 and do all read tell you satisfy again, your power and slew rate requirements keep doing as much as your wish, and at the end you will find some better optimal in some case, you may increase to 40 minus volt per microsecond; that is very high speed, but relatively low power compared to what limits you have given.

So, it depends on the spend given to, you may actually still play with IDS values IDS 5 is values, and if you play that value. Then please remember every other W by L will change, and then we will see with some time device [FL] vou t max Vin max [FL], then I find it become the other side. So, verify that those limits are also then modified by. So, you can get someone.

What is the last thing left for me to evaluate gain [FL] gain [FL] gain [FL], is it ok.

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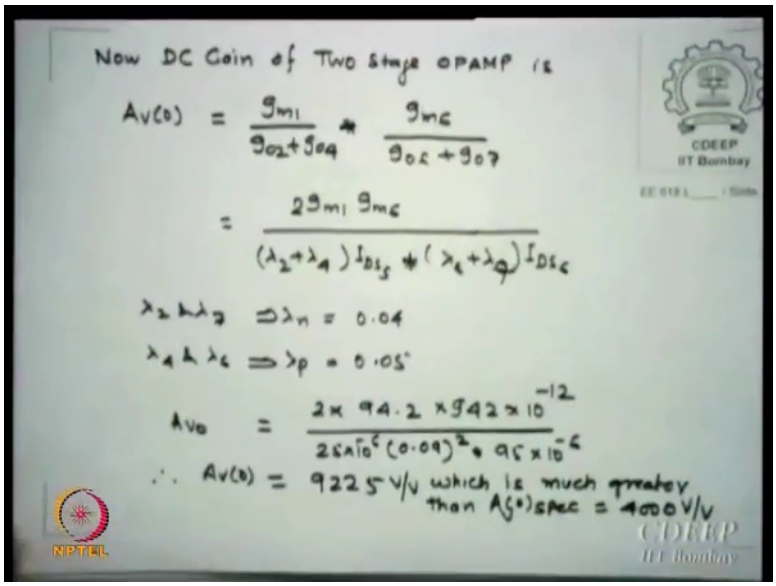

Which gain we are interested in the mid gain; that is the dc gain your expression [FL] gm 1 by, this is the total one upon ro 2 ro 2 parallel ro 4 is essentially by denominator go 2 plus go 4 gm 6 is go 6 plus go 7. So, if I multiply it becomes I think your [FL] 2 [FL]

Student: (Refer Time: 58:23).

Because current in each is IDS by 2. So, [FL] 2 or 4 [FL] same current [FL] IDS 5 by 2 is that clear 2 m 4 [FL] same current [FL] IDS by 2. So, [FL] [FL] this currents we are. Why I have, did all that, because current is, what is your specification currents IDS 5. So, [FL]

Now, given to me is for n channel, it is 0.04 for a p channel, it is point at length or equal to 1 micro amp, what is the length we are chosen.

Student: 0.8.

0.8. So, we believe that this is same this some, you are asking. You will increase the length, this lambda may go down is that clear to you, then we want to recalculate other things.

So, I know gm 1, I know gm 6, I know lambdas, I know IDS 5, I know IDS 6. So, I substitute 2 into 94.2 into 942 into 10 to power minus 6 into minus 6 minus 12, this is 0.09. So, this is and both are 0.9. So, 0.09 square this IDS is 25 micro amps IDS 6 is

95.8, but just put 95 micro amps. So, av 0 comes out to be 9000 225 volt per volt [FL] gain [FL] 9000 what do I expected.

Student: 4000.

4000, which is far away. So, might be a another gain. I do not want really this big gain. So, I can release this. So, I release the currents already if the size . So, now, keep, there are parameters which were in hand, keep playing, but every time you change something.

Student: free time.

[FL] there is no other way we can do this, but that is how what we do is, we go on one calculation, and submit it to spice, and believe that it knows better than me, and therefore, accept whatever they, that they say that is the way all of us. Actually believes here is that clear, [FL] you have to do, because gain is one of the major parameters of opamp is that correct.

So, no compromise can be made if this goes below the specified value. Unfortunately the way I did this simulation, which is what easiest to think in my this, and some books journals to also have given, this is not my original, I am not claiming it. I did it some many years ago, but it is not the, it is my original, I am copying indirectly from somewhere ok.

Right now, I am not saying it, but means I have done a times. So, I know this. Please remember this is the crucial factors we will have. What is the problem if I use this value, higher value, the bandwidth will go down. So, some limit there is a no. I want at least this much bandwidth, then I will I cannot play with this gain. So, I say [FL] bandwidth, [FL] gain bandwidth [FL]. So, [FL] [FL] limit [FL] bandwidth [FL] recycle [FL], this is how opamps are actually get designed. How many pages has suspend, you do not know all most 42, and they ask 4 more to show.

So, you can imagine the design is not very casual approach, design requires lot much thinking in lot much evaluations, and done hope for the best, and at the end of the day hope for the best is that clear. If you could have calculated first, you could have solved much of his worries, but right now, I did not know gm, I did not know 6, I did not know the gs that times. So, I could not do I, till have got all W by Ls, I cannot evaluate these.

When I evaluated that, I have already coming to an end size, then I started looking for gain, then I was hoping [FL] [FL] lambda values [FL]. Now you think of it, this the issue which I am saying is the most crucial. Let us say lambdas are equal. So, this is 2 lambda, this is 2 lambda, that is lambda square terms ria.

So, any change in lambda square [FL] you got, it is that any change in lambda 0.4[FL] 0.02 [FL] 4 times [FL] [FL] [FL] lambda value [FL] casual [FL], is it should be clear. If I just half it, I am a figure it out that I am I do not get the gain even. So, therefore, this evaluation of lambda from the spice file is a very crucial factor at every length [FL] IDS VDS plot [FL] high [FL] use [FL] is that clear to you.

So, that is something which any designer must first do. These data has been chosen from a normal known values. So, they came correct, but in case they are not actually, you must evaluate is that clear plot for given sizes, that you have various W by L size [FL] IDS VDS [FL] [FL] lookup table, [FL] and then when it comes picked up from there . So, that is the actual design things grow

Last, but not the least part in this, before we finally, go and which I am not calculating. Right now I am just showing you, this is also.

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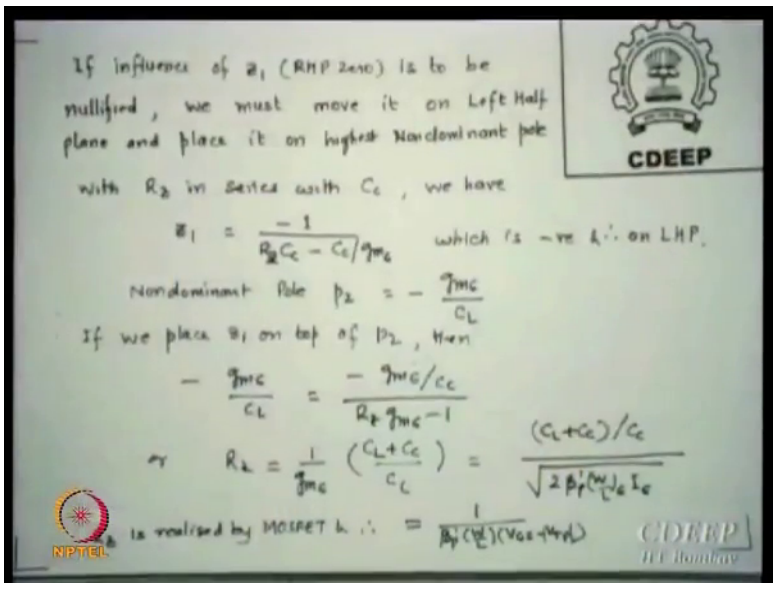


Now, old slide, and I am just reputing to you one of the technique, which we use in this design, was splitting up the poles. What is the method I use? I put a mirror capacitance

and compensated. So, what did I compensate? The non dominant pole was shifted far away by so much factor. Whereas, the dominant pole came closer towards the other side, and then I am worried whether my bandwidth is or not

So, one other technique is that, why not compensate the non dominant pole itself, since you have a zero. So, if I am instead of just capacitance, I put in series. This circuit figure if I have, maybe I can show you something here instead of this, I should use something like this. This is my r, this is my cc. Please remember this r is created by bias something here call V a a [FL]. No one is telling, it should be in saturation or non saturation. What is the choice you have to do, is r from that if r is required from smaller choose, put such that it is in non saturation. If r required is higher, go for saturation is that clear.

So, I do not want to specify what va. From where this va I can get.

Student: (Refer Time: 60:06).

That bias circuit [FL] [FL] voltage [FL]. Once that voltage is known, you fix that voltage here, connect here. Once you connect here, this r is known to me, because this W by L I calculate for this, when that rc time constant is known. I have now new z z 1 which is minus 1 upon ra c C minus C cg m 6, which is negative on the left half plane. Please remember if rz is larger, only then this will go to left half plane, smaller the rz this made is dominant than this, and in that case it will become positives 0.

So, right half plane zero can be shifted to left half by increasing rz value is that clear to you. Just look at the zero, if I want to make this is the minus here. Anyway if this is smaller than, this will become positive. So, I have, I am on the right half plane. If I start increasing this value r z is that clear. This is minus, then this is minus or plus [FL] right half [FL] if this is larger than this, the pole is zero, is on left half plane

So, and then where that there should be value, I should put that z 1 equal to the p 2. So, I cancel that p 2 ones for all, because p 2 are necessary with this cc. So, I says cc. I do not want to increase too much is that clear. Now I say if that split has to be, then why split was necessary, because p 1 p 2 are very close. So, stabilative fire was an issue for me. So, I say [FL] if I have to remove that pole without splitting or small splitting, then I will be able to actually keep cc smaller is that clear to you. That is how I must remove the second pole, this is called nulling. So, bring the 0 exactly on the pole at that is p 2 value

which we have. So, p 2 is given to is minus gm 6 by 6, and if I equate this by this formula here, I get rz is equal to 1 upon gm 6 cl plus cc C 2. For example, [FL] C 2 [FL] C 2 [FL] load capacitance, in my this. This is as I said old slide. So, [FL] do not [FL]. So, rz gm 6 minus 1.

So, but I can now I know g m 6, but I evaluated. So, this is the expression. So, rz can be realized, once I give this rz value, then using this expression, if it in saturation on non saturate, the correct expression and evaluate rz for that, that rz value for that W by L evaluate. Put that value such that z 1 is exactly at p 2 is that clear. Once you nullified this non dominant pole the only pole with you is.

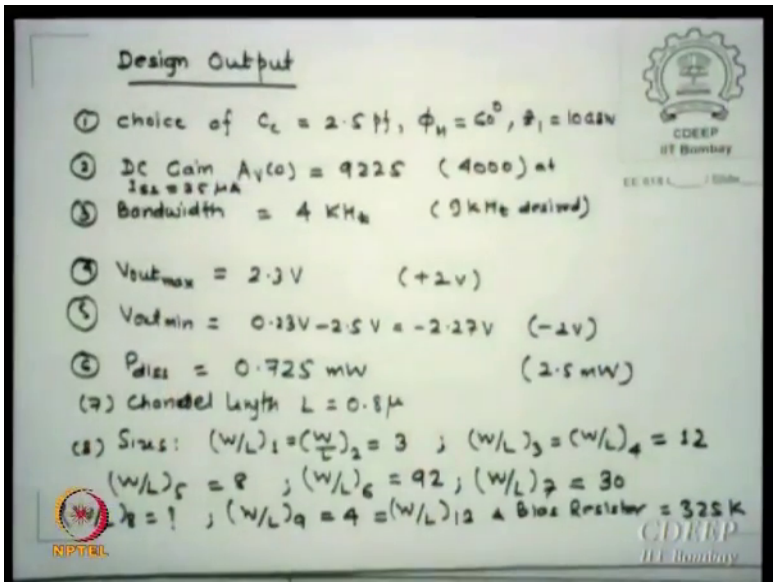
Student: P 1.

P 1 and that p 3 is still away. So, we are not carrying. So, only one single pole you have, which you can then think of what Cci should it, because. So, that it should not bit too close to 0 axis; that is the trick. So, rz allows you to do that is that clear to you. And then their bandwidth essentially is not directly heard by this method. So, to improve your bandwidth one way, is to null the non dominant pole, and keep cc to lower is that clear.

So, this method of nulling is very powerful. The only problem is what, is the only problem you will get. All these values are varying with all kinds of variations. So, getting this relationship is not very easy that they null. So, some, then still will occurred, but that still will be by, magnitude will be so small that it will not interfere p 1 in any sense, that is a trick of that. So, do not think exactly, you can null. Its very difficult, its high temperature [FL] change [FL] value [FL] change [FL]. They will not actually null it, but very close to null. So, we said, it does not affect you very much is that clear.

So, the end of the day [FL] output [FL] I had made a choice of 2.5 pair for a phi m of 60 and z 1 of 10 gbw.

(Refer Slide Time: 70:39)



This was my choice, either designer we all chose to choose this is that clear. This 60 degree is my making, you choose 70, you choose 50 55 your choice. We choose 10 times, 50 times. I already given with table, how much they, what values it will shift the dc gain is 9225 at 25 micro amps of current, expected was only 4000 rather 4000. So, we are already achieved that bandwidth, because of this larger gain, how much is the bandwidth gain 4 kilo hertz. So, very low bandwidth opamp we are received, not even megahertz. The reason is our gain bandwidth itself. We chose very smaller 6 megahertz is that clear. If your gain bandwidth point is here. So, the slope if you put it by so, much gain p 1 will be very small anyway. So, then adjust that values. So, that your bandwidths are higher.

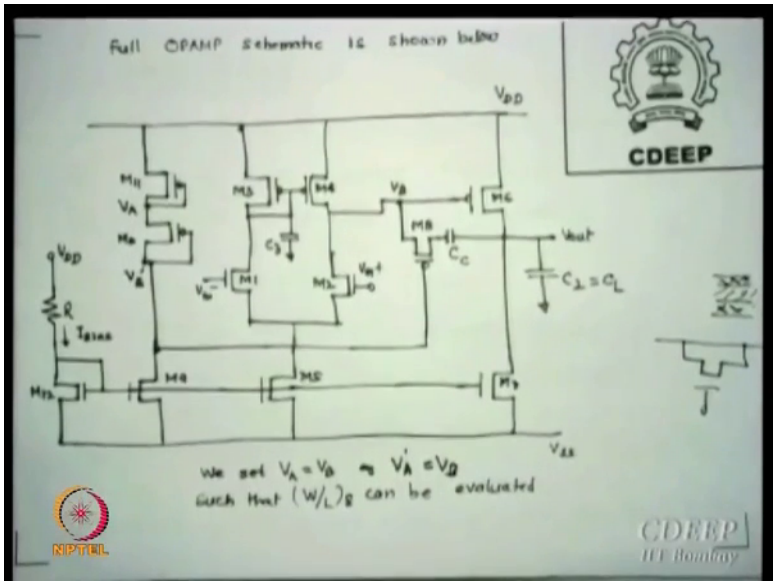
Further, reduction is cc, because you are improving p 2. So, you actually even more left side p 1 became even lower. So, that cc can then help you in the rz. So, that you can still maintain little higher p 1 value V out maximum is 2.3 expected about to V out minimum, expected was minus 2. So, you have minus 2.27 p dissipation 0.725, we are expecting less than 2.5, and one third of it, or one for most one third of it

Channel length used by me is 0.8, and the W by Ls size I got its 1 and 2 are 3 3 and 4 are 12 5 is 8 6 is 92 7 is 38 we are not calculated, because I do not know for those value of how much rz I need, because for a given p 2, I will have to do that for a given cc. Find p 2 and then such get that value of. So, I will right now put it question mark 9 is 4 12 is 4. I

also did not talk about 10 and 11, what are those values, how much vo vv you want that may decide there W by Ls drop across them

And the bias resistor use in my analysis is 325 kilo ohms. So, do you agree that whatever specks given to me, I have achieved almost every one of them is that correct. almost every one of them. So; that means, I have design an opamp for given specifications.

(Refer Slide Time: 73:48)



Finally, this is that the circuit looks [FL] va dash vab va dash [FL] you can decides these values corresponding to adjust this value. So, that the transistor may remain in saturation or a non saturation, whichever you are looking for, and correspondingly create rz there. They have calculate W by L here, W by L here, W by L here, W by L here, W by L here, W by L here, W by L here, here, here, here . So, I am able to evaluate every size of a given transistor for given specification of my choice is that clear to you ok

Student: sir who was cc also need to (Refer Time: 74:33).

Cc is the variable, cc is not going to me is that clear to you cc, I will make a choice form the, for phase margin I choose. So, is

Student: If circuit I need to put theirs (Refer Time:74:51).

[FL] cc [FL]

Student: [FL] implement [FL].

[FL] no, that was not be equal to cgds values, it is the much higher not 2 power 5 [FL] parasitic [FL] femtos [FL] you got it. So, that value physically, you will have to put, you have to create a mass capacitor right, there how do you keep a mass capacitor; [FL] therefore, mass capacitor [FL] got it. So, [FL] connect [FL] or [FL] or [FL] VGS a capacitance [FL]

So, you actually creates cc by a mass capacitor. Please remember the only thing this voltage is also very important, because the cc will be function of this voltage in [FL] capacitance is oxide thickness [FL] size [FL] that will decide the. This should make any inversion , and it should also in the size of cc, you are looking for per unit area. So, W by L you have to adjust for this value, as well to get the cc value. And please I am telling you it is not small capacitor, it is very large capacitor and much of the area in chip is actually taken by ccs transistor [FL] capacitor [FL] [FL] circuit [FL], does the value kind of values you get is that clear to you.

So, please do not take another capacitor you can make, but that is very difficult, because if you have a technology which is called poly oxide. Sorry yeah poly, yeah oxide or [FL] poly, its called pop. If you have more than one layer of oxides available, and double poly process, then you can create poly oxide poly or at times metal oxide poly

So, do not use substrate, use the upper lower of poly value, and use another capacitor on that. The advantage there is these are independent of biases is that clear. These are like the standard capacitors, additional mask [FL], but if the technology has that, then no additional mask, because that process is anyway sitting there additionally if you do anything additional money, [FL] additional money [FL] [FL]. So, generally in most capacitors in rf circuits or always of this kind

Student: (Refer Time: 77:42) separated/

Because, there Clc is so strictly, see, I need no variations I tolerate. So, I will use double poly processors. So, that I can get this capacitors of my choice ok

Student: (Refer Time:77:54).

So, please take it that its not the this technology, but rf technology is not same as analog technology, [FL] [FL] big signal technology [FL] available [FL] do there, definitely do

it. So, next time when you come, we will start of ICMR. Again verify those issues today is already up.