CMOS Analog VLSI Design
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Lecture - 19
OPAMP Design

We want to design an may be at

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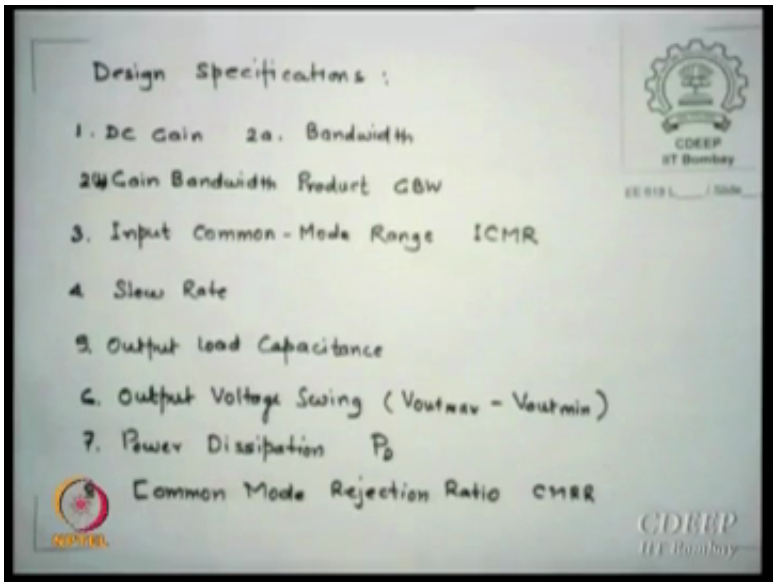

Least minimum may be necessary for example, many times CMRR is not specified because one believes for the gains we talked about bandwidth if we talk CMRR will match requirements. But if not you evaluate and figure it out. I again repeat for those who need not make any mistake DC again had nothing to do with the DC. So, A v 0 mid band gain ok.

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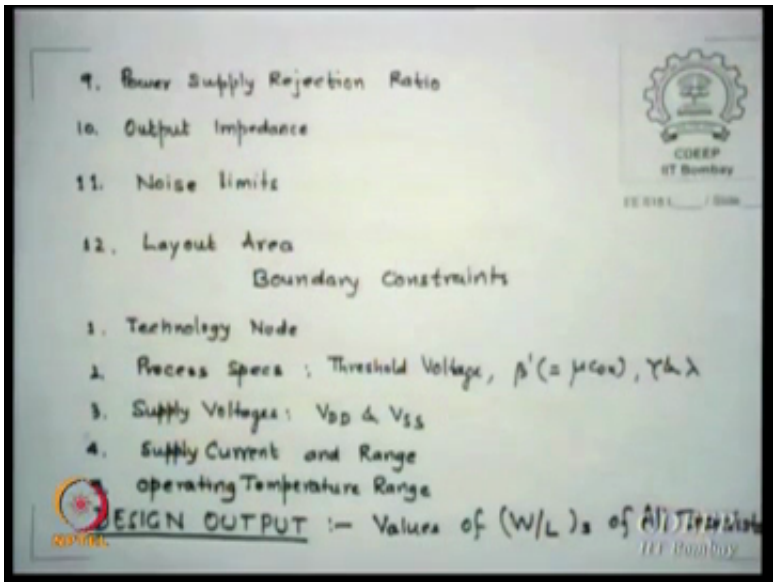

Do I move the other parameters to worry about in design our power supply rejection ratio PSRR. The output impedance some instances specified, this is something very important. In fact, in some larger circuit that impedance matching for the power transfer is very relevant. So, sometimes they do specify output impedance, then one of the major worries which most amplifiers or any analog circuit very is worried about is the noise limits and.

They really valued independently noise, we will have after this ah after design we will discuss noise. Noise a very interesting noisy area. So, it is fun to know about noise, and one who does not understand noise makes noise. So, I am the one. So, layout; layout area is also one of the constraint, essentially it comes from the technology node you choose and the area if it is a op amp is a part of a digital analog make circuit, then some area is specified for you this is the area. Then you have to fit in somewhere all of it what they want. So, layout area is for sometimes the limits, then there are constraints which I call boundary constraints. For example, any design you choose the silicon chip if you have to fabricate the design which will do it on a specific technology node.

Because if you are being spies at any cadence simulations including layouts including schematic and everything, you want to specify node because only then you will get technology file. So, first thing you have to decide this chip is to be designed on what node. And I will keep saying if you are 100 percent analog chip, do not go beyond 180 or below 1.18 microns. Everything is working well with 180 nanometers and things will

start deteriorating as you cross 100 nanometer down. So, if you are only looking for analog blocks or analog block, then always prefer 0.25 micron as the best of technologies cheaper these days by cost therefore, most of the chips which IIT Bombay students do it only on 0.25 there is per mm square cost is the minimum right now. 0.1 at it is 1.8 times of 0.25.

So, [FL]. So, the same area to that is the worry. So, node is the first thing you have design decide with as I said typically my data from the books which I am using they have a 0.8 micron data spice file. So, it does not mean that one cannot design it any other of this. You need actual data from the spice file whichever node you are using. Since I have copied it from the given book, they have a 0.8 spice file, which I am just using for my calculations. Your second worry for the boundary constraints come from the threshold voltage available for that node, and what is the beta dash value that is what is the mobility one gets. This is one of the data spice file specifies mu and of course, they also specify oxide thickness.

So, mu cox is known fourth for n channel and p channel because mu one and mu p are separate. So, you will get beta n dash and beta p dash. You also up to know something about the substrate bias parameter is gamma, and also the saturation parameter lambda. Now you will also see that some data which are given lambda also is a function of lengths. So, at what lengths you are working even if node is anything, you must figure out what is lambda there. So, generally spice allows you to know a different lambda values at different lengths. Then you have to specify VDD VSS. Typically technology node almost decides for you what is your VDD and VSS, but its not compulsory, I can have any requirements I can create on chip the other biases and can work if necessary.

But typically one does not want to do that we use whatever is given. For the node for the 0.8 microns 5 4 total supplies required. So, they generally will make VDD 2.5, VSS minus 2.5. So, that the total swing is 5 volts. Supply current and the range there is a maximum current which chip can use under this you know go it will start heating. So, the I max is also sometime provided, which is not the current you will use in any analysis, but it is the it never should exceed that value. So, it is called supply current, also kind of resistances it assumes which means what the power supply can it delivered this please remember current can be delivered as per you may have 3 volt supply 5 volt supply, but the resistance down decide what current maximum it can draw. So, that therefore, they

specify for given voltage what max current you can draw from the supply so, that you have to know how much is available to you. And then finally, the operating temperature range your chip is going to operate. For all this giving specified these as well as given the most of the parameters design specs, you can design the op amp and when I say design my output is the W by L size of all the transistor in the chip, but once I get the transistor sizes, layout is relatively simple automation can be done and you will be able to actually design the chip. So, other output as far as the design course is concerned is the size; further I had many other thing they are important, but this is the output from our side that is the end for us.

So, as I said these are constraints these those aspects, we already seen this circuit I will repeat again slightly modified one not really modified only bias circuit has been added.

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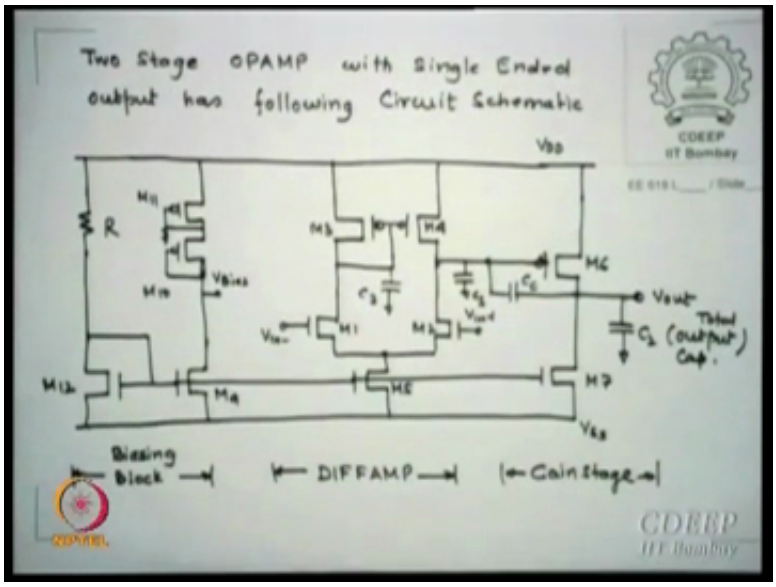

This is my single ended two stage diff amp plus gain stage, and this is the biasing circuit this R can be replaced by diode if necessary and. So, this is your actually current bias current you are creating, now many a times you need voltages let us say you want to bias with Vb. So, I put two diodes each will have some voltage drop. So, VDD minus that and will at this current what W by L issues, I can decide what drops it has. So, I can create A v bias of my choice I may put even 3.

So, but to know all that W by L for them I would need current and current comes from M 4 or a main sorry. You must be observing these are M 1 M 2 are the input stage M 3 M 4

are the current diode connected loads. The current is created out of M 5 from the mirror side. So, this is your ISS current going through M 5, this is the C 1 capacitance which we discussed and there is this feedback miller capacitance Cc, and then there is a gain stage M 6 M seven forms the gain stage, and the output capacitance which includes load. So, that is our seen now you must be finding out that somewhere I did not put some number which number I missed.

1, 2, 3, 4, 5, 6, 7, 9. So, 8 I miss. So, somewhere 8 is going to come. So, I will just left that right now additional resistance should be required, and we will see where they where that will come. So, one can find if you know VDD and you know the W by L we know from this what current is flowing through, this minus this divided by R is the current, VGS of this and these are same this is a current mirror. So, nothing great happens. So, whatever current is here can be transferred here, excess voltage is generally known for n channels for a given technology. So, use that. So, you can you will be able to get the currents in this arm and size wise it will give you whatever current you want in M 9. normally M 9 currents are same as M 12, and then increase ahead what are currents people are asking.

So, this basic mirror is not really great, but normally same sized voltage is created out of the diode drops, and to get this drop you know what you need current. So, you know this current is this. So, you can figure out what drops VDD minus that is your Vb. So, for example, tomorrow you want to bias this as a current source M 3 M 4, you can create the bias of your choice and actually connect there is that clear to you. So, why I use this? Because in case tomorrow you want double ended outputs and you have a current source biasing you can use one of the bias points to reach there. If you want very finicky about this, that this voltage is not very good what should I put them instead.

Student: (Refer Time: 10:16).

A band gap reference can be introduced there and that voltage can be used for even stricter control on Vb, but simply this is good enough in many cases. So, this is the circuit which we want to design.

Student: (Refer Time: 10:29).

No no no I just now said baba; in case tomorrow you want the current biasing and you need Vb. So, if the bias circuit is normally kept common for everyone there are who said wants you can pick up whatever he wants. This is general, in our case this whole R may not be there, we can directly you can leave M 9, M 10, M 11 full arm you can directly form for f arm this to M 5. So, its not that its necessary, but general biasing we do keep additional arm and there we actually use the same currents and figure out what bias I can create. So, is that clear to you I am I will not right now designed for you the value of M 10, M 11, M 9, 12 this can be independently handled as bias circuit, and we will not right now in our op amp design to first extend.

We will not design the mirror part, because which we can anyway independently design these are nothing to do with ahead. So, that can be independently designed, but just to show you that how much circuitry is essentially in an op amp is connected there you are right you have good question. But I just now said this is a general biasing scheme, we bias is not used by me, but tomorrow let us say I do not want diode connected load, and I want current source loads I need bias. So, I will use this. So, this is independently created and views whenever you want different bias you put different diodes is that clear? You can have another arm and put 3 diodes there or maybe 4 whatever it is and you can create different Vb values to actually suit your different circuit requirements wherever it goes.

But this is not redesigned it always comes once and you reused every time ok. So, this is my circuit which I want to design. So, I will like to design for given specifications you will now start the value of W by L for M 1, M 2, M 3, M 4, M 5, M6 and M seven this is what output of my design will be is that. So, this is what we are going to. So, on what specs we want to design? Everyone drawn the circuit. this morning only I have done accept that this part the rest circuit is same also. I showed you this CC is I have connected I knew it because I want stability anyway, I want to split. So, I am going to put it the value I may now choose how much actually that is the only thing. So, otherwise I will not go by CGD, I will actually put CC there is that. So, we go for these specs now.

These are arbitrary specs nothing very great, but typical specs and these are good enough specs in many requirements. You have a DC gain I want more than 4000 and I keep telling you that the values are not specified in design exact numbers no one says 4972 no one says. So, I want a gain DC gain which should be larger than 4000 ok.

Student: The product that do we mention what is.

They do no no if the design itself they will know how much for gain for op amp is designed for a gain value actually gain greater than something.

Student: (Refer Time: 13:53).

The reason is that that when you design a chip circuit with this op amp, we should only use 4000 that is called over design, it may be 4000, 5000 also is that correct. But not just that in during the design itself I go a any other value than 4000, because you the specs says that not less than 4000. So, I are now parameter which I can play this for some other takes to me, I figured out that A v 0 should be 4500. So, I will put 4500, because the design says it should not be less than 4000. So, I have meet there those specs anyway, but once I designed it, once I have got it those specs are fixed one chip is this done then its not change again and again, then effects you have the parameter to vary on.

Then the power supply is 2.5 VDD and minus 2.5 VSS. So, you have total currents are total swinger 5, I have a gain bandwidth our requirement is 6 megahertz then I have a load capacitance which is C 2 in our case which is 10 puff. So, all our capacitance plus CL all adds up to 10 puff they dont just go by CL its a total C 2 is 10 puff alternately you evaluate the without CL all the values by the formula we gave and add the external CL value and say that is C 2 now. So, that for the valuation right now sum number is chosen which is higher enough compared to others.

We are also told the minimum slew rate should be 10 volt per microsecond, that is the output voltage should rise in a microsecond up to 10 volts that is called slue rate. So, we are dv 0 by dv minimum required is 10 volt per microsecond. Then the output swing this is also interesting parameter, we want output to be though the power supply is 2.5 minus 2.5 the at least output swing between minus 2 and plus2. Then ICMR which is a common mode input common mode range V in max V in min. So, V in min is 1.15 slightly in order to correctly shown by it is 1.15 volt, you will be figuring out that if I have increase to 1.5 it will not be satisfying saturation. So, I first thought one point 5 then I looked at it I said is to put one extra there that is the way it is because I did not has spec somewhere. So, I just think and I say [FL] calculate [FL] [FL], but that gives me 0.35 shapes. So, that is good enough. And the maximum your v in maximum is 2 volts available to you. Power

dissipation p dissipation is less than two and half milliwatts, this includes power in the bias circuit and power in the diff amp and power in this.

Sometimes we may specify only in the diff amp and gain stage. So, right now as I say is bias circuit was not part of my design. So, this value does not include power coming from the bias, but in real life the power dissipation includes power in the bias circuit power in the diff amp circuit, power in the gain stage circuit, and in real op amp there will be a buffer stage, power in the buffer stage circuit which may be given higher. So, actual power dissipation is some of 4 arms, and that you have to use and then in the many ways you should start allocating how much arm I should give. So, that net is within this, and then try to adjust then keep varying which suits most of that is how its apportioned.

So, currents are apportioned each arm right. Now for us we have taken simpler issue. So, only two arms diff amp and so, I do not had a portion I will evaluate what current going to the other and therefore, I will be able to tell you what is the net power dissipation which I believe should be less than 2.5. So, it can be 2 volt, 1.5 volt it can be 1 milliwat sorry not volt is fantastic, but if you do this whether you reach this or whether you reach this you verify if that still satisfies fantastic lower the power better is the design. Another varies which is so far this morning we have been talking is whether the op amp design has good stability and that we must verify.

Essentially what that this means what phase margin I choose for relatively good stability? So, that is my design spec, I am deciding it what I am I should use. Design output gain for all 12 transistors I need to know W by Ls and node I am using is the reason why I have show that data which I will show you now is taken for this 0.8 microns CMOS is that. So, these are my specs, this is something I have believe I should know which I will fix and this something I will derive at the end. 2.5 VDD, two point minus 2.5 VSS is available for 0.8 microns 5 microns and a 5 volt swing all 0.8 analog circuits allow you for 2.5.

Actually higher the node higher is the voltage 0.8 is a almost close to 1. So, it is anyway higher actually why choose 5 because there is we are not using it, it is a short channel device. So, some effects are short channel are seen which in our calculation we will not use it spice wave take care of many of those parameters ok.

Student: Sir (Refer Time: 20:09).

It is a very question try it yourself for the sake of brevity, why people at all go for minus 2.5 or minus 2 plus, why dual Vd why not ground and VDD. So, there is something advantage I get by doing this they swing still I get 5. So, [FL] minus [FL].

Student: (Refer Time: 20:34).

[FL] next time [FL].

Student: (Refer Time: 20:35).

Um [FL] everyone no no not just these something he is said there is something to do with noise. So, I have gave you some noise on that. Unless always anolog circuits unless it is single ended power supply requirement comes some and a op amp do say only one otherwise you must see all op amp show two terminals that is the idea all general purpose will have VDD VSS. Only specific op amps which use only specific requirements they may use single ended power supplier. these are their pointed micron node spec taken from a spice file actually this was not 0.7, but I made it equal VTn is point seven and points seve minus point seven is VTP .

Another thing which I have not stated, but I will use in the which I now want to say the vts are there are actually vts are not specified as single values, they will specify or rather sometimes you may have to figure out in case they are not what is VT maximum and what is VT minimum. Now maximum values can made because of variation in process temperature, and also bias substrate bias if it goes through. So, VT varies with substrate bias, VT varies with variation in process, and VT varies with temperature.

So, in real life when we design a circuit we go for the bounds. So, we do use max and min values of vts and in this case it is found typically point 1 plus minus 0.15 volts is chosen as possible variation. So, for example, this may be 0.55 and the max maybe 0.85 why I need these values? Because your if you see their voltages ICMR. So, vo max or v minimum or v in minimum. So, at that time what maximum and minimum I should use out of VT which will guarantee may this min or max values. So, otherwise the W by L size will be very different from the real life. So, I just told you in a real life this delta on this is specified.

If not you have to actually generate by simulate [FL] 4 corners design [FL] to get out what max min you will get, but generally in course tell you what is the max min [FL] design [FL] feature [FL] design [FL] [FL] maximum peak [FL] . So, beta n dash is 110, 10 to power minus 6 amps per volt square and gamma for n channels gamma is the substrate bias factor which is 0.4, root volts root volt and beta p dash is 1510 to the power minus 6. So, we are roughly expecting 2.2 ratio of mobilities and gamma p is 0.57 per root not per root volt.

Then again this spice file if you see they say lambda and its 0.014 and 0.01 has lambda increase from 1 to 2. Similarly lambda p goes from 0.05 to 0.01, the link goes from one micron to two micron. So, each spice file will specify you, you see few model files and not necessarily in ng spice you have. But the level nines be shown now models will specify you, what max min it will go through other case. We choose one of the values and probably solve something, but in simulation wise should it should figure out what is it and should solve. So, I just gave you in real life.

These values are chosen by program and not by you it will actually pick up the value. 2 phi n since you are not calculating. So, I did not get c ox etcetera that also I should specify, c ox and everything, but I did not, but any how just Fermi potentials are given to you for n channel and p channel. We also wish to tell you that in most cases where the device is in saturation I will assume for calculation of VGS and by small and therefore, I use VGS is VT plus Vov or VT plus under root 2 ids by beta this is the expression I will use, accuracy probably is bit of lost, but if it is lower value it does not matter. So, if longer that is what I keep saying the longer length everything is fine shorter length all varies except something I said last time it helps you lot ok.

Is that specs you are written these are the process specs, which will be specified you and this is actually taken from a spice file for the 0.8 micron CMOS file. So, I have not added subtracted anything, which they have said if they are wrong the company which is manufacturing they are wrong data I do not have for me. It does not matter what value I get I will get instead of W by L 4 I may get sixteen out of that they wanted 16 I may get 4 for me how to get this more relevant. So, as of now, but with these specs which are standard I am told this should be relatively correct values we already done this morning the equivalent circuit using miller capacitance, the gm v 1 C 1 ro 2. So, C 1 C 2 we already specified what are those.

Now, please remember C 2 include CL or rather C 2 is CL or total; and we also believe that in diff amp M 1 and M 2 are identical that I was starting with diff amp because otherwise there will be a huge issues. So, M 1, M 2 identical. So, gm one is equal to gm two both W by L and thresholds are same for n channel transistor forming diff amps. Then we say M 9 to M 12 as I just now showed constitute the biasing circuitry the resistor r which could be a diode, for bias current controlled which right now as I say I am not designing which I can independently designed for you, but this is something which immediately I am not designing I am only designing diff amp stage and gain stage that w by l, but once I have know.

How about I want I can go back and figure out what I should push. So, how we know the data, we know the specs, we also know that it should be stable. So, all these things which I said have been known to me, I also decided the schematic that this is the circuit I want to design, right now I have chosen this in their life this is not specified. So, you may have to even decide in what circuit you should use, but generally single ended op amps single ended output stages are used diff amps are used for a normal gain stage op amp 741 and all series have single ended output the differential op amp as they is essentially two ended outputs ok.

So, right now we will not go into that, maybe we need it where there are issues something what op amp you are done in second year or third year I do not know where do you see analog lab second is not it there is one exam experiment we ask you to find out offset voltages. So, between the two inputs if I do not apply the output should be zero, but it not. So, you apply different some opposite. So, that we 0 goes down. So, one technique of offset cancellation is using a different system. So, that is why say its used many a times for an offset cancellation inside chip, not externally inside we will do something. So, their offsets are 0.

No one goes to the registers [FL] [FL] tune [FL] [FL] spot [FL] [FL] [FL] please remember what you can do on the board I cannot do anything on chip. So, you must plan everything fixed and then think it is still programmable. So, here is. So, let us start now. So, if I am. So, good if the first thing my worries are always for any amplifier is, how much stable it will be. And this morning I have with great fanfare said that as long as you have phase margins is 45 degree and up to 70 degree, we believe the op amp will or amplifier will remain stable. And I have explained it this morning enough that anything

lower or higher what it can create. So, therefore, this is typical range of phi M which I am going to use in design as a spec as a parameter is that clear.

So, I can choose 45 will I can choose 50, I can choose 55, I can choose 60, 65, 70 any of these values is within my control, I should decide oh 60 is good enough for me that is fair enough for you if you say no I want minimum 65, you take 65. If you choose different all the other values will correspondingly shift because that w by GB by P 1 P 2 will change. So, everything will change does not matter some other W by L will appear, but you must decide the margin for you. So, I have chosen these 3 values for initial calculations the final design is for 60, but I will just show you how much variation the poles will get if I choose 50, if I chose 60 or if I choose 70. Please take it even 75 is not out of question, but as I said it create some other problems and therefore, preferably keep to 70 for the given op amp circuit, since it is two stage with two capacitance and there is third capacitance will they calculate that value the C 3 which is further diff amp side can you before I tell you write down, can you quickly tell me what will be the pole there the sheet.

Student: (Refer Time: 30:58).

No no this you write down, then I will tell you what the C 3 capacitance which is coming there will may give you a pole and a 0, C3 is in the diff amp inside that is at the M 3 M 4 stage there is a capacitance look at this n 3 M 4 has CGS sitting there na.

Student: (Refer Time: 31:14).

So, that that may create a pole and also 0 because it in a feedback. So, it may have a pole and a 0 what is the criteria? The criteria is because of this the values which you are going to get, if they are larger than say 100 times or 500 times a gain bandwidth value, then I say it is dam care. Otherwise you will have to worry about what is the third pole is going to give 99 percent or 99.99 percent the CGS values are so small, that typically for example, 6 megahertz we are asking gain bandwidth, I have value it at probably I do not know we have reach there today, it will be around 900 megawatts will come as your volt frequency.

So, 900 megahertz for a 6 megahertz gain bandwidth far far far away. So, when by the time 900 megahertz frequency comes, the gain will have gone to some 1000 dBm dB

minus 1000 dB kind of thing. So, we are least worried about such poles and zeros; however, this is not to be taken without just seeing evaluate figure it out if its comes fair enough if not think of it what do I do now.

Student: Sir you to be read it out from technology (Refer Time: 32:37).

CGS is given from technologies, spice file gives you all capacitances, spice file gives you everything. Currents are decided by you say gm you get it, and gm by CGS you have to value it. So, that the pole you have to figure it out, I show you value you of calculation of that for a given beta the given values and the way I have calculated it around 930 megahertz . So, which is far away in my opinion, but I will check again [FL] mistake [FL], but I hope so, it is normally no one takes, so obviously, must be right we know phase margin since 180 minus tan inverse omega by P 1 minus tan inverse omega by 2 and this morning issued tan plus tan inverse z by 1 by w, but when it goes the other side it becomes tan inverse z by w by z 1. So, and you know I again I think I am making same mistake again, and again this is only phi and phi M will become when omega is gain bandwidth value. So, phi M is 180 minus tan inverse GB w by P 1 minus tan inverse GB w by P 2 minus tan inverse GB w by z 1. We also said this morning that typically we expect the 0 this morning we have plot, the sigma j omega excess plots and we have seen that if 0 should be on the right half plane and as far away as possible from GBw is that clear what is the criteria you said then.

Because by the time 0 appears, the gain should have fallen much larger in negative values. If minus 100 dB you add 20 dB it does not matter, but minus 20 dB if it adds it becomes 0 dB. So, that may create face issues is that clear. So, we already said the 0 should be quite far away from the gain bandwidth value how much we will check tentatively we can say 10 times, the gain bandwidth times 10 is what the 0 could be, but I have solved for all 4 cases for possible cases. So, 0 is that the frequency which is 10 times the GBw, this ensures the 0 occurs only when due to both poles gain falls to minus 42 decade around hundred dB minus 100 dB and band 0 appears. That is as long as it goes to large minus this it does not influence. So, this is now what we can do what is the what we can start choosing phi m. So, how many of phi ms I have chosen?

Student: (Refer Time: 35:31).

3 values. So, I will evaluate for 3 values this, this, this and I also know some 4 5 values for z 1. So, combination [FL]. So, I did this calculation I will show you. So, what I will get from there is interesting to me everyone has written down please note down [FL] [FL]. So, is that this statement is that I am having 3 values of phi M and I will also choose different value of Z 1 and figure it out.

What is the value of P 1 P 2 let us see what is P 1 P 2 will be come soon is that everyone has written down that is a case of phi M 60 degrees. So, see. So, this is also 180 degrees if I am not put zeros degrees put everywhere degree as long as I might have miss some places. So, 60 degree is equal to 180 minus GBw by P 1 this is the expression, which we are going to use now we see that A v 0 is 4000 is that correct.

So, what is P 1 the bandwidth. So, what is gain bandwidth? P 1 into A v 0 is that clear. Gain into bandwidth know. So, gain bandwidth is gain is 4000 minimum, plus bandwidth of P 1. So, gain bandwidth divided by P 1 is A v 0 is that correct. So, A v 0. Now if I take tan inverse or gain bandwidth by P 1 I am essentially saying take tan inverse of A v 0 is that correct and A v 0 is order of 10 to power 4. So, tan inverse 10 to power [FL] 90 degree its like infinite. So, 90 degree [FL] term [FL]. So, [FL] this term is taken care. So, now, we say let us say.

Now, z is chosen as 10 times the gain bandwidth. So, if I choose that then I said tan inverse this by this is tan inverse 0.1, which is 5.7 degree by my calculator hopefully it is correct. So, I got now 120 degree is equal to 90 degree plus tan inverse gain bandwidth by P 2 plus 5.7 is that correct. I substituted this and I substituted this and I substituted this. So, I got this. So, what do I get therefore, tan inverse GBw by P 2 I got now everyone has written down. P_lease write down this expression this is what we are going to [FL] 30 [FL] 5.7 [FL] 24.3. So, tan inverse GBw by P 2 is 24.3.

So, [FL] tan [FL]. So, GBw by P 2 [FL] everyone noted down . So, now, we are getting some feel how many calculations you need to really still there is no where we have closed to W by L we are just struggling to these there you know. So, I got GBw by P 2 is tan tan or 24.3 which is 0.45. So, 1 4 5 4 5 [FL] that roughly 0.45 [FL] inverse [FL] 2.2 [FL] [FL] x 1 [FL] 2.2 [FL] [FL] decimal [FL].

So, now we are many option one is why we chose 4000 we can choose higher, but as far as tan inverse comes, it does not matter because [FL] 90 [FL]. So, [FL] value [FL]. So,

that it does not matter for me as for as tan inverse A v 0 is concern 4000 or 5000 or 8000 it does not matter, but you can still have a choice now which you may use later. So, its not necessary or we are not worried now how much should be vary it can be anything 4000 you say limit is enough for me. Now we can also say Z 1 can be any other value why 10. So, or many other values I said why I have actually gone up to 100 times GBw. So, I say 5 times, 10 times, 20 times, 50 times,100 times distance away from 0. So, I have many values of Z 1 which I can use which is in my control I can decide what value I should push I have 3 values of 5 amp. So, I have 50, 60 and 70. So, I have 3 values of this and let us say I choose 5 Z 1 try a table of 15. So, I have 5 Z 1 values 3 fa phi M values and then I can calculate this P 2 for any one of them.

Is that clear to you what is the technique I am following. So, this is essentially let us say for example, if I use 0.05 sorry it is hundred this is how much? 105 is 1 by 20 mega like this, this will come 0.51. So, you keep changing the Z 1 value and correspondingly this term will keep changing and I will have a table to show you that. So, you get design word now that we have options means you are designing you are trying to fit what you want is that everyone. So, I did this calculation for you since I added calculators I did, the P 2 will be 1.47 GB if I use 10 points 1.31 gain bandwidth if it is 50, 1.8 5 it is 5 times and 1.19 in to GB, if it is 100 times the gain build. All that it will tan inverse that z by w changes. So, I subtract and again then I figure out what is the tan of that and then I get these values. So, you can see z can be between 100 this and this. So, pole can vary why I am interested in pole 2, the phi M was decided by pole 2 and from the phi M only I am now getting that value of pole, which satisfies my phi M by making a choice of Z 1 which I have 5 choices to make. So, from 1.8 5 to 1.19 times gain bandwidth and vary if I change the 0 from 5 times to 100 times, but you can see even if I change very drastically these values are not really changing as much is that clear .

So, typically if 10 time 20 time should be good enough in most cases, but just to get an idea that even if I go 100 times too far what values I am going to get. So, I just did evaluation for you everyone. If I do it for 50 instead of this I can get 130, now the first term will be 90 and again this can be Z 1, Z 2, Z 3, Z 4, Z 5. So, correspondingly I can calculate the value of P 2 for this phase margin for 5 values of Z 1, Z 2,Z 3, Z 4, Z 5 So, I did it for 60 degree, I now I am showing you for 50 degree and finally, I will do it for 70 degree. So, you will find that.

This does not very much changes very much, but something else changes because something because of larger phase margin, gm maybe the different or the CC values which you choose may be different and that may create further problems in some other poles 3 8 for example,. So, do not think that the small change means, small change somewhere maybe one 10 times somewhere else. So, decision is how much have you anytime seen and data book for any specific gain, they say typical minimum maximum 60degree is typical. So, we will do with 50, 70 can be min max ok has anyone noted down P 2 GBw by it can be 0.7, 6.6, 0.84, 0.54 depends on the Z 1 values I choose. If I use this 70 degree as phase margin. So, 180 minus this.

Student: (Refer Time: 44:28).

If I will subtract with 100 10 this will be ninety. So, 20 minus this and I calculated for 5 values of Z 1 again, and figured out the ratio of gain bandwidth to P 2 to as 0.2, 0.25, 0.536. You write down this of course, these are not vary relevant number just to show you if I am a designer you can do in simulation everything is fine, but when you are not doing simulation or rather when use to want to start simulation, first get hold of what around what you should simulate. Otherwise too many specification too many parameters to handle it, it can go haywire. So, do not try the chips.

Student: (Refer Time: 45:19).

So, here is the table which I created.

Student: (Refer Time: 45:21).

Phase margin 4 values of Z 1 and correspondingly P 2 values with response to this all that calculations which I showed you earlier are summarized in this table. Again even write a small program and just continuous value changes everything can be printed in 15 minutes end [FL] time [FL] there is no tangential equation, there is no second order equation, there is no non-linearity simple calculations.

Student: (Refer Time: 45:51).

Problem [FL] dn by dt is dg by dx time.

Student: (Refer Time: 45:56).

Space variance continued equation [FL] problem [FL] time frame [FL] case frame [FL] [FL] solve [FL] [FL] phi ms equation rho by epsilon [FL] add [FL].

Non linearly [FL] then that requires, numerical is that table is written down later this table does not give you a any great information, it is only trying to tell you how things change if I changed phi M or Z 1. So, I can actually evaluate for any phi M for in Z 1 what should be the size what should be your M I P 2 is that clear. Now we may have to try few of them in real design and check, but as I say I am going to do for 60 degree at 10 GB . So, one value I use, but I say I have access to.

Student: (Refer Time: 46:52).

Any value of this kind and I can still start design out you can see roughly except this first one almost everyone is around 2. So, it is not that it is changing drastically in great numbers. So, its, but in this it may change if you go from 50 to 70 things change. But on the same phase with margin is not that great change. So, you can choose 10, 20 is whatever you choose is that. So, having done this we now state the case typical value of phi M equal to 60 and Z 1 of 10 times the gain bandwidth. So, I got from this to from the table now.

Student: (Refer Time: 47:36).

The second pole is 2.2 in to gain bandwidth is that clear. Just now I got it. So, I say second pole should be 2.2 times that of.

Student: (Refer Time: 47:50).

Gain bandwidth for 0 has been adjusted to 10 times the gain bandwidth and phase margin chosen is 60 degree.

Student: (Refer Time: 47:58).

This morning I discussed. So, much about 60, Z 1 is the thing you have to fix because today I said right hand pole. We never worry, but now I am saying it that control also helps in design as many controls your get better for you because one will change drastically. So, the other can be used to not allow this to change drastically. So, as many parameters you hold that is better control for you.

Student: All right.

Away from the GBw point from 5 times to 100 times I checked, it I find 10 is normally good enough for my evaluation. So, I chose 10.

Student: (Refer Time: 48:40).

But you may start with 20 and get away not much will happen. So, for this case what is the P 2 pole we calculated from the expression gm 6 by C 2. Gm 6 by P 2 and typically I this value what does it say actually this say equal, what should it show? The pole should be larger than this value. So, that 60 degree is guaranteed for you is that correct. So, the minimum is equal 2, but anything above is also acceptable 2s . So, gm 6 by C 2 should be greater than 2.2 what is the gain bandwidth product? Gm one by CC. So, if you do this from this inequality.

I want CC should be greater than 2.2 gm one C 2 upon gm 6, what is the effort going on well this phase margin what is the value of CC I want to know. At least in terms of C 2, C 2 is given to me tenth of if I can get the ratio of this and if I know this, I know what should be the minimum value of C 2 I should hold is that what I am looking for the value of CC which will give me 60 degree plus phase margin, when I put 0 up 10 times the gain bandwidth. So, if I do this since I said that one is one 0 times the gain bandwidth z is gm 6 by CC and that should be greater than 10 times j gain bandwidth gm by CC, both CC please take it . So, gm 1 by g m 6 which less than 0.1 or.

Equal to 0.1 is that since these are this is the equality inequality gm one by g m 6 should be less than 0.1 or equal to point that is the possible. Now this value I can get this is specified for me. So, then what do I calculate? I can calculate CC value is that correct because that is one spec which I did not know how much to put cc. So, now, I have figure it out I can evaluate CC. If it is 5 times I get gm 1 by gm 2 should be less than point to 10 times, it is just now I calculate it should be 0.1 times . So, typically for 10 times gain bandwidth as z 1, the CC should be larger than 2.2 into 0.1 into C 2 put everything value here. So, CC should be greater than 0.2 to C 2 [FL] C 2 [FL] 10 puff C 2 given to us 10 puff. So, CC [FL] 2.2 puff [FL]; obviously, a 2.5 [FL] 3 [FL]. So, I know which is the minimum CC I must use. So, that 60 degree phase margin is guaranteed when I put my 0 at 10 times the gain bandwidth. So, one of the features of evaluation was [FL] W by L [FL] para [FL] CC [FL]. So, this fact has to be understood

by you that is most important part for you is to know what is the CC values. At designed what is it done in design then we may choose.

Student: (Refer Time: 52:23).

Value yourself 2.2 is the minimum, you may choose 2.5 you may choose 35, then you say 5 when to will happen. So, then you come 2.5 is that is what the design specs is trying to tell. Before I go to the actual evaluations, what is my figure of amplifier. Before I leave this before I start calculating W by Ls please remember I am now calculated this which is what I say is requirement for amplifier to be stable. Now I figure out that there is a C 3 capacitance sitting here which is essentially CGS related why CGS because of CGD is shorted this is the p channel device. So, do not say CGD [FL] CGD short [FL] [FL] CGS input per [FL]. Now if you want to see CGS or what you call there. So, are one pole which will come because of this resistance what is this resistance.

Student: 1 by (Refer Time: 53:34).

1 by gm 3 ok.

Student: (Refer Time: 53:36).

So, if I calculate the input pole for C 3 it is minus gn 3 by C 3 and if write expression for output to this I will get a 0 which is minus 2 gn 3 by C 3 . So, here a then what is the sign of 0 minus what is the sign of 0 pole minus. So, both are lying now on the left up plane. So, they are least valid because they may cancelled now if 20 dB [FL] ac [FL].

Student: (Refer Time: 54:16).

So, [FL] . So, essentially we will be may now say if my p 3 is much larger than P 1 P 2 and j 3 is also much larger than.

Student: (Refer Time: 54:23).

P 2 which I got it. In fact, as I say 900 odd megahertz then the use of this poles and zeroes is not of any relevance in further calculation though we may have to evaluate to verify, but just to tell you word from a verify just this substitution here I must get gm 3, I must get this value of CGS whatever I get and correspondingly evaluate these two and figure it out where is the poles and zeros going up and if that happens to be too far away

1000 times with band care about it. So, this is an issue which you must address they are where say if you do not where nothing was wrong in 99 cases, but as a designer I cannot accept anything without seeing it though my intention says it will not affect.

So, this is an important because we keep or talking we assign designing how do you create a right half plane 0 or left half plane shift it to 0 [FL] resistance [FL]. So, next time we will when we design we will try to see somewhere instead of c is should be RMC series of that. And once we get it much of this 0 on the right hand side can also be handled bias, that is the next stage which will have to do it right now I assume that without anything phi M 60 degrees achievable with whatever value is I attitude, but in case there is any issue further I may actually start looking that 0 also [FL] [FL] floor [FL].

Student: (Refer Time: 56:00).

[FL] [FL] cancel [FL] (( )) [FL] I do not want to increase CC that, I knew if I increase then I have more issues. So, I said CC I kept this now I bring this pole 0 on the pole and cancel it nulling the effect. So, we will do that, but before last slide I might like to show I just want to show you that there is another P 3 Z 3 available. But in most cases we never bother about them, but as a designer I thought we must show you that yeah there is a pole and 0 which you must evaluate and if it is extremely away forget it which will happen why it will happen because CGS is so, low the gm by CGS is.

Student: (Refer Time: 56:48).

Very very high frequency. So, do not worry too much.

Student: (Refer Time: 56:51).

Because CGS compared to other capacitors is very low everything is safer at least it will be like that.

Student: (Refer Time: 56:53).

Unless the size of that transistor is so big, that the CGS value boosts up and then that pole may come. So, if it is hundred [FL] of size [FL]. So, then you have to worry about

this pole is well pole 0 if I continue my design at least this sheet will finish and we will stop.

Student: (Refer Time: 57:09).

We say C 2 is given to 10 puff CC is taken to 0.2 to C2. So, we say CC should be greater than 2.2 puff. So, I can choose 2.5 puff I can choose 3 puffs I can you also choose 3.5 puffs if I need. I have calculated both for 2.5 why I chose because close to 2.2. So, I thought one value should be as close to this the other related away from it. So, that designer should actually evaluate both 3 is of course, not too close, but still a too far, but still.

Now, you look at this figure again in a gain that figure is very important you note down and then I will show you the figure and a requirement came CC should be better than 2.2 puff, and then I have a choice to make is it [FL]. When I will show the figure and come back you just right down think of this. Right now just forget this first only write down CC values are 2.5 43 puff one can choose even higher, but I have chosen only two to evaluate I will come back to it [FL] minute. So, what I see now this CC value is connected to the output of the diff amp stage is that correct. So, if this is to be charged faster ok.

That is slue rate for this, and I must see that the current which can allow this CC to get, the current is only provided from this arm is that correct. Now the maximum current which any of the arm can get is how much? When this is off this is on the maximum current which this can provide here.

Student: (Refer Time: 58:58).

Is only I 5 ids 5 is that correct to charge this is the only current available to you is that correct. Full of it because in midpoint it is half of, but the maximum possible is one current which is Issor ids 5 if I decide that that is CC dv 0 by dt because this is V 0. So, if I have to charge this capacitor by this current, the maximum current available to me is ids 5; that value I use and I say I was given the slue rate of dv 0 by dt is 10 volt for microsecond CC dv 0 by dt is ids 5 ids 5 is therefore, equal to c is 3 into 10 to power minus 12 3 puff into 10 into 10 to power 6 which is given dv 0 by dt, which is thirty micro amps or if I use 2.5.

It is 20 5 micro amps. So, the first parameter I need to know about gm 1 and 2 is.

Student: (Refer Time: 60:04).

I must get the current M 1 and M 2 is that clear. So, once I know ids 5 what is the gm value will be what current I will require half of this ISS by 2.

Student: (Refer Time: 60:15).

So, 25 by 2 or 30 by 2, I can use 2 evaluate gms which I will evaluate next time and then we start then we will start getting w bias. Once I get gm then I proportionately start getting widths and link ratios is that correct. So, the first parameter which gave got me closer to W by L came from where CC I chose from the phase margin, slue rate gain is one value of currents from where the other current value I can get.

Student: Power (Refer Time: 60:50).

Power dissipation is that correct the temperature is not even that can give me another limit; once I get my limits I may now say.

Student: (Refer Time: 61:00).

This say one 12.5 other says 15 or 20, I said fine 20 a higher current I will not choose because low power will be lower than that. So, I may choose this current, but let us say that becomes lower than this then I will choose that value and adjust this value what maximum CC I should. So, I will have to go back and change my.

Student: CC (Refer Time: 61:20).

Cc value to come back here is that lets say that current is smaller than this value, power is first. So, now, change CC to get to that is that clear. So, that is the design issue it will start.

Student: Sir.

So, means yes.

Student: Sir (Refer Time:61:36) this (Refer Time: 61:37) op amp for gain is ratio it was see (Refer Time: 61:38).

Because it is not op amp it is essentially V 0 is doing at the CC output. So, the output as the capacitors CC charges.

Student: Sir (Refer Time: 61:50) capacitance v two also.

But that is not actually charged by this current is charged by M 6 or M 5.

Student: (Refer Time: 61:55).

That is their limiting this ok.

Student: But (Refer Time: 61:59).

That that is the slue rate for the external where actually we will not use this we will actually put another buffer stage to drive that, this essentially slue rate is specified for the two stage op amp.

Student: (Refer Time: 62:11).

In which output node which is my M 6 and seven those how fast that CC allows current to come there, that is essentially caused slue rate for the two stage system. What we are saying op amp finally, is slue rate there will the third stage available, which anywhere is a bigger one and which is a push pull kind. So, it will dump huge currents.

Student: (Refer Time: 62:30).

Or it will remove the huge currents recharge. So, then that slue rate is not very important because I am actually dumping the currents heavily from the buffers. This is very important because this is going to create my next output for the push pull stage, and that I wish to know how much is that. So, these are the issues which we will discuss further as of now I have limit for CC charging because that is going to the output node, and that only can provide through the M n to M forearm which is the maximum current is ids five. So, that I charged see you then.