CMOS Analog VLSI Design
Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture - 17
Basics of CMOS OPAMP

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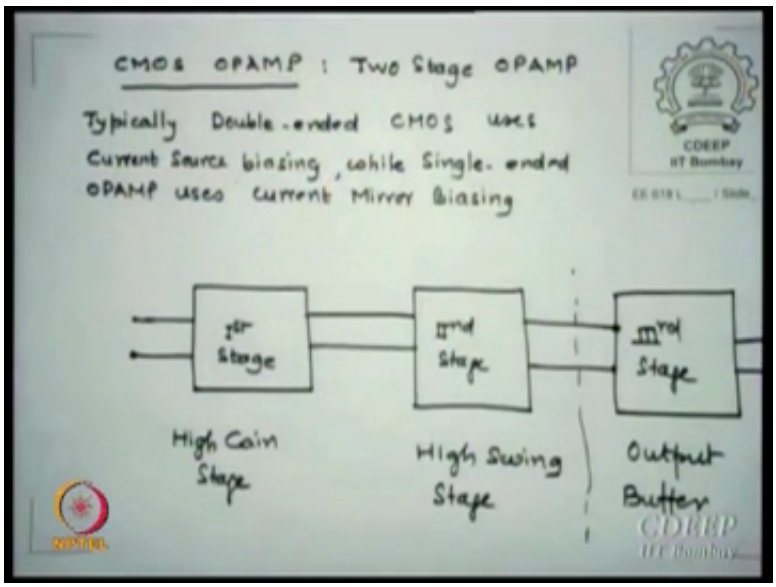

We are doing latest frequency response of amplifiers where we start with the first of the most important device of analog, which is an operational amplifier nicknamed short named OPAMP. We want to talk about of course I will show you a little later this is an a figure which I am showing you which is a sketch for two stage OPAMP. There is a possibility of third stage in real OPAMPs which is right now put dotted one. The first stage is essentially what we call high gain stage which is followed by another gain stage which is basically high swing stage. And then it is connected to buffers which is typically push pull types output amplifiers as they are called and that gives the output to you. Most OPAMPs used are single ended what does that mean the output is only at one output there are no differential two outputs.

But let us say if you wish to have two outputs, there are possibility then show I will show you one circuit which does that. So, CMOS OPAMP which is either double ended or single ended, normally if it is double ended you use current biasing current source biasing; and if you are using single ended OPAMP amp normally it is current mirrored

biasing. Normally, it is not necessary you can do any kinds of biasing, but normally it is done through current mirrors. This normal word should be taken seriously because not every circuit uses exactly the way I say individual requirements may push you to some other ones.

So, this is typically what you want to know. So, what is the first stage, second stage and third stage which allows you to do this kind of features high gain followed by high swings and then finally, the buffer out. Buffers are always required for driving larger loads and in the case of MOS circuits 99.99 they will be capacity loads. So, you are driving a large capacitor which may be the input capacitance of the next step or next state of the circuit. And like in the case of digital circuit, we typically expect the load at least four times the cox which is called four loads. So, even in this case at least whatever the highest capacitance you put 10 times cl, so that that becomes the maximum possible load, but in general in our design right now we will specify for what load this needs to be designed.

The features of OPAMP will discussed when we start designing OPAMP what exactly the parameters we are worried about like gain, (Refer Time: 03:11), bandwidth and what are what else, but you do some basic thinking on this.

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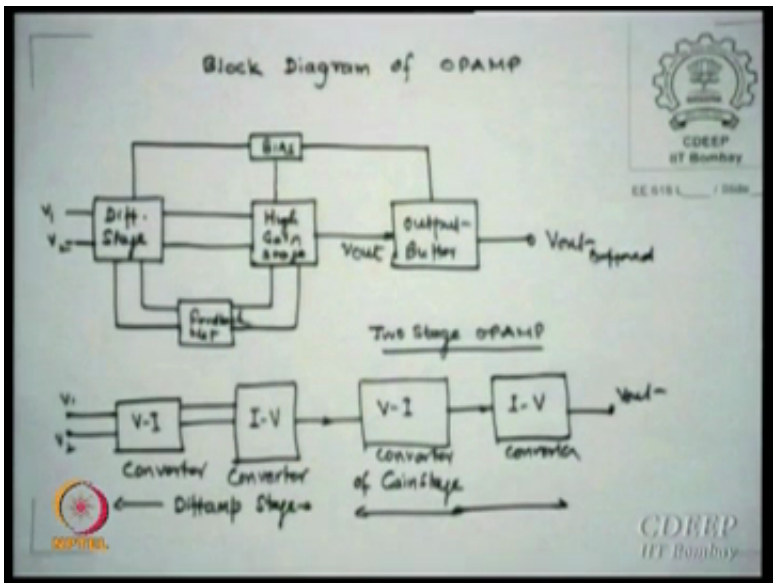

So, once I declare that I want a high gain stage the possibility of such high gain stage is either through a cascode amplifier, but it will be only generally single ended outputs and

require large power dissipations. So, we will go for diffamp. So, the first stage of a OPAMP is normally a differential amplifier or difference there is a word I keep saying differential amplifier or on a difference amplifier I will differentiate later, but it looks sometimes they are same, sometimes they are not. The difference amplifier is essentially outputs are also difference two outputs two inputs which are required in many filter organizations.

So, first stage is the diffamp which whose output can be single ended or can be double ended, and it is given to another stage which is normally high swing high gain stage. Most of the gain picked up here, the rest gain is picked up here plus swings are in group. Then there is a last stage which I am showing you buffer output buffer or this output amplifier typically it is push pull kind not necessarily everywhere, but take it normally it would be a push pull. What does push pull means, however, the top transistor will be on or the lower transistors will be on like a normal output stage of a any digital hardware, so that is, but the importance there is they can drive larger capacitance they can provide larger currents, yes.

Student: (Refer Time: 04:59).

It is a gain stage, but it gives you output swings V out max, V out min its picked up from there and not from the diff amp stage is that clear? Then in most OPAMPs for the case of stability or by without doing thinking over it there will be a feedback capacitance connected CGDs for example always there or other parasitic capacitance to may appear which may give you output to input connections at the at least the output stage this stage. And in that case you will have a feedback. Now, this feedback also creates feed forward.

So, in all our analysis, we try to avoid feed forward situations. What does feed forward can give you a zero. So, we are trying to see that zero does not appear at least in the range of frequencies where we wish to operate. Now, the feedback is what we few minutes we will discuss later, but if you see carefully this if you look at the diff amp, the first two transistors maybe here is may I put it new slide, there for the heck of it.

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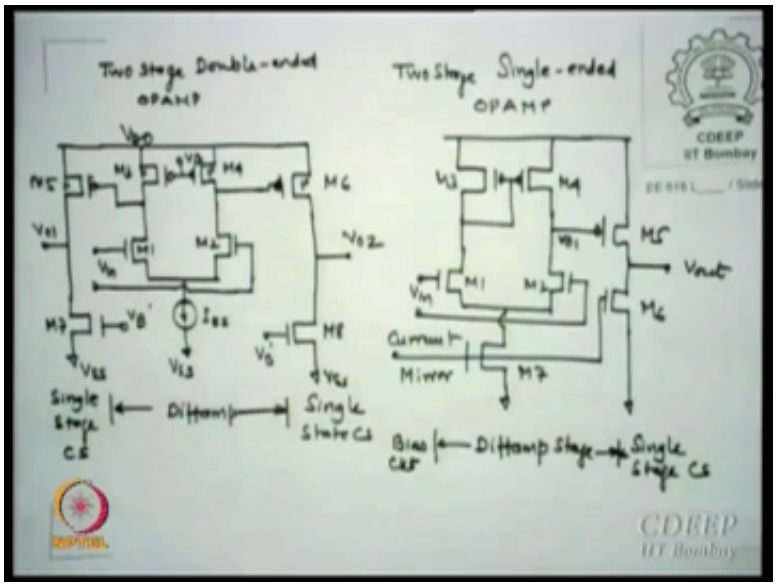

Let us look at either of them this M 1, M 2 receives input voltage and converts them into g m V 1 g m V 2 kind of currents. So, this is essentially called V 2 I converters. When these I's are fake to these they give an output which means current to voltage converter starts here is that clear. So, this block is or this block is V 2 I converter, this block is I 2 V converter.

So, this first two stages define as two parts one is the V 2 I converter part the other is why I am giving you these figures, because this is how one designs which area we are looking it ok. So, the first part is converter from V 2 I they are the I 2 v which together makes a diff amp followed by a gain stage like shown here or shown here now this gain stage you can see from here since this is an output M 5 is receiving VGS and therefore, converts currents. So, next stage of this is a V 2 I converter and that current passes through M 6. So, this will then give you I 2 V converter at this output.

So, a typical op amp two stage op amp has two V 2 I and two I 2 V converters is that point clear it is only a statement nothing very big just to tell you how fundamentally one should look the circuit from inside, is that ok? So, first is V 2 I then I 2 V then V 2 I then I 2 V this is a two stage op amp. The two possible of course, the many more, but these are the two most popular ones, which are used in OPAMP designs, this is the double-ended output, and this is a single ended output.

So, in this, this is your diffamp. Now, since it is not diode connected. So, normally current is not mirrored actually you apply through V v another transistor and create I ss, and you also bias this V BB these two make it current sources. So, (Refer Time: 08:34) W by L of the last transistor to suit this currents which is going to go down is that not the other way. The V B and W by L of this is so adjusted that the currents which I am receiving from the current source are essentially received at the I ss which you want to use as this is a design spec.

So, same this is from where V B I can create voltage difference preferably if you want a very nice table reference band gap reference or at least V T references. You can see it is a double ended, so one output is taken here one output is taken here and then you have two single stage output stages which is essentially the same one which is in the single end also. So, I can create a V o 1 and V o 2. And if I choose M 5, M 6 not identical, I will have V o 2 separate from V o 1s, is that clear? So, I have a double ended output of my choice which is proportional to input voltage V in, is that clear?

Please remember I can make a ratio of this, I can make a ratio of this. And can change the currents in this, and therefore V o 1 and V o 2 that is V 2 I and I 2 V converter can be modified to suit different V o 1 and different V o 2 for the same input V in, this is essentially double ended output. If all are equal then the V o 1 will be equal to V o 2 then you do not need that. If you are using same then why do you want to at times you still need to. In a layout, it is sometime preferred to have same output going other two sides, so you may as well use this, but that does not help too much because it consumes power for nothing.

So, this is the as I said not very often used, but if needed can be employed in many OPAMPs. There are specific OPAMPs which gives you double ended outputs, many of the LN series which is a low noise OPAMPs they are double ended outputs even 8576 is also double ended very famous low power low noise device. This is the one which is most of the 741 series 747 whatever 725, 723 whatever standard op amps you see in the labs they use a single ended outputs, a diff amp whose load is decided by diode connection we are loaded done analysis for this.

We also done this individually, so it is not that they are two different. So, it is only a question of load which you put there. And in these cases most times both this M 6, M 7 if

they are any other stage are driven through a current mirror the biasing is not shown here. So, there will be a biasing circuit, which will give you a current mirror and that same output is connected to a many transistors as you want to have same currents, is that correct? So, when I start looking into this design, all that I have to design is the W by Ls of this and W by Ls of this to meet specification.

What else I can design the size of M 7, which may design the R ss or R ss values because I can mirror whatever current I want is that clear? I do not have to M 7, M 6 same either I can have different M 6, M 7 it need arises normally I will not do that, but if I need I can do that, because I just have to make different W by Ls of this. The problem there is different how much will be decided about this because this is going to push the current.

So, it is not too much in your hand, is that ok? So, my end product is OPAMP will be given some specification to me; and all that I will design or I will get an output is sizes of all transistors that is what design is about. Because once I know the size we are not done layout maybe in between before we go details one class on the design layout maybe helpful just a minute, I will come back to it.

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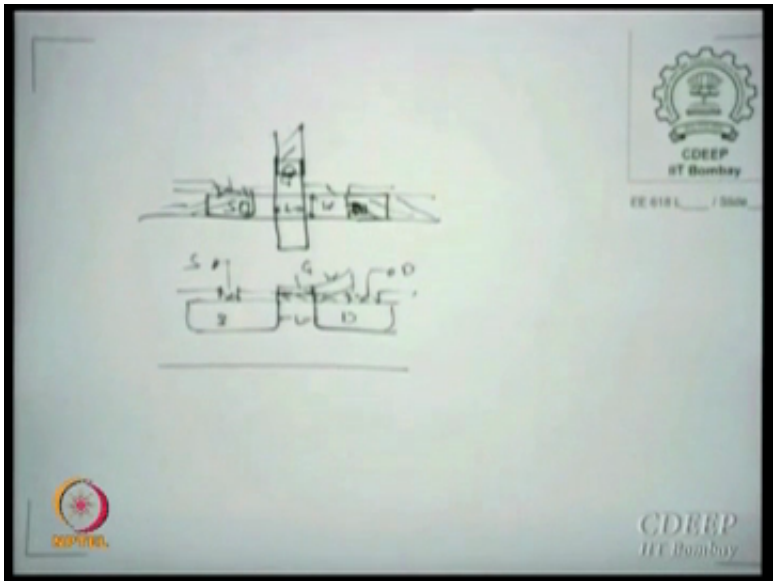

A typical transistor, I have already said this is the black line, which is thing, it is red or pink, it is a gate, this is the green line, which is diffusion. This is third stage gate, this is essentially what you are doing this is the transistor cross section is drain. And if you have window here let us say oxide on the top and contact here. So, I can open a contact here,

these are all oxides contact here, this may be my drain, this may be my gate and this was my suits. So, I can open a window inside this, and make a metal contact on this. I can open a window here and I can put a metal contact here, I can open a window here, cut and I have a contact here. This is called layout.

What is the transistor length and width here from that this is length and this something is width. So, what do you show here which is your length and which is your width; obviously, the poly thickness is your length and poly width on this diffusion width are essentially your width of transistor. So, this is essentially convert this is what I designed from circuit; and once I designed I give you designs they transfer it on the silicon to create this actual structures.

So, my gate at the end for any designer is to create patterns that is what all that we are going to do at the end. So, what there I need lengths and widths. If you give me this I will be able to draw the correct sizes of transistors and in that so I believe that the technology people can translate what I said on silicon. And therefore, the performance should actually be as values of W by L I have chosen. If it does not I will took something and come back once again that is called turnaround.

So, this please remember so as a designer our output is only sizes, some specification electrical solution given; using all that circuit analysis you should arrive at size area and of course, connections because two transistor how will we connect them, how many points will go on a single node. So, this is another connectivity problem which is interconnects. So, all are the design is the W by L for transistors and possible interconnections of thickness and widths because that we will decide R and C for the circuit. So, these are all that we designed as from a designers point of view.

Knowledgeable people pick up this mask and actually print one by one and typical process is around 24 mask for a standard CMOS. If you want extra anything else you thought I should be another this, another mask, it may go as high as 32 mask in some cases; each mask cost hell often means millions and dollars. So, do not just say I could put another window and do something, because that may cost the profit to expenses is ratio which people calculate. (Refer Time: 16:25) may do that extra also because the DRAMS would be sold in millions, same way there may be said do it in microprocessor because they are off shelved any number are sold.

But if you say some specific chip, they will be sold hundreds or a company will live by that much or a thousand two thousand then you cannot put extra money. So, vendor will decide what will do so is that clear? As I designer my job is only to get sizes interconnects I will you I can independently hundred those not very easy that is becoming the worst part right now. But for the sake of analog right now I say I am interested right now only in W by Ls of the all transistor which I see. And if I put their values I can create this if I create this I believe that technology people will be able to translate into a actual silicon chip that is the output from us transfer to actual circuits, is that clear?

So, please remember for us it does not matter any other thing is it not relevant for us. Of course, you may have limitation of bandwidth, you may have limitation of gain power slew rates, V o max, V o min, ICMRS you may put any PSRR, CMRRS you may put any number of constraints or specs for you. But at the end of this what best among them you can get for the design you are asking find W by Ls for all of them. So, I will give you a op amp design later for those who have access to SMDP sites otherwise ask someone who works in VLSI lab there is already an opamp design sitting on my SMDP site under one course which I did from (Refer Time: 18:13) IEP is called. So, there is an opamp design for about I will actually change my specs for your course, so that it is not be identical, but the method will remain same. So, those who wish to see that can even now see that. It is around 10-12 pages or 15 slides or more just to show you how designs go at the end is that point clear?

So, what is our aim is having taken a circuit and given specification this is also our choice, this one, this one any other architecture you will can choose either depends on your thinking. But then they it should meet the given specs for a given technology node as well because you will be specified 0.25 micron process 0.35, 01.8, 0.13 or 90 or 60 whichever technology they say that must conform to that technology node what will change their betas beta dash will change V T s will change, power supply will change. So, many parameters and their variations will change, and therefore, the design will become even tougher as I go down in the node values.

So, designing a 0.35 is the ideal or 5 micron will be the best because everything will work. So, when we design why we choose 5 micron because then we are sure that in case parse you translate I assure you 100 percent it will work, but it someone does it for 45

nanometers me and you will keep guessing may or may not that is the problem with technologies. So, having shown you is two hardware part this one which I am going to use now.

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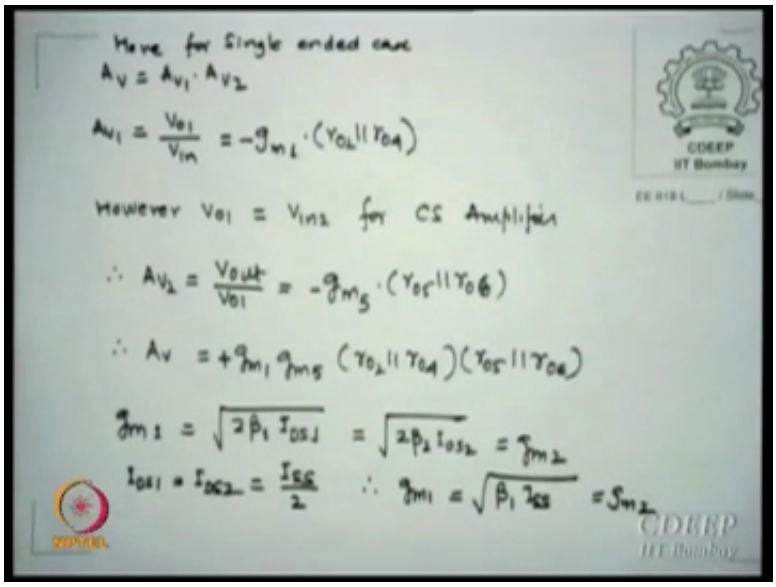

Then there are two stages diff amp stage in a output stage, second gain stage. So, then that gain is A V 1 into a V 2 A V 1 is nothing but the gain of a diff amp, A V 2 is gain of a single ended amplifier. What is this just a minute before you write which is this amplifier is please remember I never said all the input should be only on n channels. This is the p channel device which is taking an input you can see an input is coming there this is the load for it. So, this is a common source amplifier is a p channel driver. So, do not look the other way is that correct input is given to 5 which is a p channel device and to keep it minus V GS this actually the source is given higher voltage. So, that minus values are automatically created is that clear, that is we do in CMOS that is what we did here.

So, please take it this is a standard diff amp followed by a gain stage single common source amplifier whatever it is W by L will give you what are the currents it will keep will give you g ms and ros. And once I know them I can I will be able to evaluate gain of this stage and gain of this stage. So, the example is the A V 1 will be minus g m 1 r o 2 by r o 4 for the diff amp. The A V 2 will be minus g m 5 into r o 5 r o 6. So, the gain finally, two stage gain is g m 1 g m 5 r o 2 r o 5, r o 5 r o 6. Please take it in the first case the output is picked up here is that clear these two transistors have not diode connected.

So, they have r os. So, they may be g m par 1 by g m parallel, but r o will take care of them. Where are then this case one upon g m is its r o actually r o parallel 1 upon g m, but I am not taking output here anyway is that clear?

So, that base terms are missing simply because I am not picking output from that in I am only picking output from here. So, g m times either this g m of this g m because current should be half off m 2 r parallel of these two is the output voltage is that correct? Same way whatever I am receiving here this size ratio r o 6 in parallel r o 5 into g m of r o 5 g m of five is the gain for common source this is that clear. So, it is very simple what we did and therefore, I will not going to again and again solving, we already solved diff amp, we already solve common source, common drain common everything. So, we just substitute whenever is that ok?

So, there is nothing very big this is a diff amp this is a common source amplifier though I have written it, but you can see that I can just multiply the two gains. I also know I can calculate g m 1 and g m 2 by writing two beta one I DS 1 2 beta 2 I DS 2 beta 1 normally a 99.999 will be equal except the variation part. The thresholds will be equal the sizes will be equal. But do not think three and four will as same W i 1 as one and two because they are loads they may be different values compared to this. Why, there other reason also they will be different sizes, the lower transistor of what kind n kind, the upper ones are p kind. So, even for the same current, the ratio will appear. So, for that matter their sizes may be equal between M 3 and M 4, but will not be same as M 1 and M 2 as we did earlier.

So, I can calculate g m 1, g m 2, r o 1, r o 2, r o 3, r o 4 all this knowing the currents and once I know the current. Now, the question is how much current this will draw. An example I will show you this. Please remember this current there it is showing from here I do not know what is the size of M 6, I need. I will see that this current is same as this current we have both p channels, same current flows here to flow the same current here this will not be same current here. Is that clear to you?

Let us say this is I SS this is I SS by 2, this is I S by 2. So, if current which will flow through M 6 is not I SS, but I SS by 2. So, for that W by L will be different, is that point clear, though it is made here, but their size may not be equal is that clear to you? So, these are the issues we should quickly look at it from where current I that is why the first

figures I shown V 2 I, I 2 V, V 2 I. This is V 2 I which is pushing current in the load is that clear? So, the current is coming from M 5 and not from M 6 is that clear to you, yes.

Student: (Refer Time: 25:14).

You can see from it why it should have because if these two values are very different which you can I mean there is no physical problem. The problem with this the current which it will draw and current which it will able to push may not be sufficient then if it is too high from there. At those this current can be pushed here, now if that is increases too much then this will not be able to sustain this maximum current is that correct? Let us say my I SS goes through, so that till I SS it will happen, but beyond that I can always increase 4 times, 80 times, 20 times then the currents cannot be IV actually available to you.

So, device will not remain this device may go out of saturation. So, therefore, the best possible solution is round this current into this which guarantees you both transistor to remain in saturation is that clear. These are the tricks we know to simulation if you do hopefully some we may not you are have you change were yourself and figure out what has happened and that is the trick, yes, it will.

Student: (Refer Time: 26:20).

Please take this is this gate, and this is the source. This value is can always be equal to this if the currents are same. If this current and this current are same these values will be always equal, so that is why I am saying I am sizing that way [FL]. I am exactly telling you this I is equal to beta by 2 W by L V GS minus I am keeping things fixed. So, that I can push the same current is that clear? If V 0 1 is essentially not you know this is divided by these this is the ratio this is an AC current you at you do not confuse between ACs and DCs is that clear? The first part was a DC biasing situation the now I am talking of AC current. Please get these two loads differently working. So, I done the minimum expressions I have figured out, I can just tell you we are just running the jokes what we are done.

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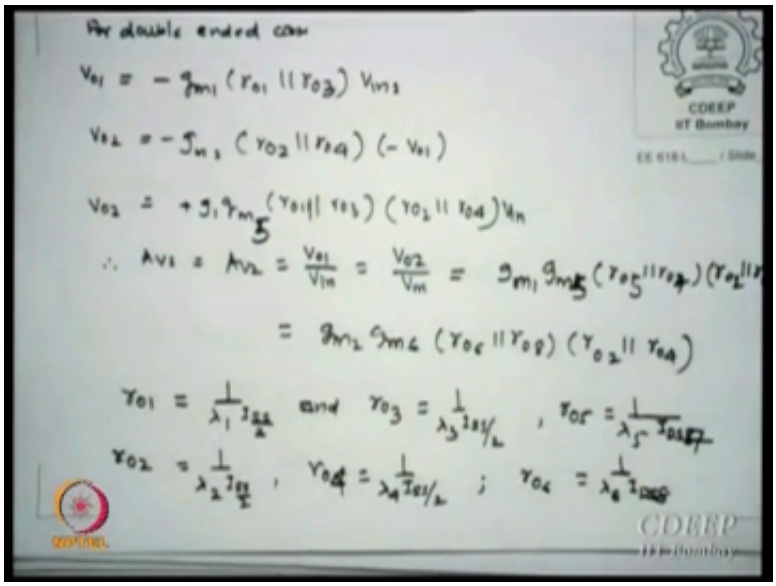

I can found r o 1 by 1 upon lambda 1 r s by 2 r o 2 r o 3. Similar way, I can calculate all r os, and I can calculate all g ms. And if I know one of them, then I can start calculate like all lambdas are equal let us say for p channel; and all lambda were equal for n channels. So, it may two r os will be required to be calculated for those iss is known. So, go back and calculate g m for them and keep doing till you get W bias for all example I am just going to show. This is the formulas only that I will design use for design of a diff amp is that correct diff amp with this. So, I have an example for you, you know this does not look to be very nice expressions is that ok? What are doing I am just trying to say I can evaluate r o, I can evaluate g m in terms of size and currents I SS by 2 and W by Ls will decide my r os and g ms is that clear if alphas lambdas are known.

Typical lambdas for 5 micron process, this 0.06 for width; others may have 0.04, 0.025, but which one is better higher or lower, zero is ideal that is r o is infinite, zero is the ideal, but zero will not get the larger technologies have larger lambdas in general. So, a typical values which my problems taken from (Refer Time: 29:47) book IES 0.06 is typical value they choose, but in real life when I give a problem I may not choose find 06, it may be much different from that then I may use it technology of 0.25. So, the specs given by 0.25, I will use it in your calculation. Right now as I said I am using biased data, and therefore, I am using his values, but otherwise please take it the given data is coming from where technology file on a spice there is a technology file, which will give you all specification for that technology node of a transistors, is that clear; so picked up

actual data from there, which in my case I will give a table or at least give the values. So, is that point clear?

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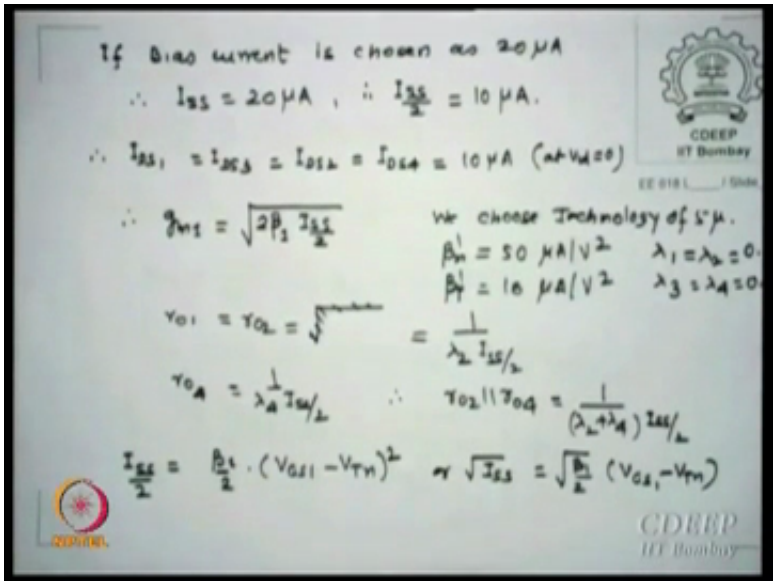

So, let me start solving a problem, which may clarify many of those doubts. Let us say I have total bias current in diff amp is 20 microns I SS r o is 1 upon lambda I D and g m is under root 2 beta I DS [FL]. I agree it is relevant, but that one you can think [FL] single ended all single-ended. You know as I say double ended are specific devices required not that they are not used by the way they are use a differential systems, but as of now ok. Please remember I am using just to give ideas using data from Boyce, Baker, Li's work or Li's book. So, pardon me if that data is copied as it is and problem says may which slightly modified or used there also, but I saw myself I not check with them. If the bias current is chosen as 20 microns then the each arm will get a DC will be off I SS by 2 which is 10 micro amps.

So, I can calculate if given betas lambdas, so I calculate g m 1 which is 2 beta 1 I SS by 2 I know beta n dash I just do not know right now W by l, but that is what I need to know. r o 1 is equal to r o 2 lambdas are given to you which is lambda by 2 I SS by 2, r o 2 parallel is 1 upon lambda 2 plus lambda 4, there may be equal. But if you wish you can write lambda 2 plus lambda 4 into I SS by 2 is that I am not saying lambda are equal then I lambda 2 plus lambda 4 times I SS by 2 is 1 upon r o 2 parallel r o 4. So, this value I will calculate 0.06, it is 0.06 per volt both of them all actually lambdas are chosen same

actually even that is not true p channel lambdas are different from n channel lambdas for that is what I let us say for the simplicity.

So, what is the current in each arm of a diff amp all says by 2 is beta 1 by V GS minus V T 1. So, root I SS root beta 1 by 2 is V GS minus V T 1, and within this for what purpose [FL] expression [FL]. Do I know this? For a five micron process I know V GS 1 how much it will be.

Student: (Refer Time: 32:03).

V ov plus V T for this technology V OV is 0.37 volt as I declared earlier Boyce book, is that ok? What is the purpose of doing this if I know these two values then and if I know this value then I have known beta dash then what can I calculate W by L that is the purpose of all those evaluation is that clear, root I SS is beta 1 by 2.

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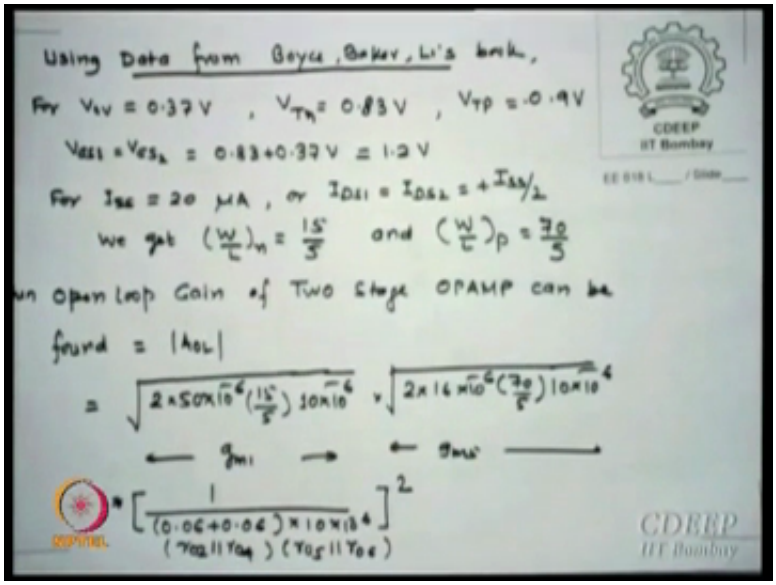

So, if I do this, so if V ov is chosen, 0.37 volt for a V T have 0.83 for n channel and 0.9 minus 0.9 for p channels then V GS 1 is equal to V GS 2 equal to 0.83 plus 0.37, which is for a fivefold supply. V SS is 2.5 minus V DD is 2.5 total supply voltage is a fivefold for which these values are valid. So, always V GS 1 or equal to 1.2. I SS is 20 micro and each is a half current. And if you solve this that becomes W by L and is equal to 15 by 5, and by same argument same current going up I can, I like to calculate V GS 3 and V GS

4 from where instead of 0.83 use 0.9 because I still believe access voltage is same for both n channel and p channels.

So, if I know V GS 1, V GS 2, V GS 3, V GS 4, I will be able to evaluate W by L of 1 2 and for n channel as well as for three and four for the p channels.

Student: (Refer Time: 33:52).

Please I have already said whenever I calculate W by Ls, I neglect all 1 by lambda V DS terms, but when I calculate r o I actually use it because other way r o becomes infinite. So, all calculations have W by Ls and g ms, you may forget about 1 plus lambda V DS term. But whenever you will calculate r o that time do not neglect lambda because that will create higher works for you. So, I know these values. Now, to find an open loop gain, what is the open loop gain the first stage g m 1 r o 2 parallel r o 4 is the first stage, g m 6 r o is 6, 5 and 6 as not forwarding them that name.

Student: 5 and 6.

5 and 6, r o 5 parallel r o 6 is the g m 6 5 times that is the gain for the second stage. So, this is g m 1, g m 5, this is r o 2, r o 5, r o 5, r o 6, substitute the values already I have fixed evaluated it is that correct? So, if the substitute this I did not calculate, but roughly I did some calculations this is called back of envelope mind calculation. So, no envelop, but just by looking at it [FL]. So, around just write down this typical value we should getting around 2500, what should be a unit? Volt per volt is a voltage amplifier specified properly, though it does not matter because say ratio, but even then do specified which amplifier you are using. So, give a unit V by V.

Now, why this will gain was ok, is that point clear? I am able to evaluate and why this L was ol was written though feedbacks are right now used in any part therefore, it is called open loop gains, the next part that we will put closely now that is the next thing we want to do. So, right now itself I started writing open loop, so that later we do not have to say (Refer Time: 36:07) open with. So, I have calculated is that everyone written [FL].

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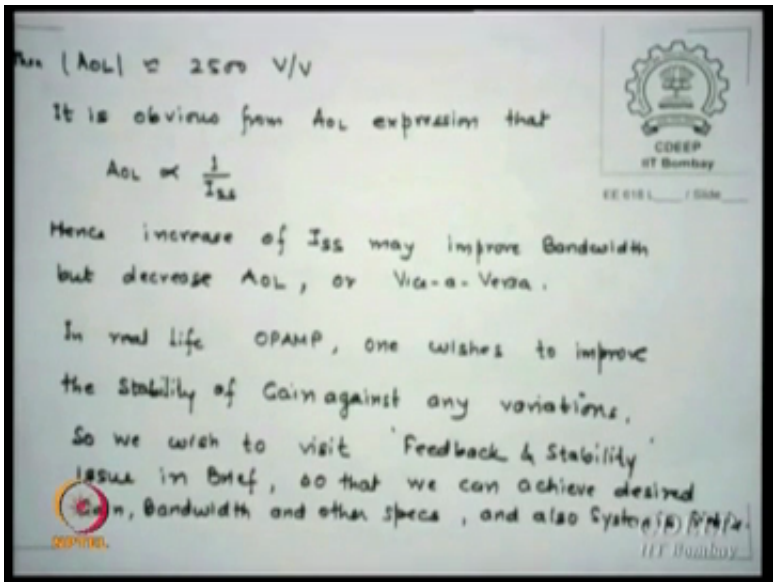

So, A OL is typically I am not exactly, it may be 25, 24, 90 or 26, 50 whatever it is there is [FL] hand calculation [FL] just [FL], but along that. Now, the gain which we want to see very clearly from this expressions of A OL [FL] I SS [FL] I SS a denominator [FL]. So, [FL] lambda times r o sorry g m times r o [FL]. So, proportional to 1 upon I SA [FL] square [FL]. So, we say open loop stage gain for a two stage amplifier opamp is essentially inversely proportional to I SS, is that correct, this is a feature which you should use for your designs, is that clear? What is the feature I got why did all these calculations I figure out if I reduce the current by ten what I will achieve low power fantastic.

Two things I may lose image I may improve bandwidth also I may lose bandwidth also, but I may get gain higher. Another thing I may hurt is that you see the slew rate it will not charge faster. So, then if I want very highs high slew rate, I want higher bandwidths, I will increase g m; that means, I will increase I SS, but I will lose the gain because gain and bandwidth will go opposite, is that clear to you. So, this is what designers do which one you have to cater to and how much closer you can come from either side. So, I wrote again hence the increase of I SS may improve bandwidth, but decrease A OL or vice versa.

Please remember in real life we are not just worried about these values, but we want that these values remain constant for what variations, process variation, temperature

variations and even power supply variations. So, if any variation in power supply appears, currents will change any variation in W by Ls of process parameters will change, currents will change and in any time temperature changes. So, all the current change. So, our worry is we do not want gain to vary any such environmental or design related variations. This word that they should be very low sensitivity for them essentially meaning system should have some mechanism which actually monitors the change and corresponding proportional something it returns to input which corrects it either way. If it is increasing, it should decrease; if it is decreasing, it should increase such a system which we do is called feedback systems, is that clear?

So, why feedback, because these are not constant values; in other assumption right now we assume everything 5 volt remain same W by Ls are same everything is same between M 1, M 2 itself they will not be same. And if there is plus 5 percent, minus 5 percent, you have 10 percent variation which is possible. This may not be possible, this may not be happen on your layouts because that is the screen graphic does very well, but when it goes to silicon and lithographic technique does not allow everything as good.

So, we wish to visit before we are going to the op amp design that since I want the stable gain stable everything I like to quickly look into little bit of feedback which I did in second year many of you might have done it. Many of you still remember better than what I know, many of you never wanted to know so learn now either way. So, let us refresh our self from the feedback because we know feedback and stability that are related. Obviously, this word is true that one kind of feedback may actually spoil the stability, the other may actually stabilize. So, all our tricks is to see that the one which stabilizes always remains. And in some other case that is the joke every designer analog says if I am designing an amplifier, it oscillates; if I am designing a oscillated amplifies.

So, the trick is the amplifier must work as an amplifier and design oscillator must oscillate at a frequency, and the issues are always the opposite. When you design a oscillator, you want something happen and suddenly damping starts. So, what are happened, same way amplifier you think everything should be ok, then it starts giving outputs like this. So, the worries are very important in design, and this should be understood from the basic perspective of feedbacks.

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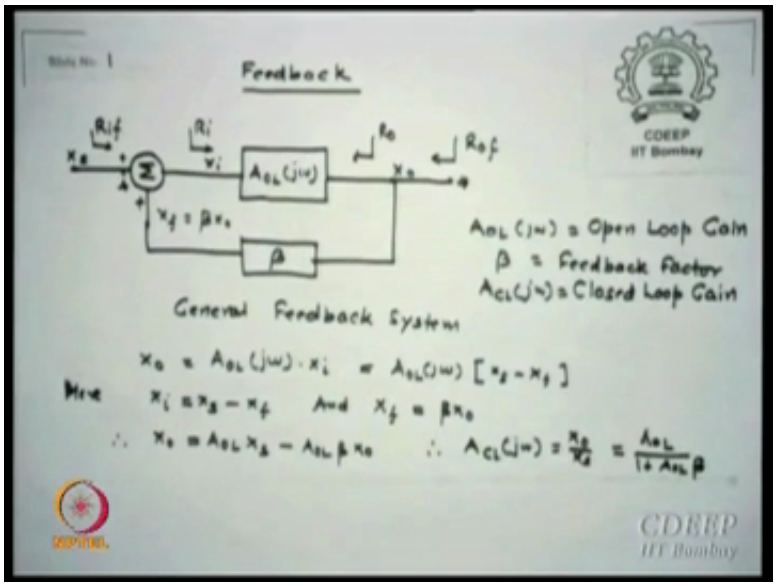

So, let us look at feedback once again. Typical feedback system is shown here. As I said this is only a precursor to what we are actually looking for, but I am just going quickly through the basic feedback k, which will make us understand why we are doing something. So, this is an open loop amplifier; x s is the signal, r i f is the input impedance seen from that, this is some kind of a summer or adder sigma term. The impedance seen by the open loop amplifier is r i, and this is an input x i; output resistance seen inside out to the open loop amplifier j omega output is x 0 and the impedance seen outside x 0 is R o f which decease essentially from network impedance from beta.

The feedback is through a fraction of x 0 is returned please remember beta is always less than 1. So, fraction is returned to the summer and then x s plus x f will happen depending on the sign either x s minus x f occurs or x s plus x f occurs depending on the sign of to which you receive. So, A OL is called open loop gain, beta is called feedback factor normally beta is passive element normally, but need not be. And if it is need not, if it is the other way then the analysis becomes very, very complicated, but right now we will say assume constant.

So, we say x 0 is the gain times x i; xi is the input to open loop gain and amplifier x 0 is the output. So, x 0 is A OL j omega x i A OL j omega x i is nothing but x s minus x f the way right now signs are shown; x i is therefore, x s minus x f, because of this I wrote this

and x f is nothing but beta times x 0. So, x 0 is A OL x s minus A OL beta x 0. So, if I now define the closed loop gain which is x 0 by x s, then it is A OL upon 1 plus A OL beta, the sign of this can become minus depending on the A OL is what sign, is that clear? A OL is negative it will become 1 minus a beta if it is two stage it may become one plus a beta. So, right now I did not want to put a sign in real life, I will put a minus or plus as it appears. Now, this fact that closed loop gain related to open loop gain through A OL upon 1 plus A OL beta; and in the control system theory or in feedback theory, we give some names for this.

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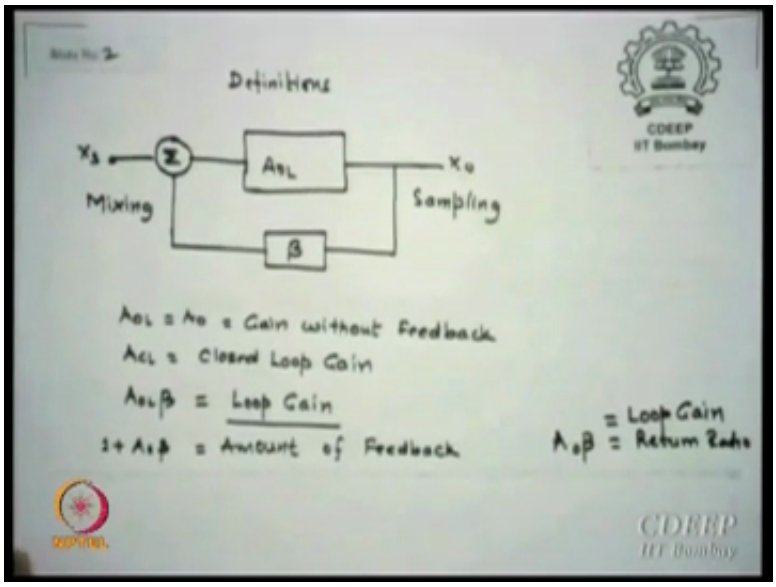

If you have any book, these are standard definitions in any book including the book yesterday I said about (Refer Time: 44:25) and me; so [FL]. A OL is the open loop gain this is called mixing area this is called sampling area. So, you sample the output return to input to a mixing. So, A OL is gained without feedback A CL is the closed loop gain with feedback. And we define a term A OL beta as the loop gain, as the loop gain; also it is called return ratio some books like Grace they are large book use it return ratio. So, if you are (Refer Time: 45:01) raj happens to see the (Refer Time: 45:03) book [FL] return ratio, I will to use the word return ratio not the loop gain.

So, essentially the 1 plus A beta actually decides the feedback available to you because A OL is the open loop gain, and this is additional term which is coming who is deciding the part coming from feedback. These are definitions. If you see the iterations everyone has

is the standard and as I say at least the fourth year students were taken my course second year, this slide I actually copied from that, you can see this number appearing here is that?

Student: What is amount of feedback?

1 upon a beta decide how much you are away from you if open loop is A OL that is the point which is changing the gain by putting 1 plus A beta. So, if that is larger A OL will be is net gain is smaller if it is smaller that is higher, but you will never reach A OL anyway unless beta is removed.

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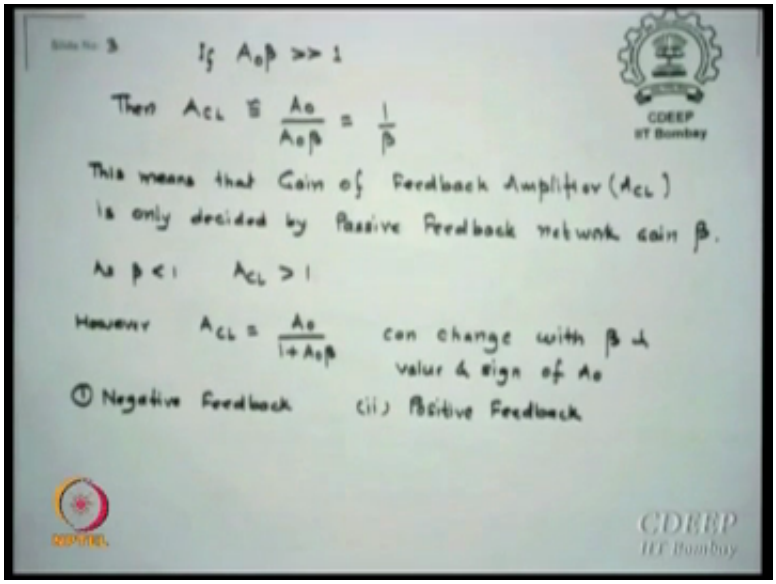

If let us say the loop gain a beta is greater than a and A OL A OL cancels or A O A O cancels and we see closed loop gain is one upon beta is this good or bad? It is very good because beta is a passive network, which is relatively can be kept constant. So, if you have a feedback and you are gain loop turn loop gains are higher then you are safer because your feedback is very much stable. So, what worrying all this calculation is we always assume beta gain is once you do this, it is constant no actually beta itself may vary. Beta resistor [FL] temperature coefficient [FL], but that is why we say r 1 upon r 1 plus r 2 [FL]. However, beta is less than one then A CL can be greater than one and; however, A CL is A 0 1 plus A beta can change with beta and value and sign of A 0.

So, there are two possible ways the feedback can affect us if you see our figure if the x and x f are in the same sense, then the add and their opposites are sorry their opposites and they add, if they are in some sense they actually subtract. Battery [FL] plus minus plus minus add [FL] plus minus minus plus subtracted [FL]. So, essentially one which reduces the x i value from its x s value we say it is negative feedback, but it does not mean always reduces it also can correspondingly change output will return less feedback and try to adjust, where do we think positive feedbacks are used.

Student: Oscillators.

Oscillators: for all amplifier will preferred negative feedback and that is what my issue was that when I design an amplifier, I land up in this and our design an oscillator and I land up here, because both are functions have some parameters, one may dominate over other and you forgot to trained them well. So, it is ok, so basic idea is to design a negative feedback circuit. Just for the sake of completeness if you have a negative gain feedback what essentially we gain in an amplifier is that everyone this is standard.

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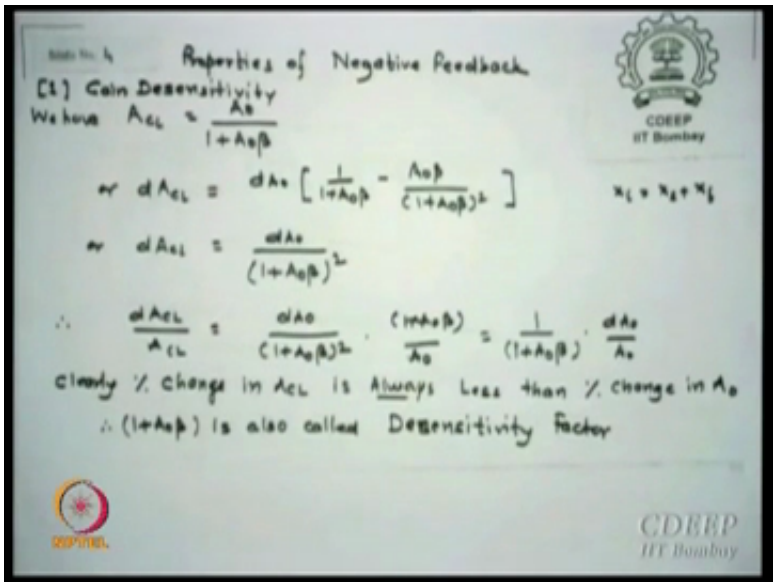

The first thing it actually does is desensitivity of the gain. What does desensitivity means it reduces the sensitive. If you see a closed loop gain which is A 0 upon 1 plus A 0 L you can write I have sometimes I wrote A 0 sometime A OL. So, it is A 0 up on 1 plus A 0 beta d A CL is d A0 upon differentiate [FL] then we say d A CL is d A 0 upon 1 plus A beta this still connecting this d A0 is into 1 plus A 0 [FL] multiply [FL].

So, this essentially give me d A 0 by A 0 is equal to 1 upon A 0 beta d A CL by A CL. So, you can see any change in A 0 will be reduced by 1 plus A beta for the closed loop system. So, you are desensitized. Change in A 0 is now reduced in the A CL system by as much as 1 upon 1 plus A beta. So, this is called desensitivity parameter or factor. So, any percentage change in A 0, please remember this is the standard technique of showing sensitivities d A 0 by is dy by y equal to dx by x [FL] relation [FL] percentage in this percentage change in how much. So, essentially they say the change percentage here will be reduced and this because by this factor. So, this is say desensitivity. The second advantage which feedback gives for an amplifier specific is let us look at the.

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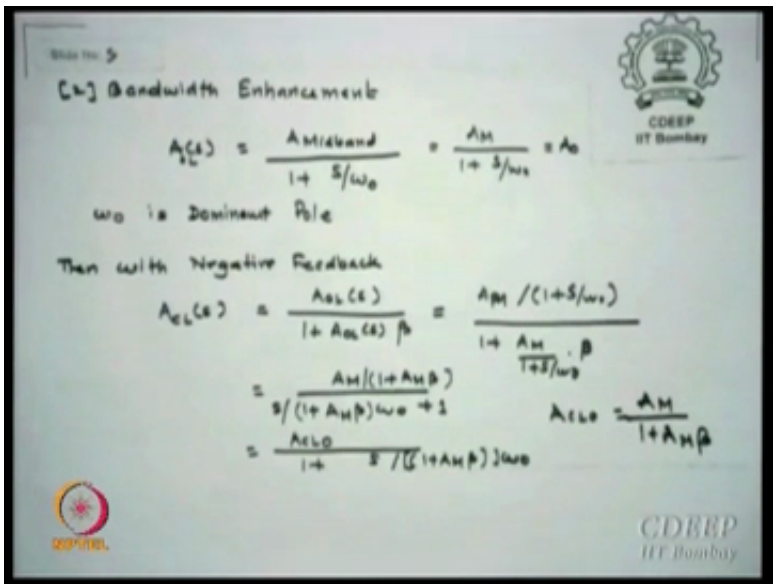

So, the second feature of negative feedback is it improves the bandwidth let us say your open loop gain is a midband upon 1 plus s omega 0 where omega 0 is the first pole dominant pole we call it than am upon one plus s omega 0 is A 0, A OL is A 0 right now. Then with the negative feedback A CLs is A OLs upon 1 plus A OLs beta substitute this quantity here and here. So, you get A m upon 1 is midband gain A m upon 1 plus s by omega 0 upon 1 plus A m upon s plus omega into beta collect the terms and define A CL 0 as A m upon 1 plus A m beta which is independent of frequency. So, dc closed loop gain dc closed loop gain am is the dc midband gain for open loop system

So, I get A CLs is A CLO upon 1 plus s times s by 1 plus A m beta times omega 0. So, now, the pole has been shifted from omega 0 to 1 plus a beta times omega 0. So, you are

improved your bandwidth by this much amount by just putting a feedback is that clear. So, why is that clear, but if you see CLO closed loop gain what it has done it has reduced by that much amount. So, bandwidth has increased by that much amount.

Please take it the these are my notations names, you may have if reading from any other book and they have follow, but follow universally what you follow once, like spice you just k as the beta. But some spice new versions use k by 2 or rather beta by 2 as k. The think of it this can worry you because you are losing 50 percent on that like spice level threes level 49 versions use the beta dash by 3 has k dash whereas, the 3.3 the old versions and the spice there only use beta dash as k dash.

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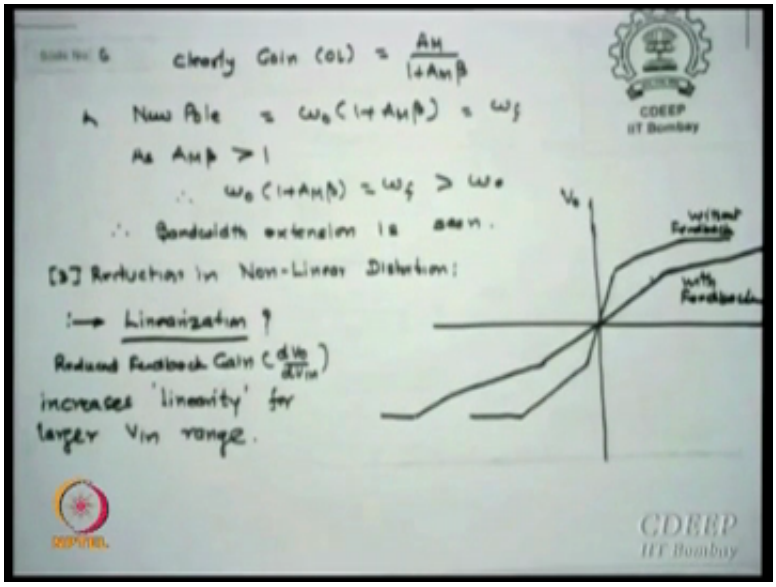

The next of course, this I made a statement obviously, the bandwidth improves gain false. Third most important reason why one works with the feedback negative feedback says it actually reduces what we called non-linear distortions in amplifiers. What does non-linear distortions means, if you have a characteristics V 0 versus V in for a given V in value if the linearity is not held then the since the curve is not linear it is a non-linear term.

So, when you actually find V 0 in terms of V in V r square cube polynomial terms will appear. So, much of their power or energy will be lost in other frequencies second harmonic, third harmonic and higher harmonics. Whereas, you want all the energy should go to fundamental so that means, larger the slope change more and more energy is

being lost that is V 0 is not getting at that frequent fundamental frequency exactly transferring from V in that is called harmonic distortion. The third harmonic distortion is the worst among all, so that phases in exactly with the first ones. So, it gives huge in difference. So, in R f design or any other designs the worry is DHD what that we will see later.

So, let us say this is the kind of characteristics without feedback and in this range p zero v in is linear beyond this of course it change of the slope it may actually for further. So, these are non-linear terms. So, any input here or here with this slope will give you second and third or fourth harmonics. However if you add a feedback you are just now seen k means something like release now particularly, but this, but now you can see the this frequency term up to which

Student: Sir, above 1 is without (Refer Time: 54:44).

Sorry, that is what I am seeing how it is opposite.

Student: (Refer Time: 54:49).

No.

Student: Yeah.

That is fine. So, what essentially is trying to say is as I change dV 0 by dV in changes; that means, the linearity is correspondingly changing. So, the idea behind putting a feedback is increase linearities. So, [FL] linear what is the purpose than you may be increase linearity, but your gains will be correspondingly different from your requirements, so is the bandwidths will be different, but at least for large signal operations probably you will be able to operate better.

So, this is the three things by everyone goes for negative feedbacks. So, from where them now in our OPAMPs or anywhere from where or any amplifier where the feedback is coming in a transistor normal transistor if common source for example, is there which is the feedback which is coming from T gd, C gd, d is the output node g is the input node. So, the capacitance between gate and drain essentially is always available to you as a feedback factor.

So, irrespective whether you put any c external c is there, C gd is always going to put you in negative feedback system. And if that happened that is why systems had lower bandwidth we are calculated vcgds, but it is relatively will be stable operations one more stability that c will built actually increased, but doing that what else we will use we will see that that is our designs.

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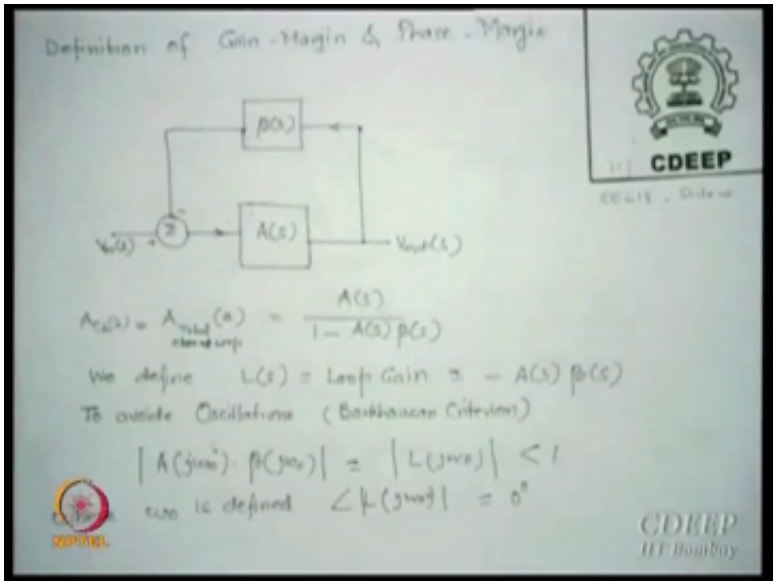

So, we want to using this before we quit for the day, there is something which you should know there are the two terms you used in feedbacks or any (Refer Time: 56:52) system of free frequency response recalled those terms as gain margin and phase margins. These are most important parameters in design. We will be specified phase margin for an amplifier or if not specified as a designer you will have to choose it how much I should have. Should I have 45 degree phase margin, 50 degree phase margin, 55 degree phase margin or 65 or 80 or 90? You may choose either at the phase margins how will they influence the performance is what we are going to see.

So, what is the phase margin we will like to see. This is our closed loop system. The closed loop gain is as upon 1 minus as beta s and as I said we define the loop local loop gain as A s beta s here they as is taken minus. So, sign is going accordingly there is a standard criteria which is called Barkhausen criteria for oscillations some non instability it says A j omega 0 into beta j omega 0 which is L j omega 0 should be less than the magnitude y should be less than 1 first stability. Where omega 0 is the frequency at

which the loop gain phase is 0. I repeat omega 0 is the frequency at which the loop gain is sorry the angle or phase of that is zero angle means phase, phase is 0 at that frequency at that frequency A times beta must be less than 1 then the system will remain stable. In case of oscillator, what will do it we will actually both these to make it oscillate because gain is minus though this is taken at like this, but this sign is taken as written with a minus signs because the gain is less than db the way we calculate. So, you will just check it we will come back to it again.

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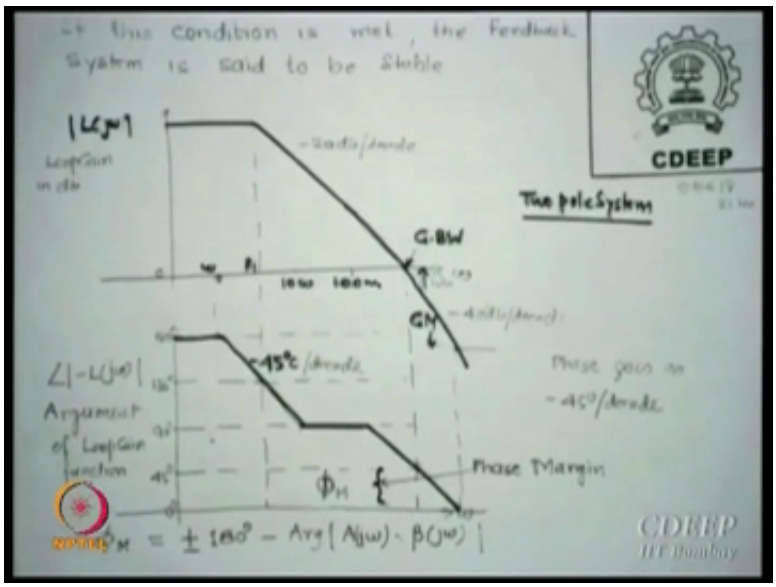

Now, here is the important graph which is given in every book; if not you can note down from here. This is the representative graph nothing very this is Bodega plot. I am plotting a loop gain versus frequency. Let us say I have a pole p 1 where the loop gain starts falling from this frequency p 1. And let us also say if I design the second pole is at the gain bandwidth point which I can design GBW is this where the gain becomes one the pole actually occurs there, is that point clear? The p 2 pole occurs right here is it just to explain nothing it may occur later or it may occur earlier, but just to make the case important study case, is that kind of the first pole is here. Second pole is actually starting here at this point.

You know from the Bodega plot that once the poles this 3 dB point goes the loop gain will start falling by minus 20 dB per decade. And it reaches if there is no pole till then it will go to the 0 dB point or it crosses the omega x s at this point which is your gain

bandwidth point. And let us say if the second pole occurs here that will also give you another 20 dB per decade fall. So, this 20 plus the second pole 20, so the next fall will start going by 40 dB. If there another pole somewhere here when your 60 dB, it will start falling down afterwards let us say the third poles occur here at this point 60 dB will start falling. But once the gain falls below minus 90 dB or even 0 dB, it is not a gain anyway is that correct? Gain means lower something which is positive only if it is positive dBs; otherwise it is a fraction you know if it is a fraction you may still call it a gain, but it is not really a gain. So, gain is only up to this as long as s plus dBs.

Now, if you have done where complex in general well and I last day I did tell this tan inverse or the angle for this is tan inverse imaginary by real essentially gives me what they call argument or tan inverse points and for these you studied if not some other day. At first pole it just at least have 45 degree down from the midband point. Midband points start 180 degree because that is where the loop gain starts. So, from 180 at the pole it should have gone to 45 degree down because this slope is 45 degree per decade why 45 tan inverse 1 is 45, so that is a 45 degree. So, from 180 goes to 135 at the pole position 45 degree down per decade assuming per at the pole

And it continuous to fall by 45 degree per decade as the frequency increases, but since there is no pole ahead then delay this after this total of j 1 j is over 90 degree the phase will become constant. And it continuous to remain constant, but it wants that at the second pole it should go 45 degree further down. So, from this ninety degree it should go to 45 degree. So, this 45 degree per decade must cross at 45 degree point at the second pole is that clear?

So, this therefore, slope becomes something like this. And this is the point please remember these are the points of interest to me at the pole p 2 or at this gain bandwidth point the phase of loop loop gain phases how much 45 degree, is that clear? If you increase further this gain 60 db or 40 db down then finally, phase will become zero, phase will become zero. If you further go down, it will actually increase further minus of that value as if you say when the oscillation starts when the output and input becomes in phase if they are out of phase, they will remain in negative feedback stable situation.

What we are trying to see now is if when the gain is 0, you are still in the negative feedback phase 45 degree you are away from it, is that correct. Let us say at this point

would have occurred here, I do not have figured here somewhere then what would have happen, the gain would have been positive A 0. And a phase now is zero or other side which means the signal is now returning phase with the input is that correct which is the condition of growth that is instability.

So, to keep it stable what is the criteria when the gain is loop gain is positive the phase should not cross zero. So, the margin up to which this is available to you is called phase margin. So, how much is phase margin with me here 45 degrees. So, 45 degree is the phase margin available till that time the gain, you can see from here beyond this the gain has already crossed zero and my phase has not gone to zero is that correct? Beyond if this could have gone somewhere here are the gain would have remain positive and phase would have across zero then I would have in phase component in the feedback in which case the growth would have started. So, this is essentially called phase margin.

Then a zero degree phase if the gain is negative then you are safer, this is called gain margin. A zero degree phase how much you are away from GBW point is it called gain margin right now this is negative, but let us say if you are in opposite side gain margin will be positive, and phase margin will become negative which means you will have a unstable situations is that correct? So, in normal case gain margins are not specified because they essentially represent I am in away. So, we only say as long as phase margin is 45 degree, why 45 degree is important for me, why not 30 even as long as it is anything between 45, I am still safe. What is the worry we do not want to go below 45 anything, any additional capacitor parasitic appears, how much phase it can give you 90 degree that may push it down earlier than what we thought.

So, the minimum because 50 percent point I have to get it. So, I say at least 45 I should have so that the worst stage gain margin is zero at phase margin is 0. So, we are exactly cutting each one is that clear. So, the minimum phase margin for stability is 45. Now, we will see tomorrow some more details of this. And we will prove that the phase margins are essentially adjusted because what will phase margin will do they are deciding poles is that correct? We know poles reside the bandwidths.

So, by changing the phase margin we are also designing the bandwidth for the amplifier. So, how much otherwise you will have got to 90 also you safe very safe very safe may have lower bandwidth because then only this can occur, that very safe may create your

bandwidth very, very small. So, you need higher bandwidths and you will also need safe margin. So, somewhere between 45 is very lowers so never tried 55 degree to 65, 70 degree is the range in which and this number has something to do with transient response also, which will see next time zeta functions.

We are right now only looking which frequency response frequency response; if I see a time response I will suddenly see something else is happening at the phase changes and that time I will say how much margin I have really to work with.

See you next time.