CMOS Analog VLSI Design
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Lecture – 13
Current Sources

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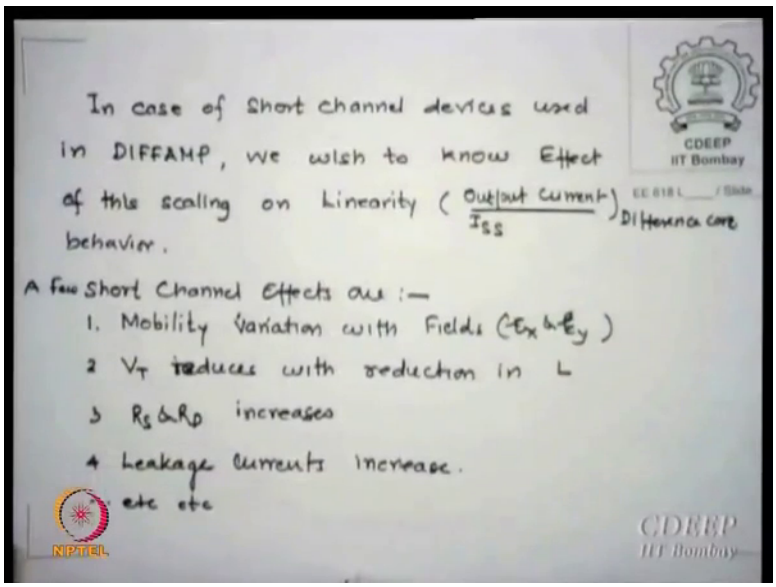

So, we start with what we were talking last time; continuing with some little more about DIFFAMP. Though actually DIFFAMP needs much more explanations. I will start working on DIFFAMPs frequency response later after these two days, after the exam and that time I will show you more problems of DIFFAMP designs. So, let us start with the present a problem which is not really present in last 15 years, 10 years I can say we have been working with short channel devices. And I repeat for those who have forgotten a short channel if device is defined as if the channel length of the device is comparable to the source drain junction depth or almost of equal to the depletion layer width in the gate region, is that clear if they are comparables, then we say device is in short channel.

Essentially the way scaling goes that we scale the dimensions of the device let us say from the depletion layer width below the channel and the junction depth of source and drain. Either of them are comparable to channel length then we say device is in short channel. The problem with short channel as I say when you scale length and width the problem is it creates lot of problems on linearity which is essentially the output currents.

And we like to see then what happens, but please remember scaling is more relevant because the voltage we normally do what we call voltage scaling.

If we do field scaling that means, all voltage length everything scales then there is no problem everything is scalable, but there is not possible because the power supply values are not decided by scaling people, it is decided the system people. So, we started with 5 volt, 3.3 volt, 2.1 volt, 1.5 volt, 1.2 volt, 1 volt, 0.8 volt. So, this is not something which I can decide this is someone else is going to decide. If I scale them then the voltage to length ratio or fields will be larger because voltage will not scale as much as the lengths will scale. And there is the issue where it creates problem for performance.

Typically, of course, there are many short channel effects you must have done in many other courses; I just list for something which you heard me in this course. One other problem I see is the mobility variation due to the fields because both E x, E y in increase there is also a problem of V T reduction as the channel lengths goes down go. There is another issue some other device person will know that we have come very close to 90 nanometers around, there is a increase of V T this is call bounds. So, there are issues there also if you are in that region you will have to take care of your V T much more.

Then there is an increase of source drain resistances, the reason is as I just now said scaling things the junction depth goes down and the dimensions also x and y goes down for source drain, so resistance actually increases. The leakage currents also increases because of variety of leakage mechanisms including diode leakage, gate induced leakage or what is called griddle that gate tunneling effects, band to band tunneling and n number of time high field injection problems. So, there are huge problems in leakage currents. So, they the normally enhance and the huge scale. However, as I said these are not the only effects, which we are worried about in digital course someone must tell you or in devices course someone tell you much more and that, but you always reduces with channel lengths think of it.

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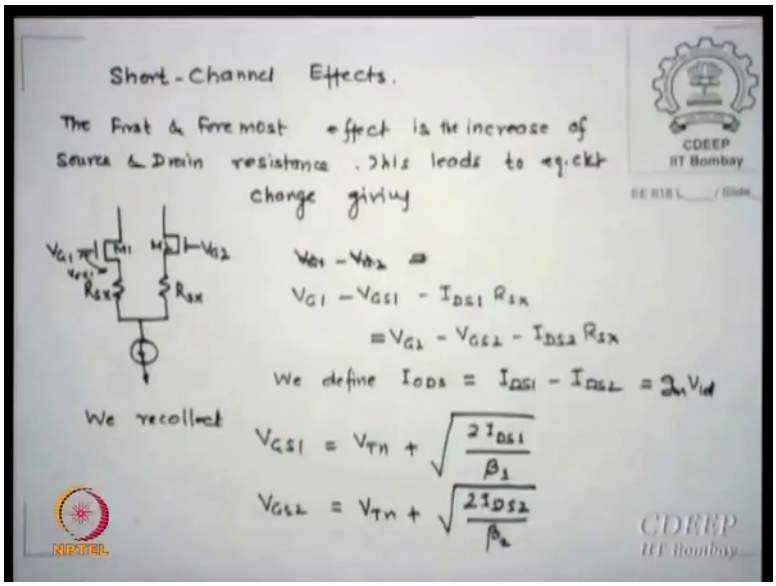

So, [FL] device [FL], the first and the foremost effect a absolute terms, leakage current absolutely increases enormously (Refer Time: 04:15), some of the leakage currents are exponential and that is of our worries. A leakage of course, as I said this is not a digital course, but just to give an idea what we are saying. For all high performance circuits, we are interested in what we call on to off ratio, on currents hardly increase and the off currents which is the leak part of which is 90 percent leakage increases enormously. So, our worry starts that once I said you also that why which we allow student to continue listen because off power is larger than on power. So, therefore, it is better if you use rather than keep it in standby, this is of course, a fun part in that do not go.

So, let us for us which is immediate of interest is this. As I said there is a increase of source and drain resistance, drain resistance of course, can be taken care through the load value. So, you can say even if 10 ohms increase there, the loads are 40 kilo ohms or 10 kilo ohms and above, so that series resistance that does not matter as much. Whereas, in the source side if you see a resistance what it strikes immediately, if there is a source resistance in a amplifier what does it do, it reduces the gain drastically, is that correct it is called source degeneration.

So, the first problem comes and the short channel device is used, there is a source resistance now and it enhances as channel link goes down further. And because of that there is a source degeneration effect, which reduces the gain of a DIFFAMP, this is an

issue which otherwise in a long channel we may not worry about. I will not derive the expression, which follow soon.

We define a term current difference between this and this I ODS defined as I DS1 minus I DS 2 which is essentially gm v id where V GS 1 V GS 2 can be explained in this expressions. And we can now seek for this node V G 1 minus V GS one minus I DS R x is equal to V G 2 minus I DS R x minus V G 2 is essentially equal because this point does not move. So, this is an equations which now you may have to use in your evaluations is that clear. And the major effect as I say is instead of doing all of it again is source resistance in an amplifier is 1 plus g m R ss times again may go down that is the feedback effect in fact, you will see. Is that ok. So, this is a typical expression you can look into books.

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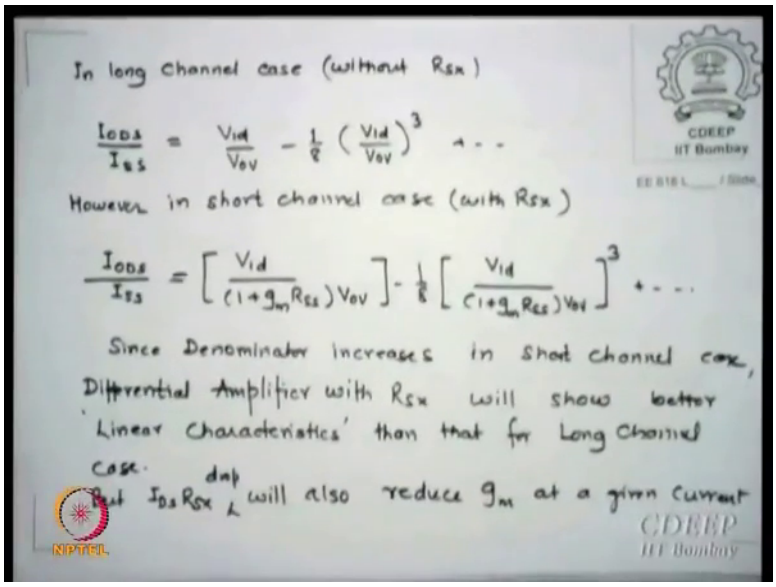

Of course does not have some other books, I do not recollect. The ratio of the difference current of the (Refer Time: 07:11) divided by I SS and net current which is current source supplies can be expressed in a Taylor series which is V id by VOV minus 1 by 8 V id cube by VOV plus other higher terms. Since V id by VOV is smaller since denominator increases in short channel case differential apply with R sx will show better linear characteristics that is fantastic because then it will actually if we see the terms this term will be even smaller because now so you will actually come closer to linearity. So, one of the advantages of having source degeneration at the cost of gain is your linearity

improves. So, it is something everything is not going wrong as we think so. But if I DRS drops will also reduce gm because the available current available voltage to you is smaller, so essentially gm at a given current will also actually reduce. However, please remember, what is our design parameter all through as I say though I have written expression in terms of V ov, but what should be our design spec on g m by I DS.

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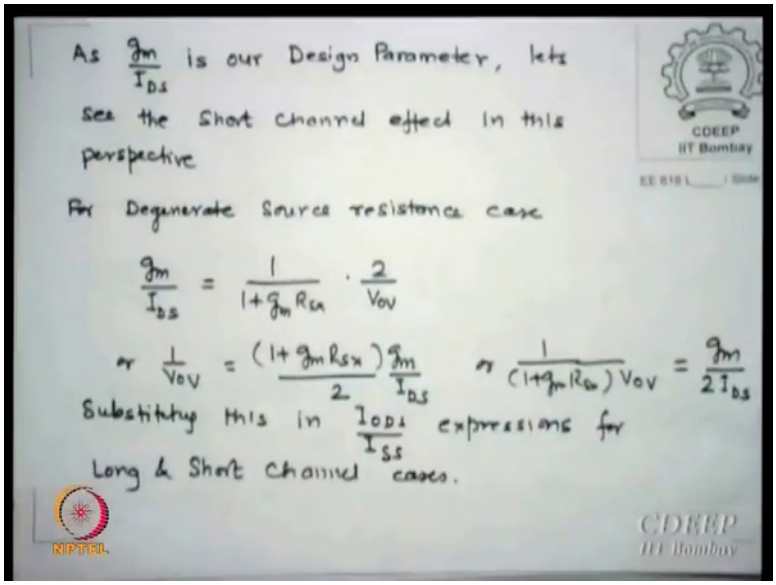

So, if you look at this gm by I DS term, so we said last time and as I say g m by I DS is now 1 upon 1 plus g m r x 2 by V vo. We are not just 2 by VOV as we thought or if we calculate VOV, this can be in this term. So, substituting this in I OD ISS expression for long and short channels I already divided one upon VOV is this expression or this expression is g m by 2 I DS. So, if gm by I DS is our design parameter which we are going to have why did I say that VOV is not a good parameter of design, because V GS minus V T the excess voltage which can be chosen by any number or can vary any time. So, instead of that we prefer to have something which is more rigid which is g m by I DS ratio. So, we say all that I am trying to get the expression for 1 plus gm R sx VOV is equal to g m by 2 I DS. And if I substitute this expression in the I OD expression both for long channel and short channel.

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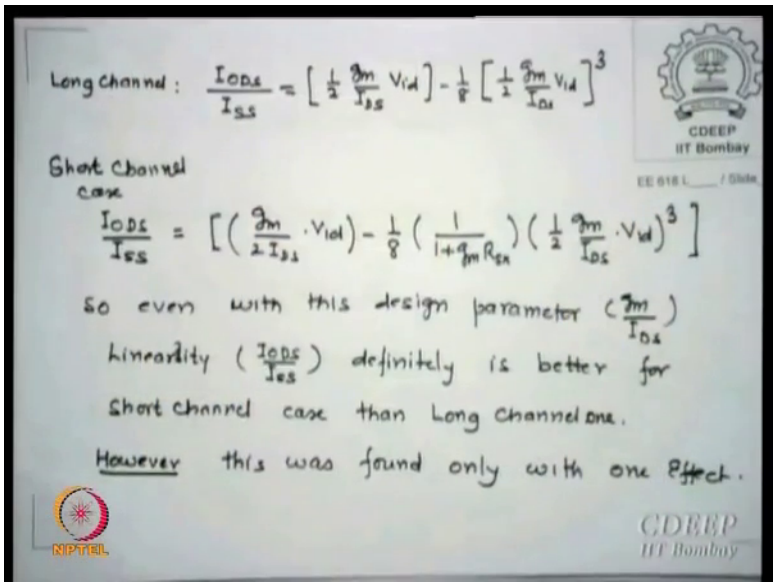

So, if I substitute for both this 1 upon g m R s x into this into this expression for long channel and the short channel for a long channel it becomes half g m by I DS V id minus 1 by 8 half gm by I DS divided to the power cube. And in a short channel case I ODS I ss will now become gm by 2 I ss V ID minus 1 upon 8 1 plus g m R sx V ID cube. We now see since the second term has large 1 plus g m R sx divider there this term will be further smaller why it is called cubed term is not interesting to us call it is introducing a non-linearity in the IV characteristics essentially. So, to make a linearity this term should be smaller. So, by sources resistance available, the second term goes down there are first remains same, and therefore we can say that in a short channel device even with g m by I DS design parameter, linearity will improve with short channel device.

So, do not feel you know everyone always try to curse short channel devices, of course, digital people do not care so much because the first thing they look into or even we should not look so that way bad way. Because the first thing they says the electron or whole transit time from source to drain will be smaller if the channel length is smaller, smaller the propagation time higher is the speeds. So, for any high speed circuit the first criteria for me is channel length be as small as possible preferably 0, then everything. What is these devices are called when it is equivalent channel lengths are 0, I thought maybe you have done some seminar these dates arrives. There are devices called tunnel devices or tenets which do this or called also ballistic devices, where typically they have no restriction of movements, some other day some other time.

So, the point I was trying to say that short channel device is better as far as linearity is concerned, the only problem which it may create is and net gain may actually, but gain can be pushed through other by increasing I DS. But if I increase I DS, power will go, so there is an issue there. Or if I increase size the capacitance is inclusive the bandwidth may go down. So, they are not that it is so trivial, but at the same time at least swings are larger. So, if you are looking for is larger swings, yeah this is the better device. Normally, what did I say channel length should be as high as possible for what purpose I say the R out essentially is given by lambda dash by L? So, smaller the channel length the output resistance is higher good for gain g m R o. So, longer length devices always are preferred for high gains.

So, you think of it now conditions where do are you working at, what are you looking at and therefore, correspondingly sizes may be chosen by, is that design clear to you, this is what designers do. I want this, so what should I do is that ok all of you? So, now, we this is something, which I last time should have done a finish, I thought I have finished once a while I thought or maybe I did not, I do not know. As I say I am going to talk about the DIFFAMP once again little later with the bandwidth and some other issues which DIFFAMP is creating. Why I am now worried about DIFFAMP problems, because DIFFAMP as I keep saying is the main gain stage of an operational amplifier which is our workhorse. So, anything I want good from a opamp I must get first from DIFFAMP itself. And any problem which DIFFAMP is showing will automatically a problem for opamp is well.

So, at the end I am interested in an opamp designed not really specifically only DIFFAMPs, but I know if I design this properly I understand what to design and I also can design opamp as good probably. We will see there are other issues may come with opamps, but they are different. Before I first I thought I should finish that and I also thought I should do a frequency response, but I thought that frequency response can wait because we will look into that more specifically from the stability criteria. So, we will club everything there. Right now you assume the bandwidth is essentially given by one upon 2 pi R out into C l or C GS or C n whichever is the value given to you the other r by C R c constant must be not comparable here and therefore, neglect. So, mostly I am talking of a dominant pole which will be given by one value of the capacitance given,

this much you are anyway done in your second year or third year courses, so that that much knowledge right now may be sufficient.

Please take it, it will have impact in our designs last time I showed you values bandwidth gives you R out by C l values C l given to you it evaluates your r out r out gives you lengths and I DS and therefore, this I DS has the another limit coming from given bandwidths is that clear? So, do not ask me that you I have not taught that I have taught in indirect way. So, here is the new chapter I wish new area we want to start because these are required in normal opamp or DIFFAMP designs, so that I will first do that. Few things which are of basic blocks in any analog circuit or analogue IC is how to bias. And one of the strongest way of biasing those circuit we suggested is through a current sources. So, we like to see which are these current sources and our current sinks.

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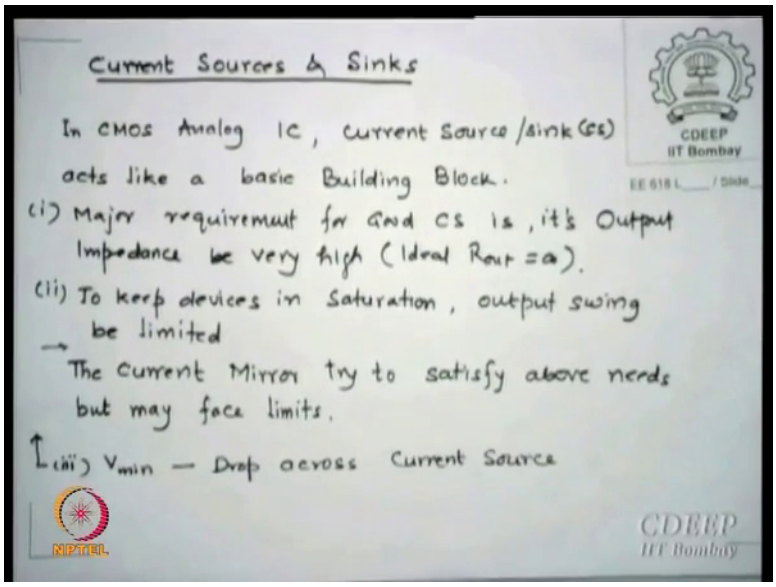

But how do you differentiate between a source and a sink? If it starts from power supply then we say it is sourced; if it goes to the ground it is called sink. Basically they are not very different, but just for the sake of clarity anything which current enters the ground then it is the sink if current emulates from the power supply then it is called source. They are identical in values many times the same current may go down, but just to get where do I put that source current source as such may we call source or sink theoretically it does not matter, but principally one should know where is the placement going on.

So, as I said in most analog ICs unique current sources the major requirement for a good current source it is its output impedance. I will enter here. The first is you need R out as large as possible preferably infinite if it is ideal source; otherwise, as high as possible. We also should see that to keep devices in saturation the output swings are limited, if you are too much output swing you may go out of saturation regions. So, a current source when you design, you must see that you are always in device should remain in saturation. Why do I say current source is the device saturated device, because saturated current of a transistor is beta by 2 W or beta by 2 into V GS minus V T or VOV square into 1 plus lambda V DS.

So, VOV square; square means it is a square law term and therefore, we say and if we do lambda is very very small a current is constant, current is constant, therefore, it is call current source or sink. So, device must remain in saturation if you want a current source. So, many a time this swing which you are actually expecting in your DIFFAMPs or many other places is limited because this current source may not remain current source there. And therefore, this has to be very limited of course too far away normal ranges, but you must keep in mind.

And third and the foremost is V minimum what is this why I am worried about V min what does that mean? Normally, we say that the diode for example, has a cut in voltage of 0.6. So, what does that mean that till that voltage is reached in for bias no current flows is that. So, if V min is the drop across the current source. Firstly, it will take V DD minus this much available to you downwards is that clear; that means, it is also now consuming power because there is a v drop there it is consuming power. So, to minimize power and you want to have a ideal current source is what?

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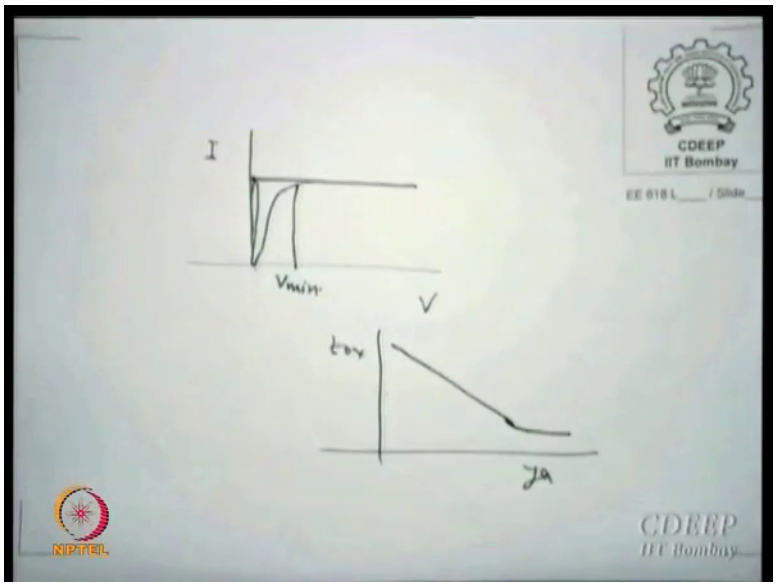

See if I plot I DS versus V DS I would expect I DS versus V whatever I find draw if I good current source I will like something like this, but in real life something like this happen and this value is V min is that ideally what do I want like this constant current source. So, I must minimize V minimum as much as possible; in reality 0 it cannot be made because device will have some drops, but how much minimum we can go is the goodness of current source. So, how many three parameters to worry about, one is the output resistance, two swings available to you which makes device remain in saturation, and three the smaller the v min better as the current source is that correct? So, these issues are clear to you? So, these based on this and I said you already apart from every other thing a typical current mirror satisfy many of these requirements directly, sometimes indirectly.

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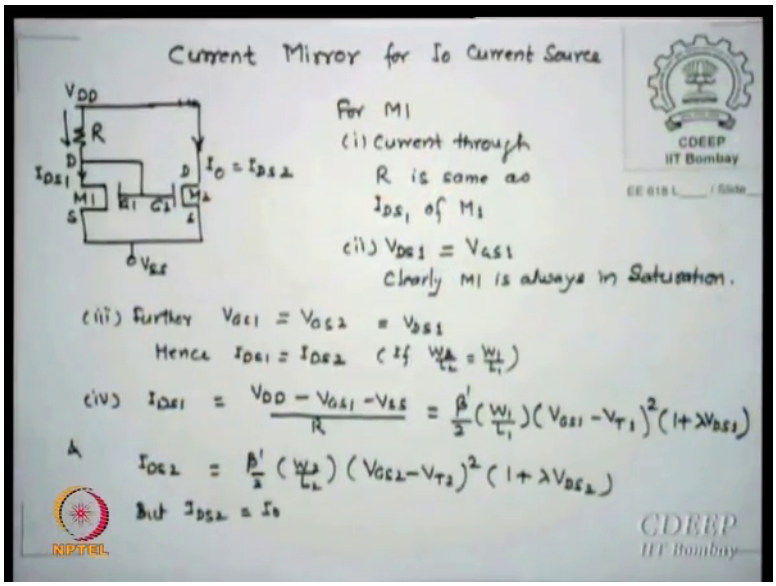

I hope that you appreciate what we are talking about that anything you have already done, but all that I am now trying to show you the piece of what you did in second year thirty or wherever you were is design perspective. It is not that this theory was unknown to you, you knew it anyway as good probably or maybe better than me, but now as a designer what I am looking at, but to know design we must go through theory a bit again. So, let us have a normal current mirror which is called simple current mirror shown here which is giving to me a current source of I 0 value, which essentially the way I had correct is I DS 2 or M 2s drain current, there is no connection here, please take it. So, it is V DD power supply I have a resistance R, then I have a transistor M 1 whose drain is connected to its gate. The two gates of M 1, M 2 are also connected and M 2 then has a current which is I DS 2 which I declared as my current source, which is I am creating from mirror. Mirror in the sense whatever in the first M 1 I am having that is mirror two M 2 that is mirror 2 M 2, and therefore, this name was given current mirror.

Since, I am connecting gates, so whatever is V GS 1 is same as V GS 2. If the sources are connected and gates are connected, V GS for both transistor should be same is that clear. And if the sizes are also same then what will be same, the currents will be also same is that clear. If their sizes are also same, I repeat what I say, V GS 1 and V GS 2 are equal, and if their sizes are also equal by I DS equal to beta, beta dash by 2 W by L V GS minus V T square. So, we say if V GS is same for both and we say both transistors are have equal currents. So, we have mirrored the current in the first to the two, but will calculate

they need not be equal and then sizes. So, we will just look into it. If they are equal then of course, I DS 1 is I DS 2 and I DS 2 is your R 0. So, we have current source which is proportional to are exactly equal to I DS 1. So, this is mirror one.

However, in case their sizes are not same which mostly will be I DS 1, now I can calculate the current please remember current in the resistor is the same current in M 1, because there is a gate which does not allow any dc current to flow. So, I DS 1 is V DD please remember this current in this R through R is V DD, this is shorted, this V SS sometimes this V SS will be 0; otherwise, it will be minus value. So, right now the way it is minus of minus, so it will add in fact, is that clear, please put V SS either 0, if given or minus of something.

So, typically what we do we said (Refer Time: 23:58) let us say I need a total power supply of 3 volts, so I have V DD I have put 1.5 V SS, I put minus 1.5. This is called symmetric rails, but it is not compulsory that it should be equal to one also can be done 2 minus 1 or minus 2 plus 1 also can be done. They are advantages and very, very poor thing all four problems also may appear if we change we need to be if there is not symmetric the analysis becomes very complicated.

So, we normally is always all books, all teachers we will take it simple solutions and maybe ask you what from what happens if they are not equal. So, this minus this they were subtracted by one of the V GS. So, we did in plus V SS you can say add in numbers minus V GS 1 by R is the current flowing in this. But this current in the transistor is beta dash by 2 W by L V GS minus V T square 1 plus lambda V DS 1 this logic of same this I DS to is beta dash by W 2 by L 2 V GS 2 minus V T 2. Now, if the transistors are not identical V T 1, V T 2 will also be different. So, as sometimes even lambdas may be different, but right now assume and lambda dash by L, L is say common for both devices which is generally the drain. So, I am not using separate lambda, but otherwise you should use separate lambdas as well.

And of course, as I say I DS 2 is the current source which I am looking for I 0. So, I have two equations I DS 1 and I DS 2. So, I take a ratio of I DS 1 by I DS source or I DS 2 by it is one because my I DS 2 is my outputs. So, I take a ratio of with reference to I DS 1 what is my I 0, I 0 yes is that I mean this is what you are done. So, this is just to replicate what I said.

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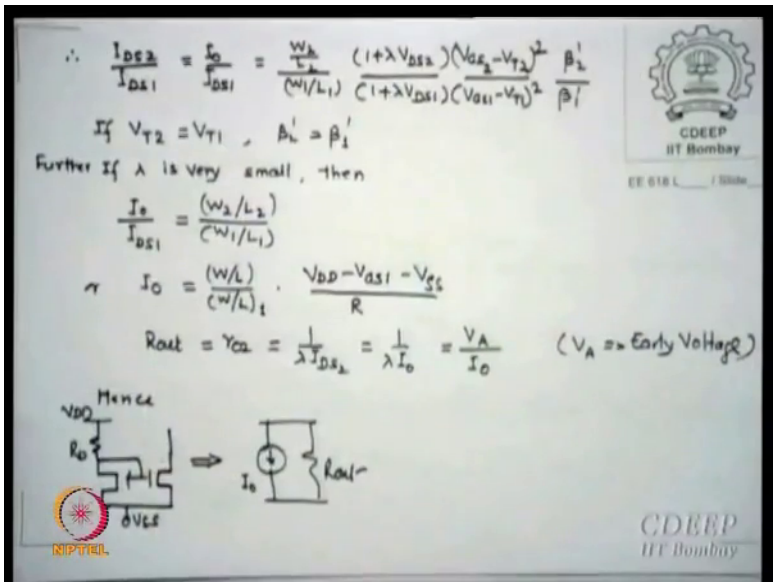

So, if I divide the equations I DS 2 by I DS 1 is I 0 upon I DS 1 which is equal to W 2 by L 2 divided by W 1 by L 1 beta 2 dash beta 1 dash (Refer Time: 26:15) is also right now kept separate. In case they are there you just cancel that they are seen they you can cancel that. Why I did this because there may be some p channel devices sometimes may come somewhere, so we do not want to write now write anything, but generally they will be canceled. V T they both are n channel in the same process of same channel length nodes, then beta 2 dash would be equal to beta 1 dash also V T 2 will be equal to V T 1 also lambdas are same.

And right now assume lambda is extremely small 0.05, a point zero in that case everything can be cancelled out V GS 1 is anyway equal to V GS 2 by force because you have connected the drain of n 1 to the gate off M 1 and gate of M 1 is same as gate off M 2. So, V GS 1 is always equal to V GS 2 if VTs are same this term cancels. If lambdas are small then this term cancel and if betas are equal this term cancels. So, all that I get is the ratio of sizes W 2 by L 1 upon W 1 by L 1 and then I substitute I DS on value which I derived as V DD minus V GS 1 minus V SS by R. I 0 is essentially the ratio of W by L of M 2 to M 1 multiplied by this current which is V DD minus V S minus V DS 1 by R.

So, if I want to design a current of value particularly what I will fix, I will fix R, I will fix R. I can also fix V GS 1 through which term V GS 1 minus V T is what?

Student: V ov.

Vov. So, I can fix access voltage a priori as I get 200 millivolts, 300 millivolts, VTs are given to me which I do not fix, but they are given to me. So, I can actually know what is my V GS one supply I am going to fix anyway for the technology I am given. So, 2.5 minus 2.5 for a 5 micron 5 volt technology, typically this will be why I am talking of 5 volt, 5 micron because much of the problems which they are solved better in actual design are given in (Refer Time: 28:40), there is one of the very good hardware engineering books. That for they are two books the latest version of Baker is also appearing.

And if you see them they are given the real life values of course, the only thing they did not want to show you the 0.25 or 0.18 micron results which new book of Baker has shown some of them. But old ones they wanted to keep because of the problems of the security or something they are all data given is only 5 micron 5 volt process. Since I may solve some problem from there, so I thought I will keep this value, but any other value data must be given to me. Like for example, of a 0.25 or 0.18 VO is normally taken 200 millivolts, but for higher it can be 0.4. So, it is not that this number is fixed this is what you design based on your power supplies.

What is the criteria for that the device should remain saturation irrespective because there is sufficient headroom must be available for me to keep device. So, this value is also not very fix, you can actually take some value around and use that also is that point clear. Typically as I say for most analog design which we do at 0.13, 0.18, 0.2, 1013 0.25, 0.18, we use this value of 200 millivolts. This is typical value, please do not think it over one of my student has taken 0.25 now that 250 micro you might have chosen. Because he must have figured out that by doing this yes, he is now going for laser headroom fair enough does not matter, but at least is keeping device guarantee lean saturation, so that may be his choice.

So, if I want to calculate therefore, I can and if I then fix the ratio of W by L 2 to 1; 1 of course, I will fix what should be 1 W by L by 1. Normally, the minimum W L 1 is one you can use you can use 5 micron by 5 microns as for a 5 micron process, but this is one and this then you accordingly put 10 micron by 5 micron, 20 micron by 5 micron depends on the increase you want to go beyond this. Typically, what is then R out for this circuit, the current source shunting R out is nothing but lambda I DS 2 which is 1 upon lambda I 0; and many a times, please take it one upon lambda is used as early voltage.

So, V a by and units it is correct V by R V by I is resistance. So, if given instead of lambda I may pre specified in early voltage I am specifying u lambda indirectly is that clear to you.

So, if also I give you lambda dash, and I am actually specifying the length. So, how do I design us look at the way given a value he actually I access to other parameters. So, typically you can see if this is in the order of micro amps, this will be order of 5200 volts, so you can see this will be order of mega ohms or above 10s of mega ohms. 10s of mega ohms is not extraordinarily large resistance compared to infinite, which you would have liked to, but even then relatively much enough good enough for normal use is that ok. So, this is a good current source we thought, but in reality we will say it is not that good because if we calculate the V min for this which we will use later and you will figure out that this is not that great is that class everyone written.

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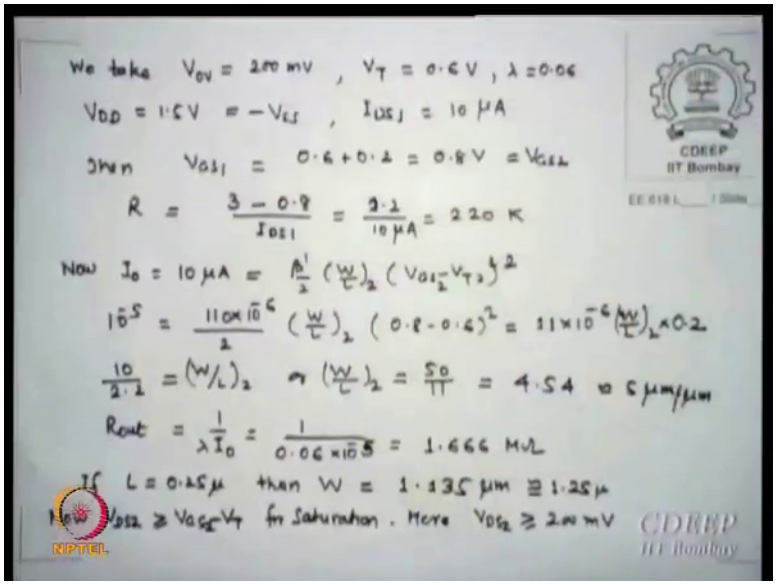

Here is some example which I am using maps quickly, V T 0.64 lambda 0.06 VOV 200 millivolt, supply voltage is 1.5 minus 1.5 V ss, I DS 1 is 10 micro amps. So, what is V GS 1, now I assume VOV as 0.2 volt or 200 millivolts. So, V GS 1 is 0.6 plus 0.2 is that how do I get my V GS 1 VOV plus V T. Since I am given a current in the first arm as 10 micro amps. I can calculate the resistance used as V DD minus V SS minus V GS 1 by I DS 1, which is around 220 kilo ohms. Essentially saying if I have a 2.5, 2.1 supply I put

220 k as the resistor; there the drain current of M 1 is 10 micro amps, is that clear, 10 micro amps. And I then calculate.

Student: (Refer Time: 33:50)

Yeah, yeah in a technology, it is normally fixed, you are right your point is right. In our case same because V GS 1 is same. So, we assume it is the V DS are also same, so vo is also same. If they are not equal then you can use differently, but in a technology is very difficult to change V ovs. Normally for keeping a transistor on saturation some value is fixed for all of them for p channel it may be different from n channel for all n channel will have same V ov.

Student: (Refer Time: 34:24)

If you have seen my earlier drafts, it does vary, but then you have to find optimum VOV there. If you have to plot it and figure out what V ov, I should use. If you see your earlier notes we are showing you if it varies what do we do finally, figure it out. See, analytically if you do if you keep varying then you cannot analytically solve then you have to go numerically or plots graphing is essentially in numerical solution. So, if you do numerically we will get exactly, but if I do analytically my assumption has to be something which I can evaluate.

So, if I 0 is 10 microns then beta dash by 2 W by L 2 V GS minus V T, VTs are equal let us say then I substitute all of it here and evaluate W by L 2 which is by 50 by 11, which is around 4.54 microns. It is taken from that technology is 110 micro amp per volt square. I think have I not written here, maybe this is written here the hundred and for n channel this value also will be specified to you for a technology mu c ox will be given to you. Typical value for 0.25 or 0.35 is 110 microns per volt square is the beta dash values, this is typical data is taken from 0.25 micron processing.

Why I am insisting on 0.25 as much, because most of the analog blocks will be designed on 0.25 or 0.18. But if they are mixed signal, which technology they will have to design whatever digital is asking I do not have any choice, they say 90 nanometers they said 12, 11 nanometers I will have to design all of it for that technology. But if I am only doing an opamp for my own sake or comparators I want to market on for board use, then I can design on 0.25. As I say scaling has some advantages, but it actually reduces the gain.

So, we preferably to have little larger technology node, but not too large because then it creates huge power losses. So, we are trying to manipulate that.

So, most analog chips which are marketed will be either on 0.25 or 0.18 some may be on 130 nanometers, but rarely on 90 nanometers. Please do not think there are some analog devices which are on 90 nanometers, but in general I have say. Almost all opamps which you see access areas 5 7 6 or that kind all of them are typically 1.2. But if opamp is a part of it digital network some system then it will have to be designed at that, and you will be surprise that gain of 10 to power 6 is unthinkable there. So, then you have to really worried about how best you can get solutions there.

So, think of it R out if I given lambda, so I get 1.66 mega ohms. If I choose length 0.25 typically around 1.25 micron widths are good enough for W 2. And you can evaluate you can get your source. We must guarantee V DS 2 should be V GS 2 minus V T for saturation, therefore V DS 2 must exceed 200 millivolts because then only we can say its remain same saturation.

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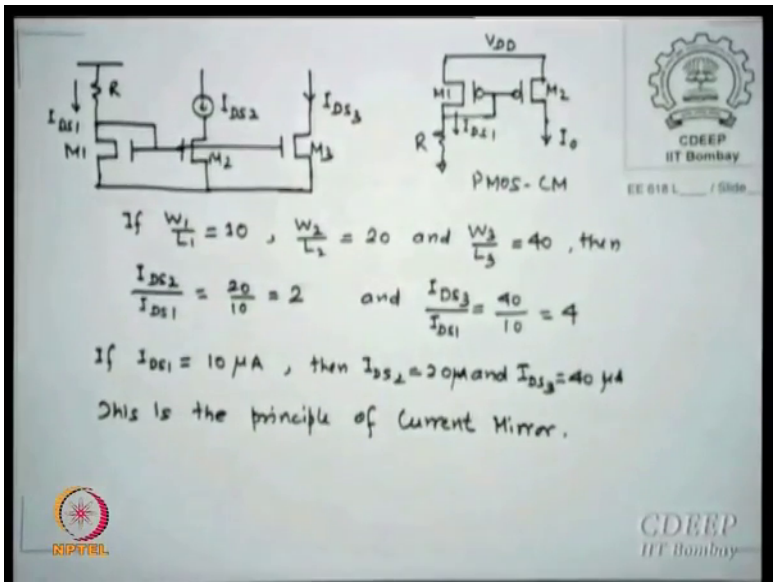

Here is some interesting features how mirrors are used, the mirrors are used to create currents in different arms. So, it need not be of the same current in different places. So, I may actually have this R M 1 based calculation to give me I DS 1, and then I can have W by l differently for M 2, M 3 as long as I connect their gates V GS 1 is equal to V GS 2 equal to V GS 3. And in that case, the ratio of this to this is W by L, ratio of this to this

W by L will give you the current proportional to I DS 1. So, it is I DS 2 by I DS 1 will be 2, I DS 3 by I DS will be 4, if these are the sizes. So, it will flow 10 micro amp, 20 micro amp, 40 micro amps currents.

As I said these currents are actually sinking you know because the currents are going towards ground. If you want to create a source kind, a p channel devices can be used, is that clear? In n channel current is going to the ground, if I had to take up from power supply I must create its current source which we can then use it only a p channel device I had two sorry. If a p channel device then I can have gates connected to drain of M 1 as they are, they were and then R is grounded and this is your V DD. So, current here and current here is the ratio of W by L of M 2 to W by L of M 1 same as n channels is that clear?

Now, I will give an example why I use this many times it is called sourcing combinations. So, is that clear? This is source and these are sinks, you need not call it that way, but the current entering ground is sinks, current coming from power supply is called source. This is the nomenclature need not be very seriously worried about it, that figure clear to you. So, n channel device I can create current mirrors so is. So, far if you want further currents else are what should I do extend this gate ahead put another transistor of different W by L, if you need a current of that proportional to this the third arm keep doing this as many as you want. Why we can guarantee M 2 there always in saturation of this M 2, because V GS 1 and V GS 2 are always connected to gate, therefore, if one is in saturation yeah there has to be inside. Here is something which you should learn because this is what yes no it does not because V GS 1 and V GS 2 is decided by this minus this one time only, this value minus this is this value is that clear.

So, that is one time decision, R will decide how much is you are actually getting is that correct, but a given this minus I R plus V SS is the all that the V GS will be so which is getting fixed anyway through R. This another issue which many designs will require is the following is that this plus.

Student: sir V DS always carrying between.

V DS 2 why should it very very;

Student: (Refer Time: 41:57)

V DS 2 will be always equal to V GS 2 will prove it, it is always at the edge of saturation, we will come and showing.

Student: (Refer Time: 42:07)

Whichever is the current there, it will always be equal to V DS 2 will be V GS 2, just take it so that device is permanently in saturation.

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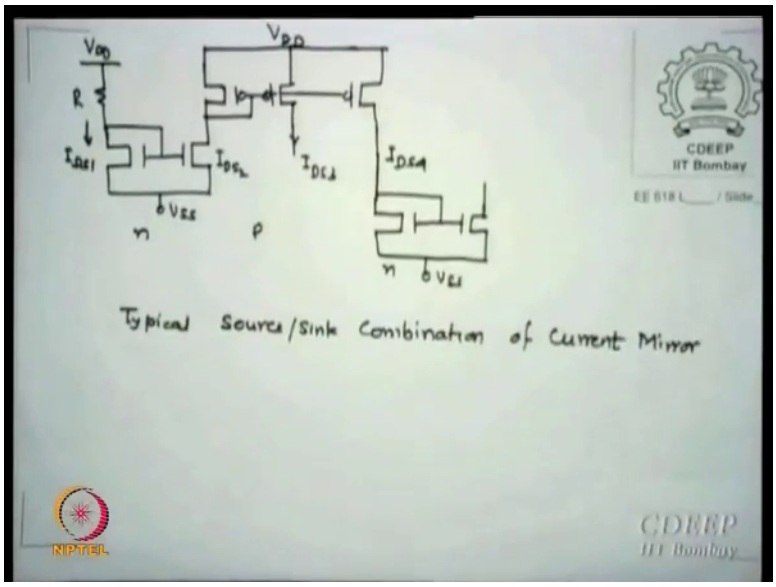

Here is a method of transferring currents; you create a n channel current mirror which is sink kind. And then you want to transfer on a p channel device at the source current. So, you have another p channel source area. And please remember now I do not need R there, what is that R was giving you anyway current. So, this current of I DS 2 in acting like a source current or the bias current for this mirror. So, if you want further go down for another n channel requirements ahead, you bring this instead of all now same current can go to the next n channel block and you can run through. So, what can I do it for example, this is 10, let us say this is 10 and for say reasons this is double the size this is 20, let us say this is 40. Now, this is 40 and if I double it this is 80. So, do not jump from 10 to 80 in one go, is that correct. Do not jump that means, do not put W by L 2 equal to 8 here to make it 80 currents 8 times current why, what is the problem if I make W by L 8 times what is the problem?

Student: V T (Refer Time: 43:43)

Now, the major worry probably is the capacitances there is that correct capacitances there. The another problem is in layouts as we call. What is layout issue layout means sizing if you do? What is the aspect ratio do you know length and width, length by width is called aspect ratio. If something is the aspect ratio is like this and some as like this, then any drawing scheme will make error on one or the other is that correct. So, typically devices should be of same aspect ratio or close aspect ratio is that point clear to you. This is graphic problem not really a problem of device, but graphically when h line which is 0.1 micron and 20 micron length, I will have much more errors get to that length all about 0.1 everywhere. Instead if I have 1.1, 1.1 and accordingly adjust then I can get more accurately the ratios which I am looking for is that clear. This is called traffic problems on chip.

And therefore, layouts when you draw, you do not put larger device in one go parallel them if possible as many as if you wish to increase W by L, is that correct this is essentially paralleling. It also distributes the power, so that it does not consume at one point huge powers is that clear to you. So, therefore, p to n; n to p is a normal method of jumping from low currents to high currents, is that clear to you. Please take it that if you make a spice simulation with eight and you get and you extract and it comes back do not get satisfied because you are not done thermal analysis, in actual chip that thermal part will appear anyway whether you like or. So, the chip may on the circuit may work, but in real life it may not or as good, I would not say it not, and therefore, these issues should be thought a priori.

So, these are design issues this is nothing to do with it actual mirror, mirror could have been simple whatever ratio you want, but in design one must think how many ways we should go so that it is universally acceptable values which you can get. I agree, but eight fingers still are in parallel capacitance. So, they are adding there. They are powerless heat problem probably is minimized, but the capacitance problem is not minimized because they are at the same node all capacitance this actually distributes the capacitance

Student: graphic (Refer Time: 46:26)

Traffic it can solve that once you are individual transits that is what fingers do now that they solve the aspect ratio problem. But the capacitance had that node is still some of them whichever you do is that ok.

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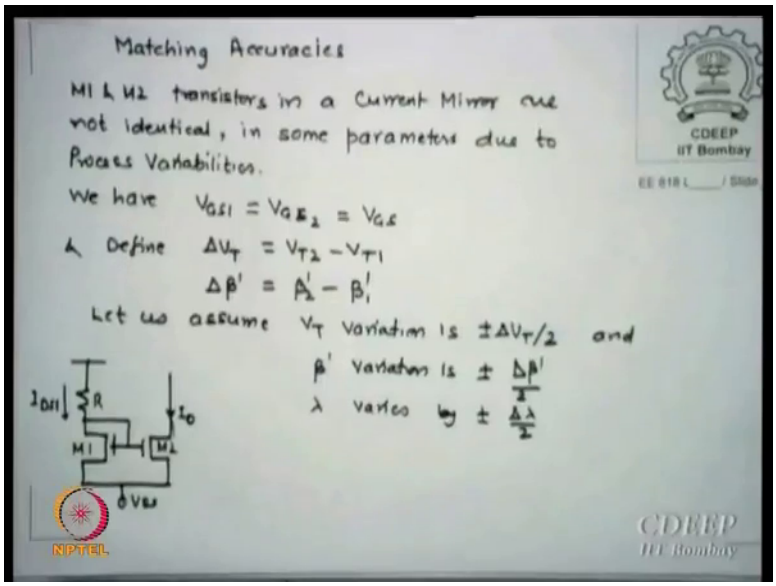

Now, there is an issue which we must look into before we proceed further the issue comes that how much is your so called transistor M 1, M 2 are identical because all the mirror was talking is W by l ratio only or VTs were common know this so common. So, how much is the mismatch between the two transistors or number of transistor you are going to use, we will decide some way the accuracy of current mirrors. So, what I am saying if there is a variation and I have taken a simple case I am going to solve for a plus minus variation equal variations and figure out what is the percentage of variation at the output current, if these device has changed by so much let us say 5 percent. So, is the current ratio changes by 5 percent, 3 percent error, what is the percentage error if this inaccuracy occur, either designer I am now worried, because I am shrinking everything and I am worried how much accurately I am doing that.

So, this is an issue which as I say now has taken into prominence because we have started worrying about inaccuracies. The inaccuracies come from varieties of ways which are called variability issues in process and they cannot be handled by anyone these are there for those who are device background to some extent there is a finfet. So, there is something called the thickness of the thin, there is also a spacer thickness there is also the length up to which the spacer ends, there are seven parameters which we go on finfet design. Now, which one is dominant, we do not know because all of them may vary with all processes.

So, nowadays there is an issue which one should be controlled better than compared to all of this and there is an issue which is now worrying every 90 or 45 nanometer down thing. One good news always something goes bad luck favors you as you go for 16 nanometers down or 12, 16 or below the scaling law has changed now, it is not really scaling. Say for example, if you see this is additional feature just I will come back, we are thinking that oxide thickness is scaling like this as years, actually it is not now it is like this. So, much of my worry has actually reduced in 16 nanometers. So, gain and I say happens people are smarter than the device, but device becomes at the end much smarter. We are trying to understand the process and the circuit relationship and then to the performance system and we are trying to get some kind of what we call thumb rules.

What are thumb rules they are no real legal status, where we say V T varies by delta V T by 2 beta dash varies by plus minus delta beta as by 2, lambda varies by delta lambda by 2 for M 1 and M 2 is that figured drawn, earlier drawn. The next slide will actually explain what I meant. This analysis is not new, this is done many years of clear also it is not that I am doing only I am doing it for (Refer Time: 50:12) right now here this is the very common analysis. And this is not true only for this device this is true for everywhere whichever variation, this is how one solves the sensitivities is that ok, everyone.

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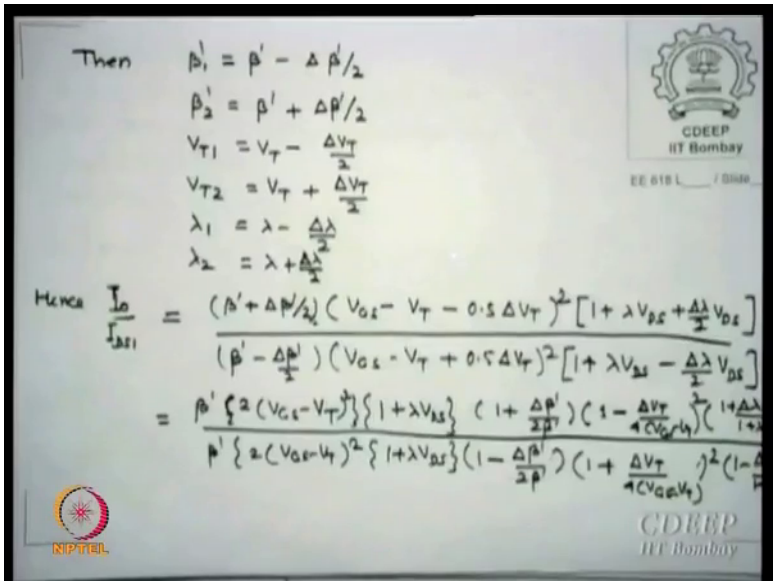

So, we like based on the analysis which is based on the thinking I said beta 1 dash is beta dash minus delta beta dash by 2. Whereas, beta 2 dash is beta, beta dash is an average value over which one is less than delta beta dash by 2, the other is plus delta beta dash, this is only the variation. So, what is the net variation delta beta dash? But half is given here and half is given there, similarly for V T, similarly for lambda. And now I take the ratio of I 0 2 I DS 1 this is my beta one dash into sorry beta 2 dash into V GS minus right now I am assuming VT s of this sorry this kind. So, is that correct, V T the average value plus delta VTs because this is subtracted, this is minus square 1 plus lambda V DS plus delta lambda by 2 V DS. The I DS 1 current follows the one, one values beta dash minus delta beta dash by 2 V GS minus V T plus 0.5 delta t square 1 plus lambda V DS minus delta lambda by 2 V DS minus comes because this is minus.

I take out this big term out I take beta dash from here, I take V GS 2 times V GS minus V T outside here. And from here I take 1 plus lambda V DS here. From each of them the first two terms I take out, so that becomes beta dash into 2 V GS minus V T square plus 1 plus lambda V DS. Now, for this the term when you take beta dash out is 1 plus delta beta dash by 2 beta dash 1 minus delta V T upon 4 V GS minus V T square 1 plus delta lambda V DS upon 1 plus lambda V DS and opposite sign correspondingly is this; however, these two values are say. So, they can be canceled this is taken only to remove something from nominee denominator and numerator is that ok. Just each part common terms I removed, so that I can remove those terms is that ok? So, sorry you can redo yourself if you wish.

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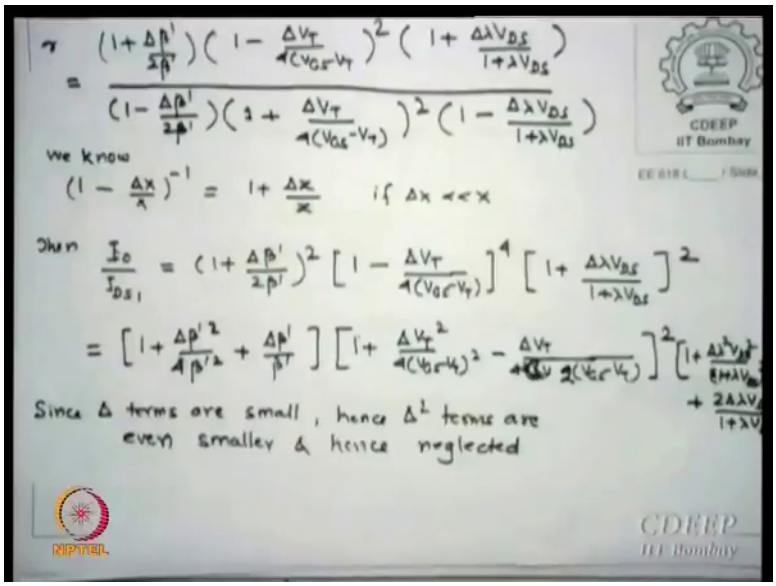

That the cancels term after that you get one plus delta beta dash by 2 wilt I have 1 minus delta which is the square plus 1 plus this divided by minus signs corresponding opposites of that. However, 1 minus delta x by x to the power minus 1 if delta x is much smaller by binomial expansions, it can be written roughly equal to 1 plus delta x by x. So, 1 minus delta beta is the; what I am doing it now there is a [FL] term [FL]. So, I get I 0 upon I DS 1 is 1 plus delta b dash by 2 b dash square 1 minus delta b t upon this to the power 4 into 1 plus lambda V DS. And the assumption is the deltas terms are much smaller which is why they are called deltas and binomial expansion is valid, all higher terms are neglected. Then I expand square terms something square I can write a square plus b square plus 2 a b or minus 2 a b whichever is a minus b or a plus b. So, I expand this I expand this I expand this. Then what did I say what do I what can I say if delta is small all delta square term is still smaller, so [FL] number simply expression [FL].

You do yourself and verify, but this whole trick I am using is to prove that if I want to calculate I should get a very simple expressions. So, here delta square terms delta square terms or delta square terms are neglected by me. As I say these numbers should be maybe right also, just check the numbers. If there are two just used two, if they are four use four, [FL] a plus b or a minus b [FL], a square plus b square minus 2 a b or plus two a b nothing great, no maps is that ok, all of you?

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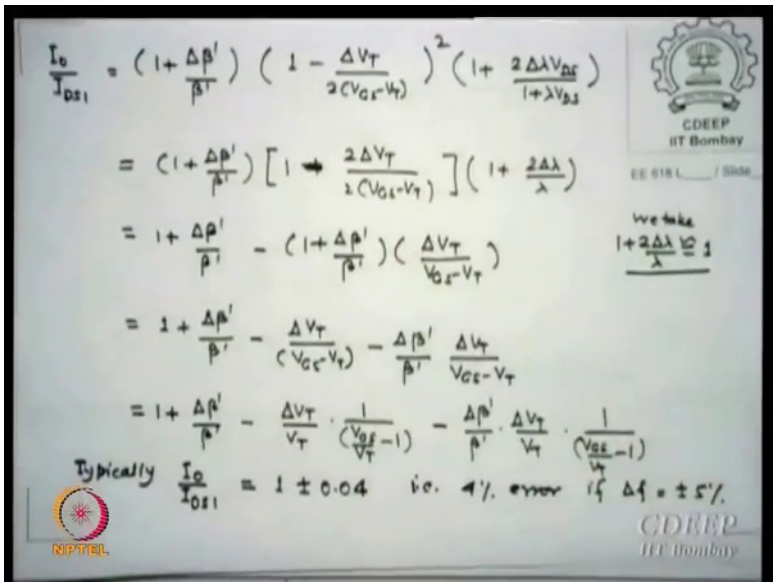

So, if I do that I neglect those this term I get this expression; lot of game I play. You look at this last before you write the first line 1 plus 2 delta lambda V DS by 1 plus lambda V DS I say lambda V DS is normally larger than 1, V DS is more. So, a neglect 1, and if I neglect 1, I can calculate removed V DS then I say I get 1 plus 2 delta lambda by lambda, but delta lambda by lambda is very small, so I neglect that also. Then you can keep them, but this is how I quick calculations if you want to do how much you will figure it out how do I do.

So, if I keep doing this analysis, I expand this I multiply these two terms, this I became I removed it because I say 1 plus 2 lambda by lambda is 1. So, I get final expression is you can rewrite by then was see 1 plus delta beta dash for beta dash minus delta V T V GS minus V T minus delta beta dash by beta delta V T upon this. If I take delta V T by V T out delta like being this delta beta this why I write delta V T by dT delta what is that way I am telling then the percentage I can actually declare. So, I just do tricks on that. So, to say if you have function variation within plus minus 5 percent, I 0 to I DS ratio will be within four percent of error. These are for a specific values you may get more earlier depends on V GS minus V T is used and yeah only V GS minus V T use, yes, dominant if [FL] term minus [FL] you got it?

This may be 5 percent this may be totally have 1 percent, so 4 percent error you are going to get if 5 percent error you see in the VTs or in sizes or in p terms is that ok. So,

this is how one evaluates the errors because this is something very crucial how much accuracy I am holding when I say I am mirroring it, is that clear? How much accurately I am mirroring it. So, these numbers are not really great or something just to tell you that do not believe that exactly transfers it does not and depends on the values it may be even more or sometimes even less is that ok? So, we will continue with this.